Pixel Luminosity Telescope

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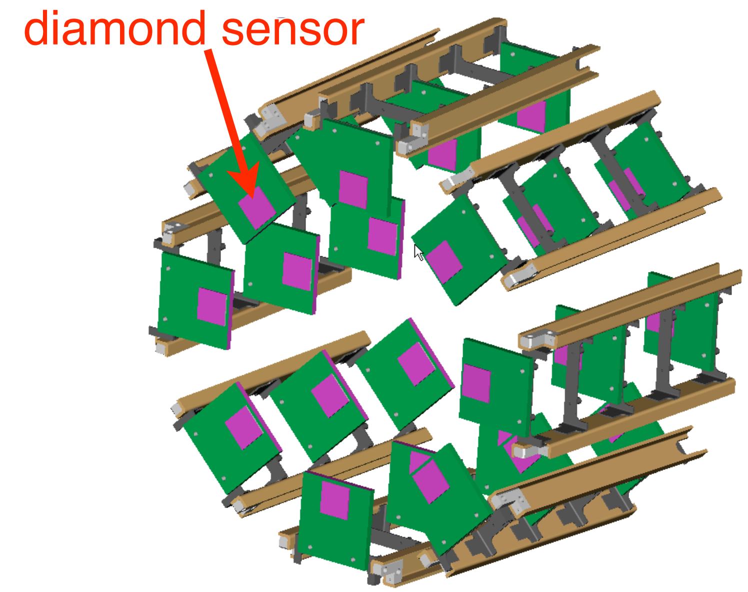
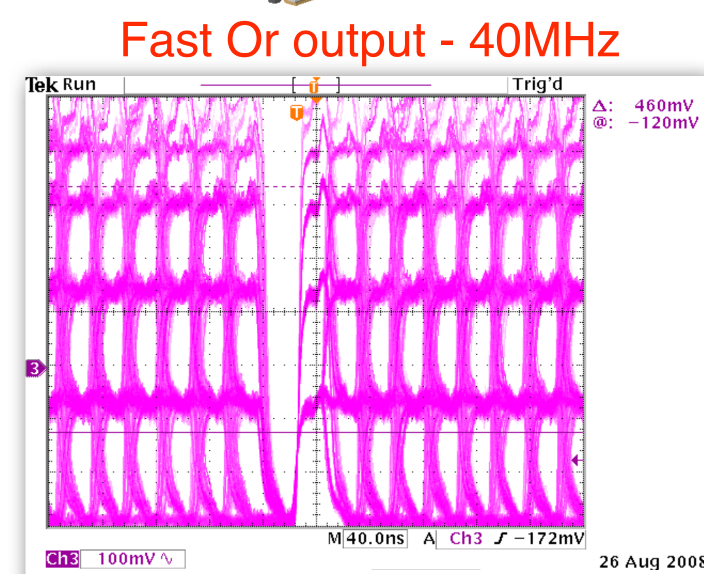
Outline

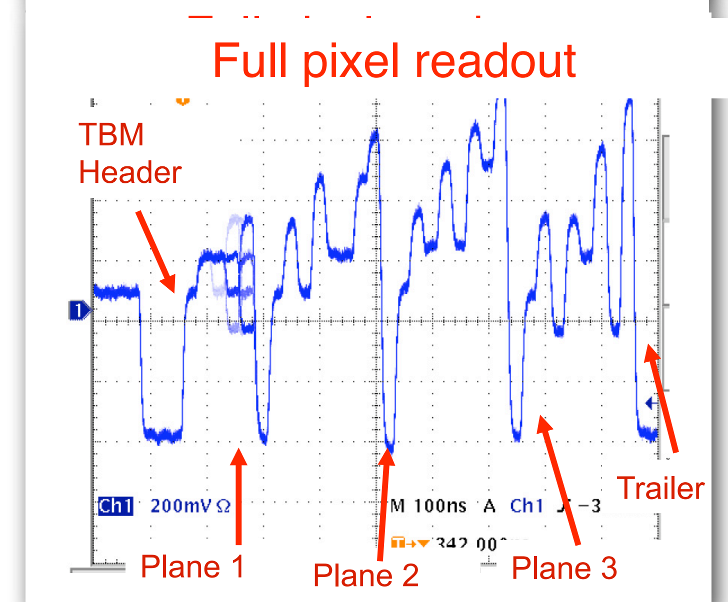
- PLT introduction
- Developing of the bump bonding
- Test beams experiments
- Current projects

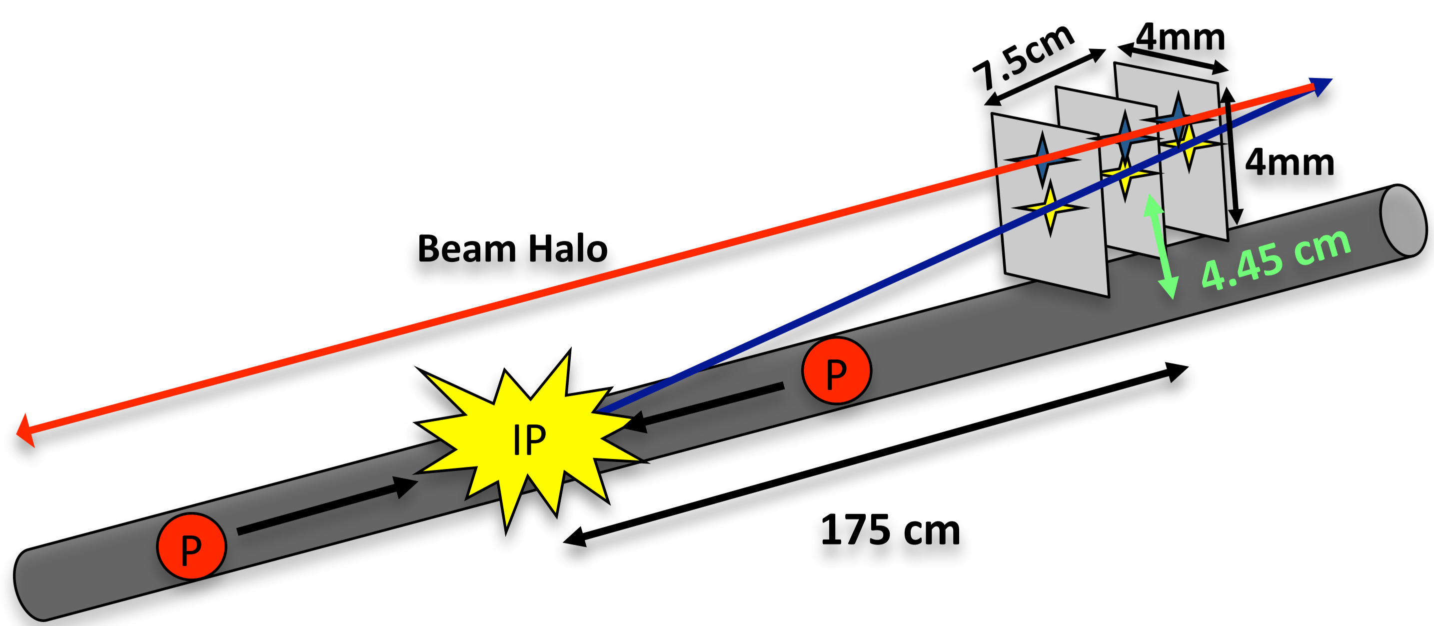
PLT project overview

- PLT is a dedicated luminosity monitor for the CMS.
- Designed to measure relative luminosity with better than 1% precision.
- 8 telescopes (3 planes each) on each side of the interaction point at η~4.2.
- Each plane contains pixelated **single crystal CVD diamond (active area 4 mm x 4 mm) sensor** bump bonded to the CMS pixel readout chip.
- Dual readout mode.
  - FastOr mode for measuring luminosity at 40MHz rate.
  - Full pixel readout for calibration, diagnostics, and systematic correction of the fastOr mode (1kHz to 10kHz).



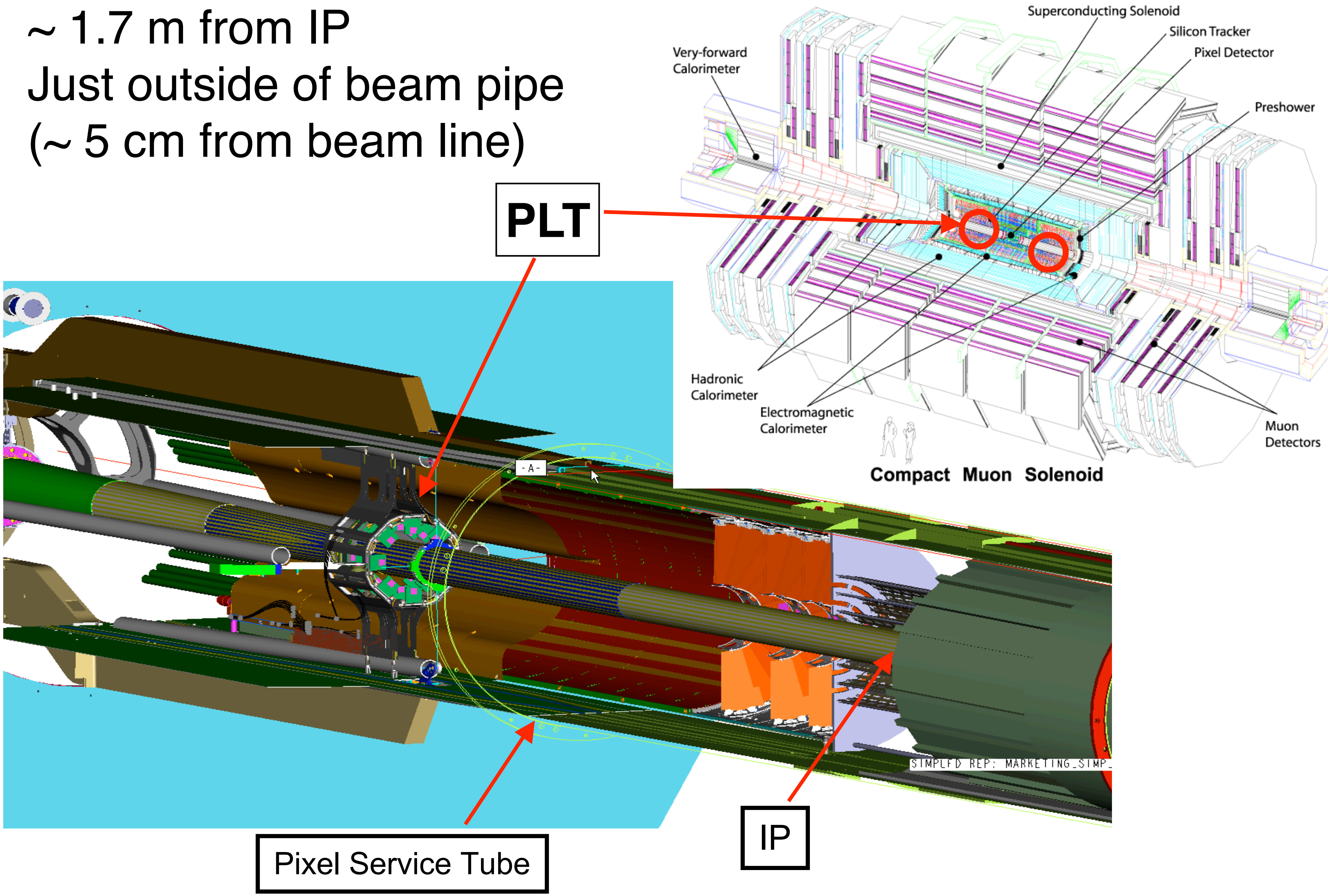






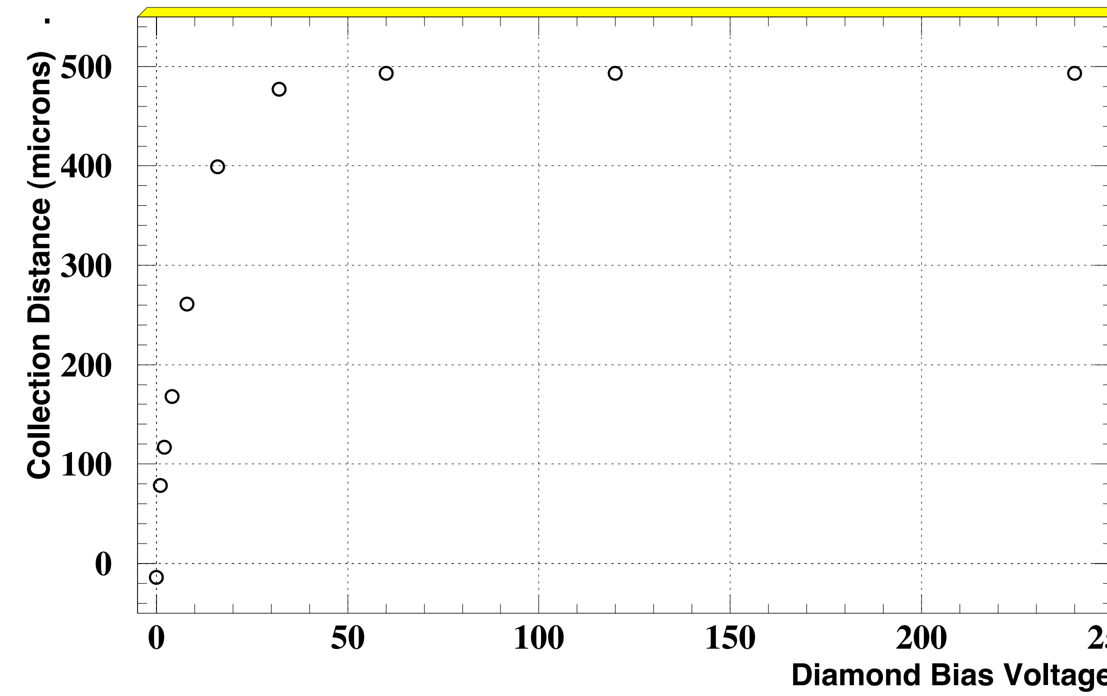
Location of PLT

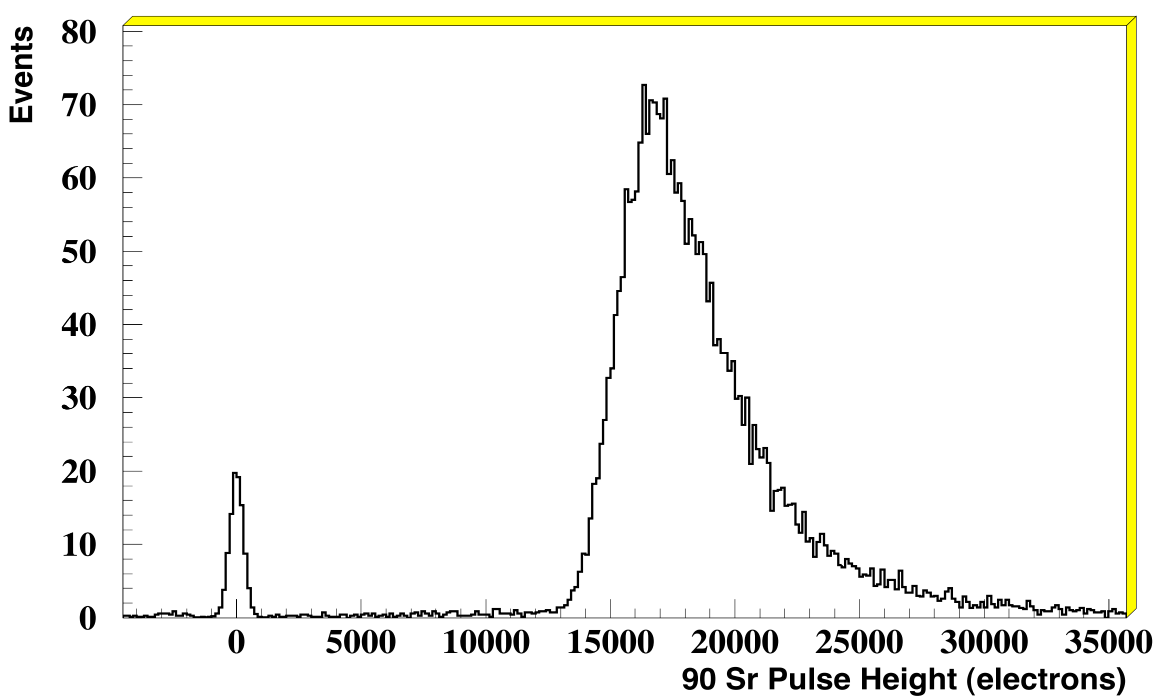
- ~ 1.7 m from IP
- Just outside of beam pipe (~ 5 cm from beam line)

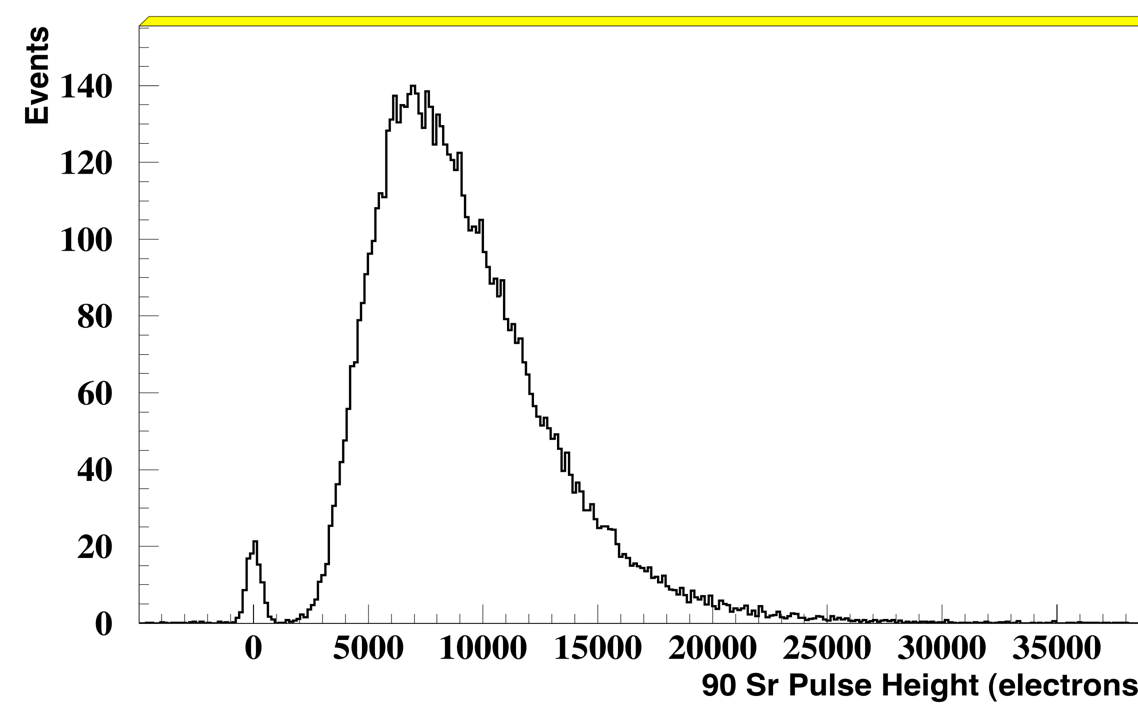


Diamond Sensors

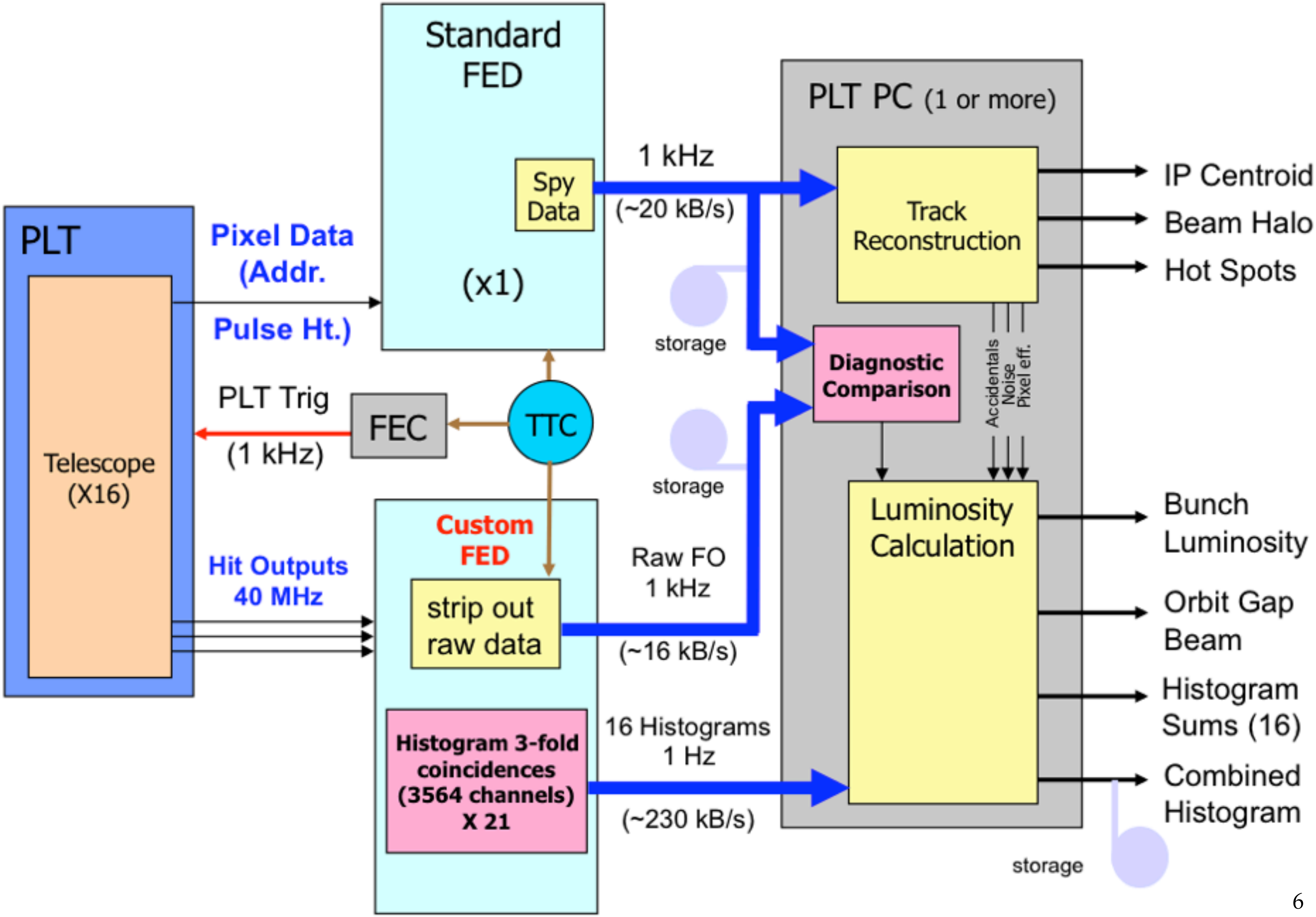
- Radiation hard (few × 10^{15} p/cm^2)
- No need for cooling
- Full charge collection < 0.2 V/μm
  - ➡ 18,000 e^- signal for 500 μm diamond
  - ➡ Landau 60% narrower than for Si
- Pulse height well separated from pedestal
  - ➡ compare poly crystalline diamond





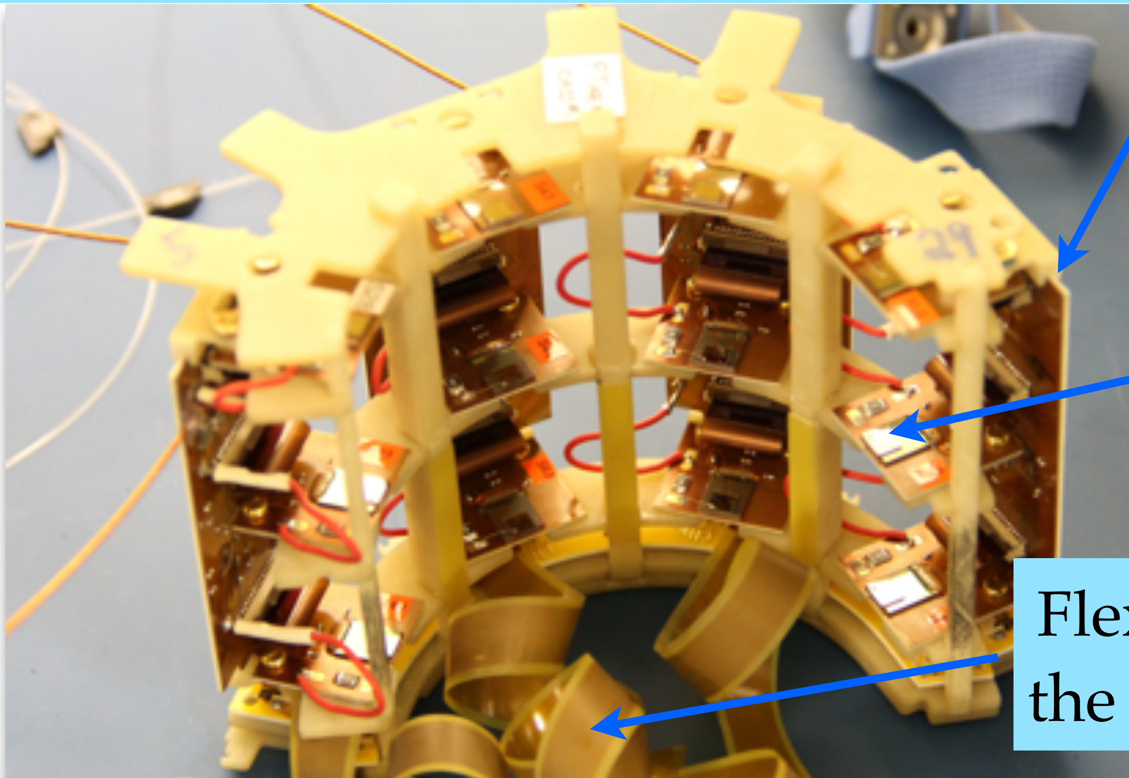


Data Acquisition



PLT in pictures

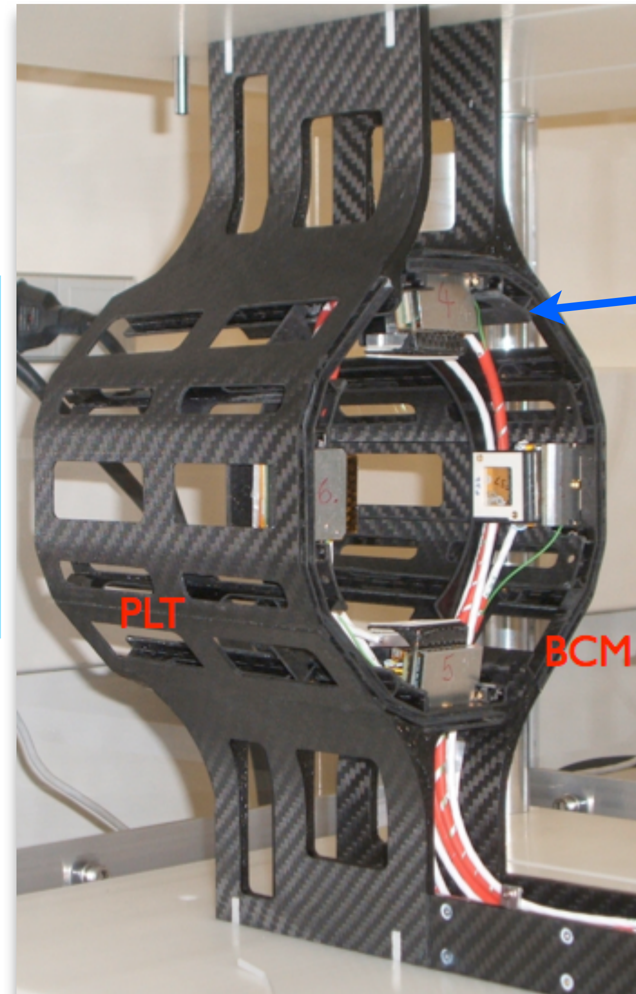
PLT Cassette



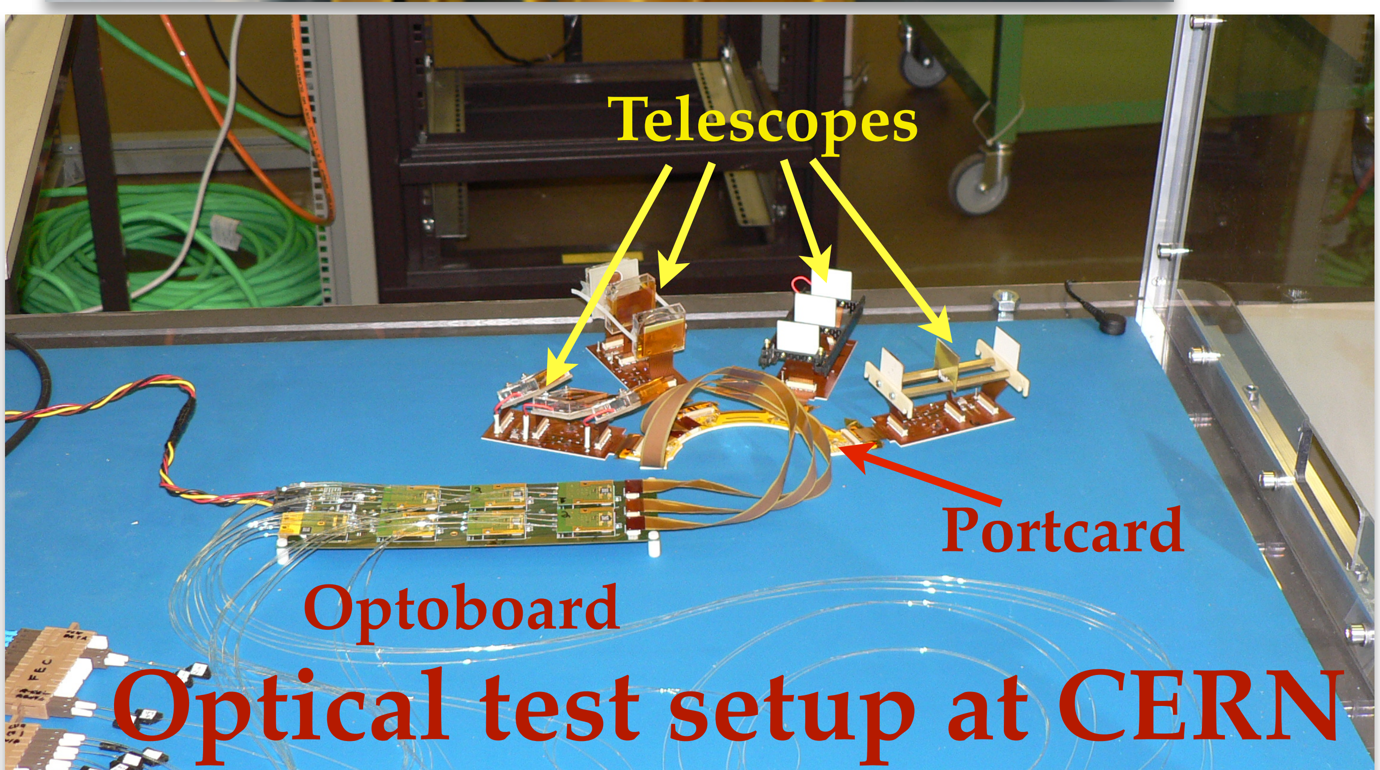
HDI

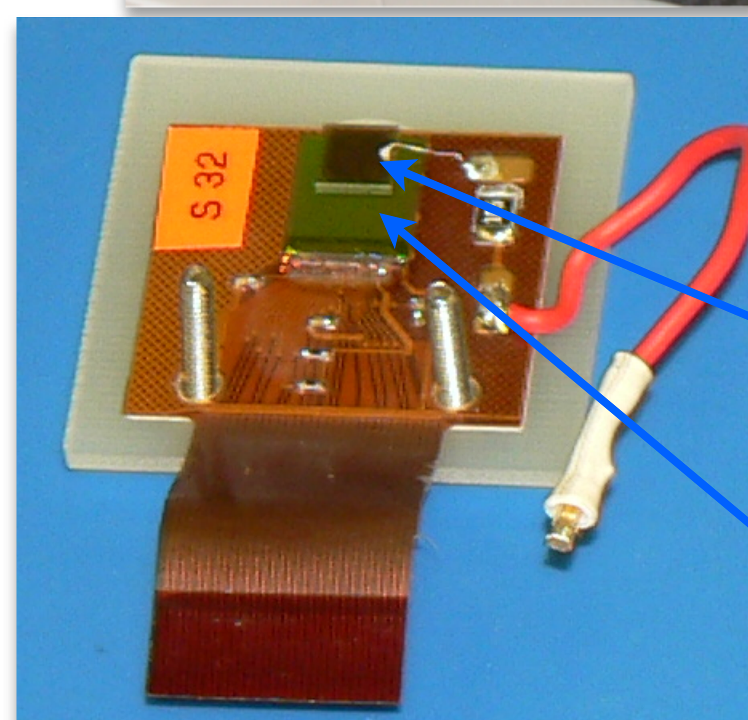
Hybrid with diamond sensor and readout chip

Flexi-cables to the opto-board



PLT / BCM carriage (2 half-carriages)





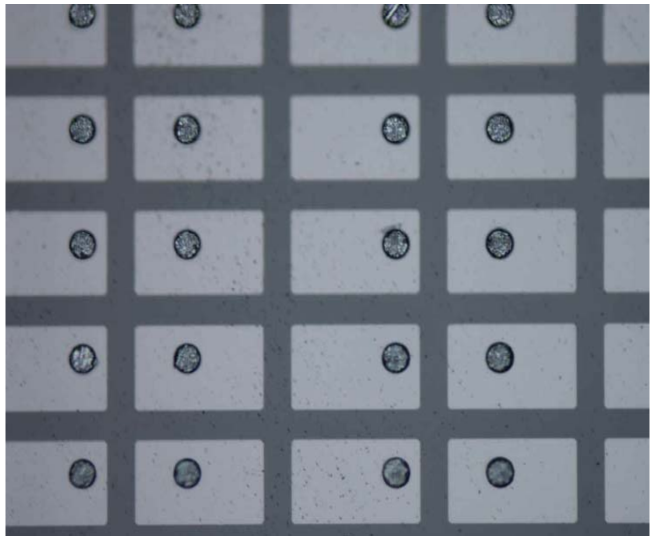
PLT Hybrid board

Diamond sensor

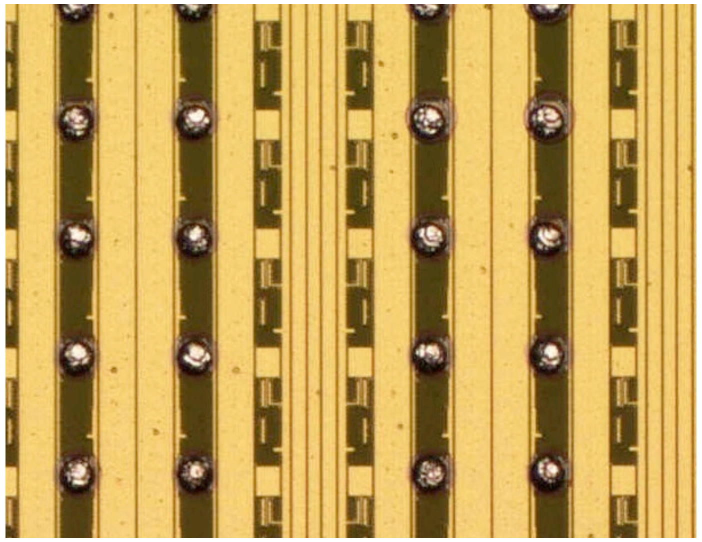
CMS pixel readout chip

Developing bump bonding

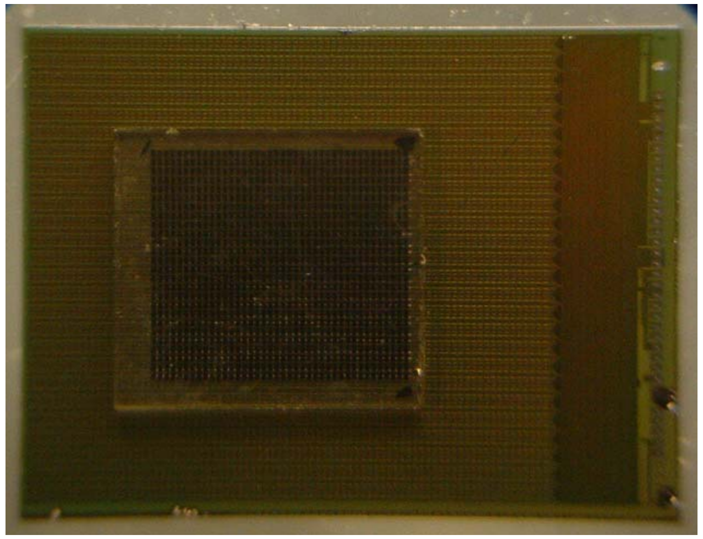
Challenge: Bump bonding individual 4.7 mm × 4.7 mm diamond sensors to single ROC die.



Bumped diamond

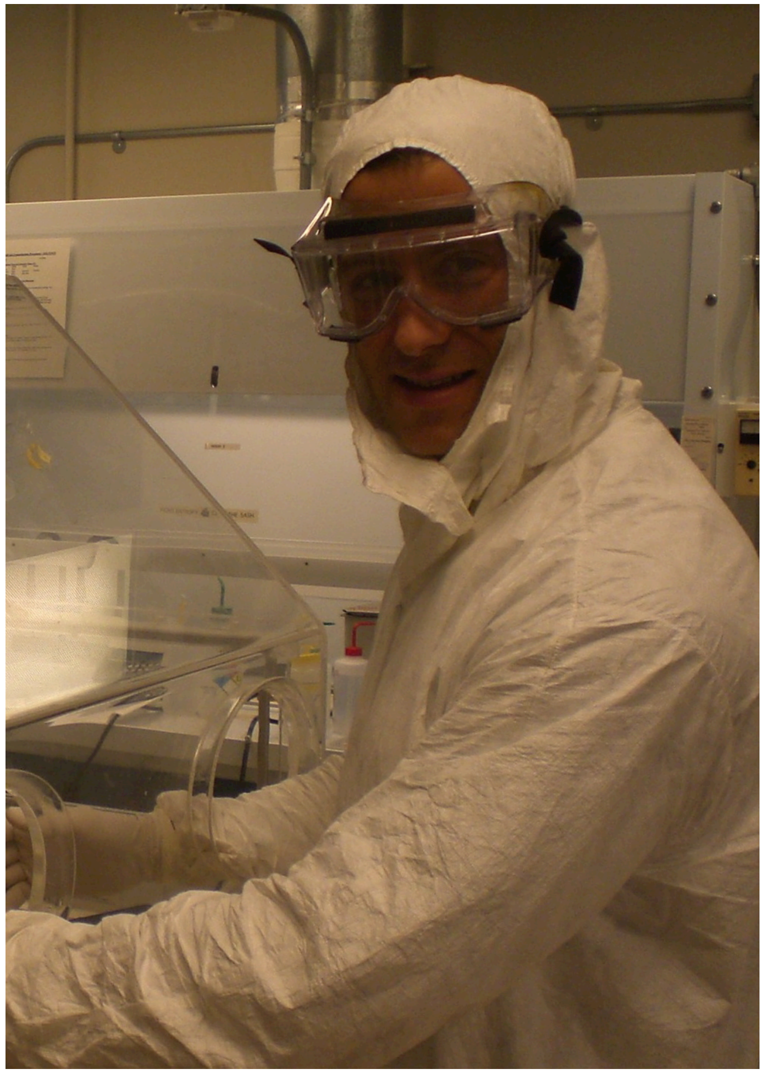


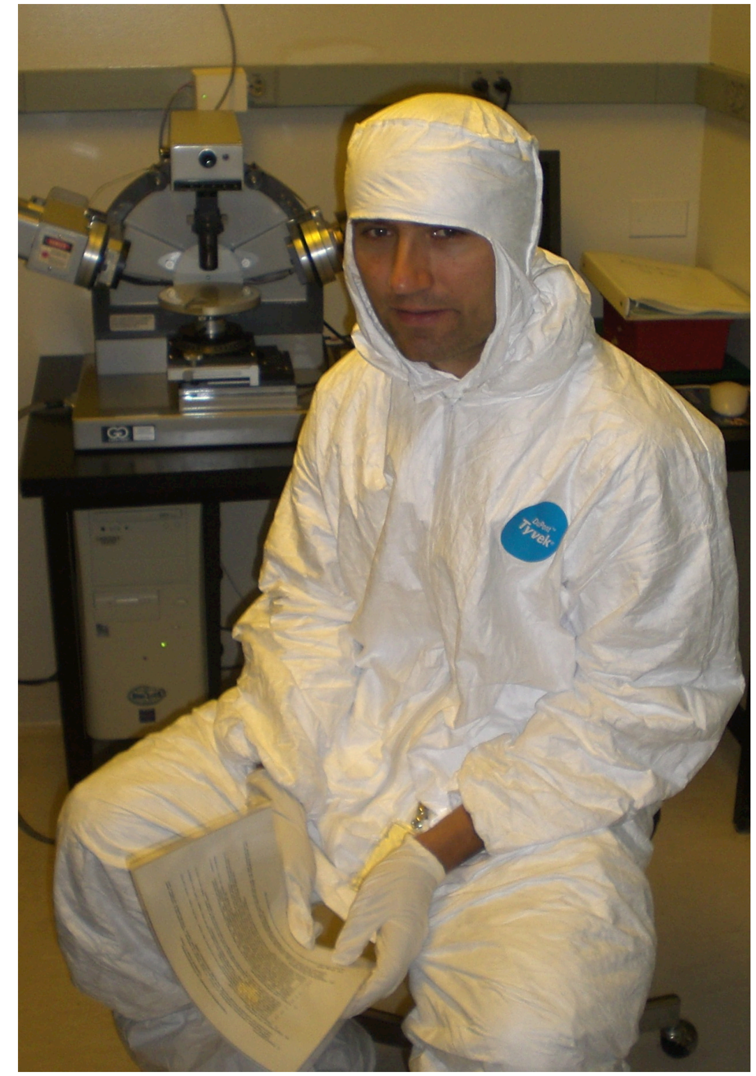
bumped ROC



bump bonded detector

Developing Indium Bump Bonding Process





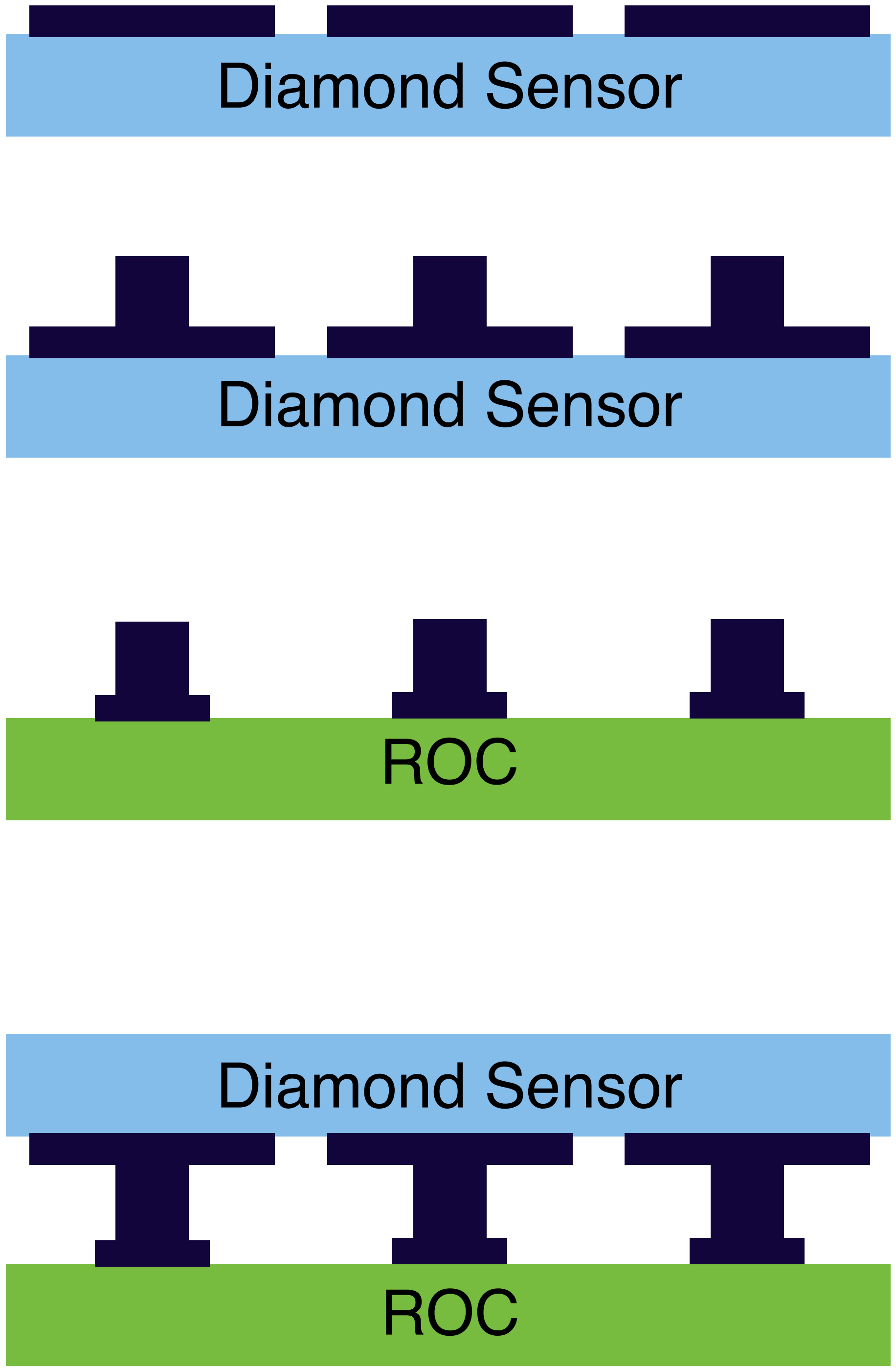
- Most of the development work was done by:
    - ➡ Princeton University technician -Bert Harrop
    - ➡ Rutgers University graduate student - myself
        - 4 years experience in semiconductor industry

PRISM

- Princeton Institute for the Science and Technology of Materials.
  - ➡ 500 m^2 Class 100/100 Cleanroom Micro/Nano Fabrication Laboratory.
  - ➡ Full technical support staff of fabrication Engineers that provide industry insight on the latest in micro/nano fabrication.

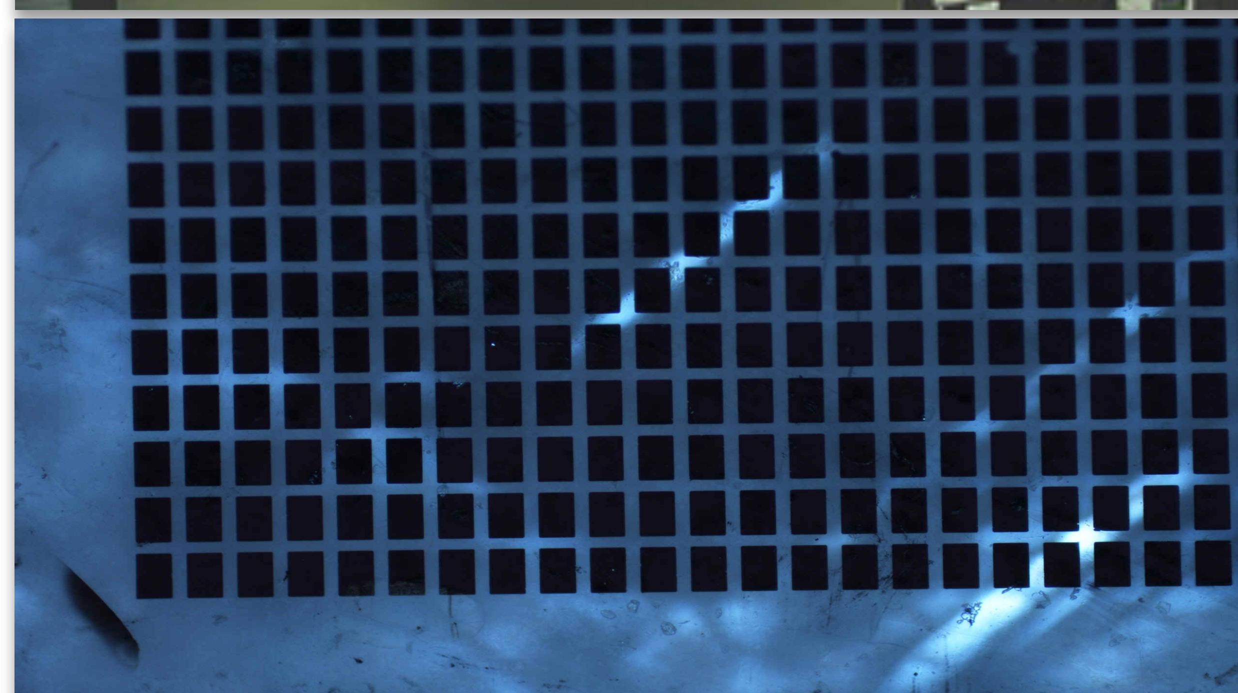
Bump-bonding outline

- Put Ti/W pixels on the diamond.
- Anneal.
- Put Indium bumps on the diamond.
- Put Ti/W on the ROC pixels, followed by Indium bumps.
- Flip and bond.



Ti/W metallization on diamond sensor

- **Pattern diamond (Photolithography)**
  - ➡ Spin on resist (AZ-5214) 4000RPM for 40 sec)
  - ➡ Pattern Expose using the MA-6 (2.0mW / cm^2) for 90 sec
  - ➡ Plasma de-scum.
- **Sputter TiW - Angstrom Engineering Metal Sputterer**
  - ➡ Sputter ~150Å of TiW onto diamond
- **Liftoff**
  - ➡ Acetone Soak overnight.
  - ➡ Ultrasound 5 second.
- **Anneal at 400 °C in O_2 atmosphere.**



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Double layer lift-off process
(principle)

1st layer of PR

Flood Exposure

2nd layer of PR

Pattern Exposure

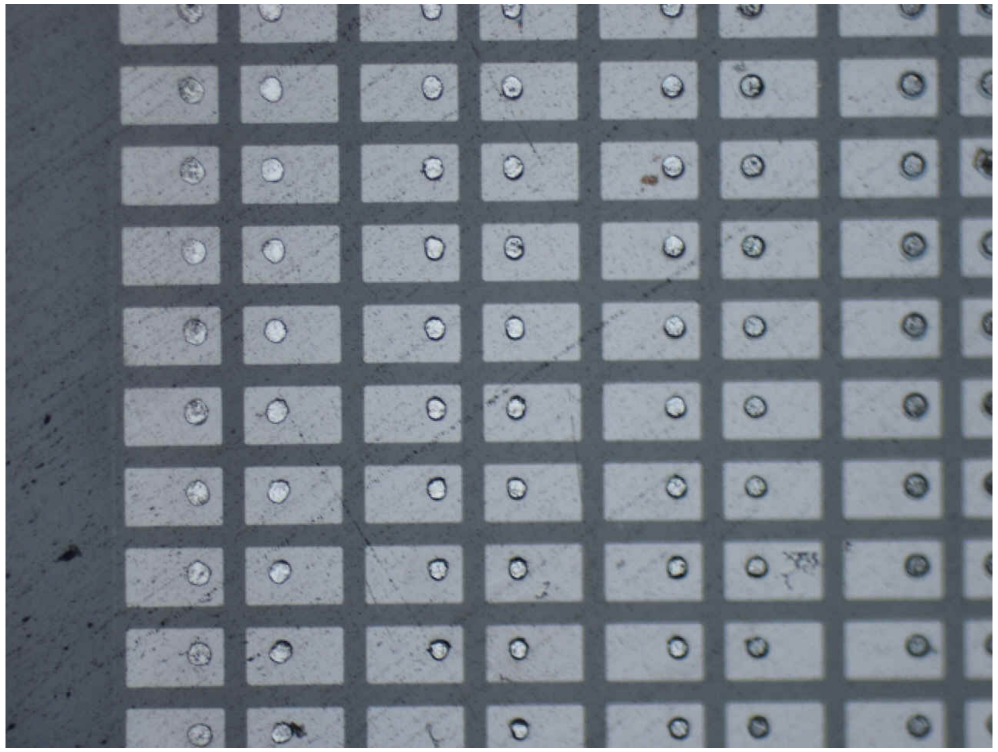
Develop

Deposit Metal

Lift-off

Indium bump process

- 1st Layer (6-7um)
  - Spin resist (SPR-220) @ 250RPM for 15sec then 1200RPM for 40sec
  - Soft-Bake (on hotplate) Ramp 60ºC to 100ºC (Hold @ 100ºC for 2 min)
  - Flood Expose on MA-6 (2.0mW/cm^2) for 400s
  - Hold for resist setup at least 2-3 hours better overnight (24hrs)
  - Post Exposure Bake (on hotplate) ramp: 20ºC to 90ºC @ 180ºC/hr, hold @ 90ºC for 2 min)
- 2nd Layer(6-7um)
  - same steps as above but instead of flood exposure do pattern exposure
- Develop in 1:1 with DI:AZ312MIF
  - 2.5 to 3 minutes
- Deposit 7-10um of Indium
  - Rate = 50Å/sec
  - Thickness = 70 -100KÅ (piezo-crystal does not work at this thickness, finish by time)
- Liftoff
  - Acetone Soak overnight
  - **No ultrasound!**



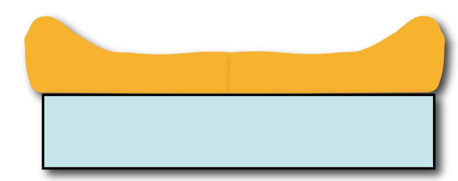
Edge bid effect.

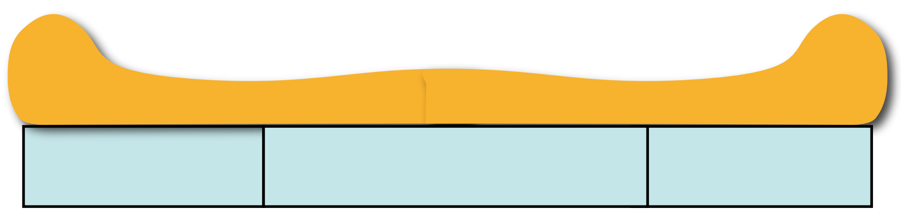
- During the spinning of photo-resist on a sample a build-up of resist occurs at the edges.

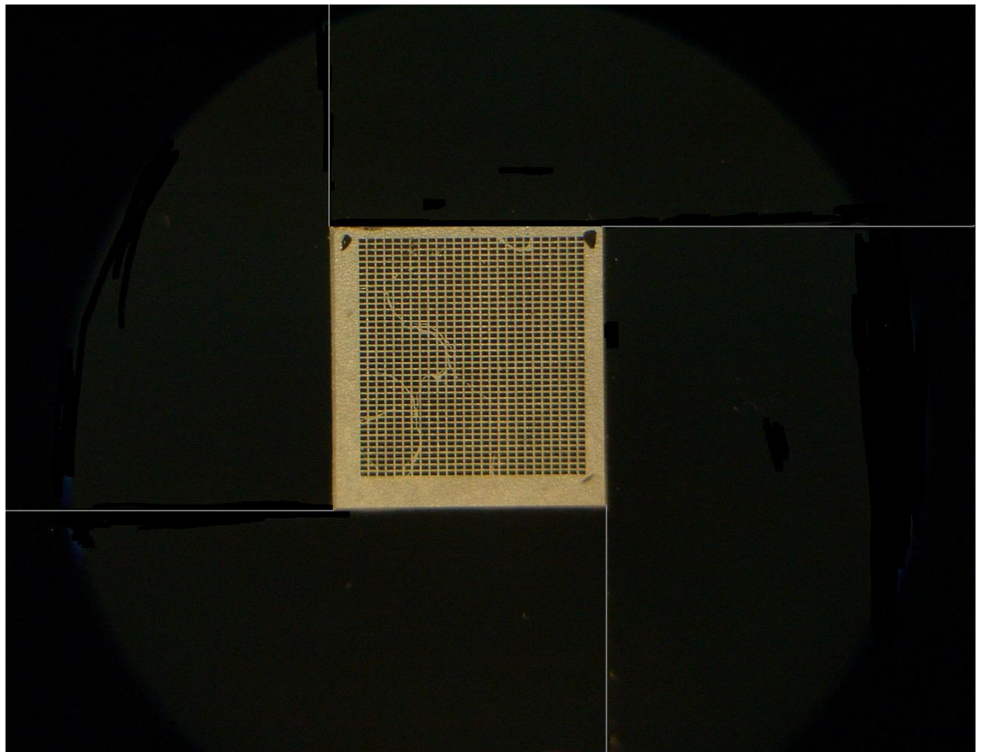
- We eliminated the edge bead on the diamond by placing a frame around it and leaving the build up on the sacrificial frame edge rather than the diamond.

    - Place the diamond, pixel side down, onto vacuum fixture and secure with vacuum.

    - Place frame segments face down surrounding the diamond, mounted as close as possible to prevent gapping.







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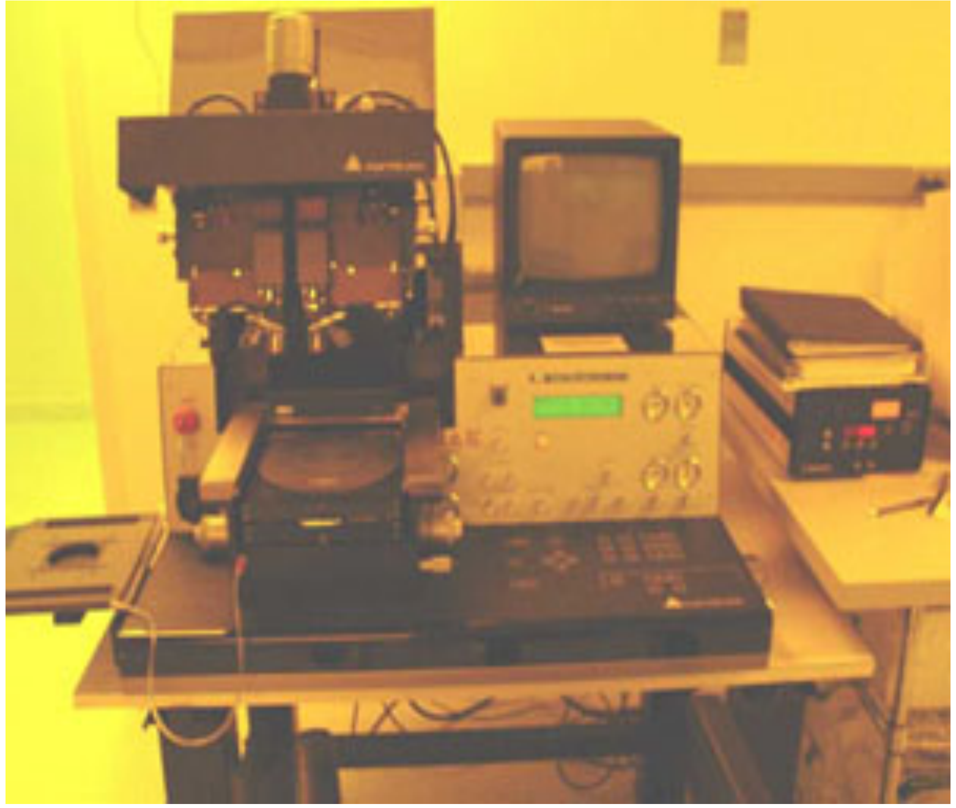
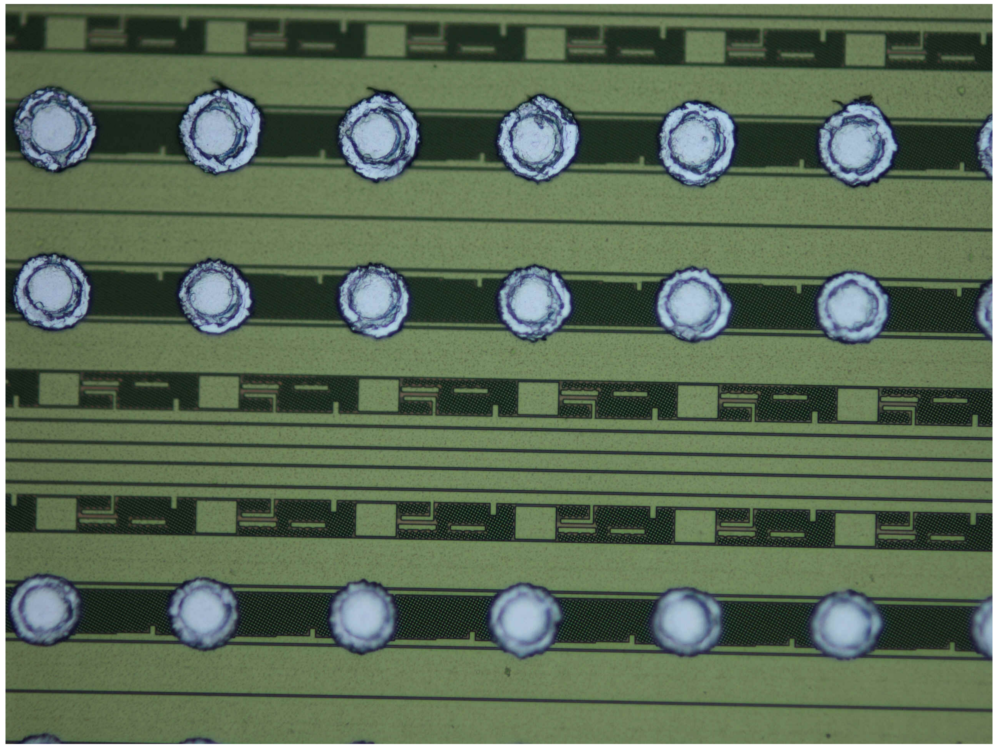
Bumps on the ROC

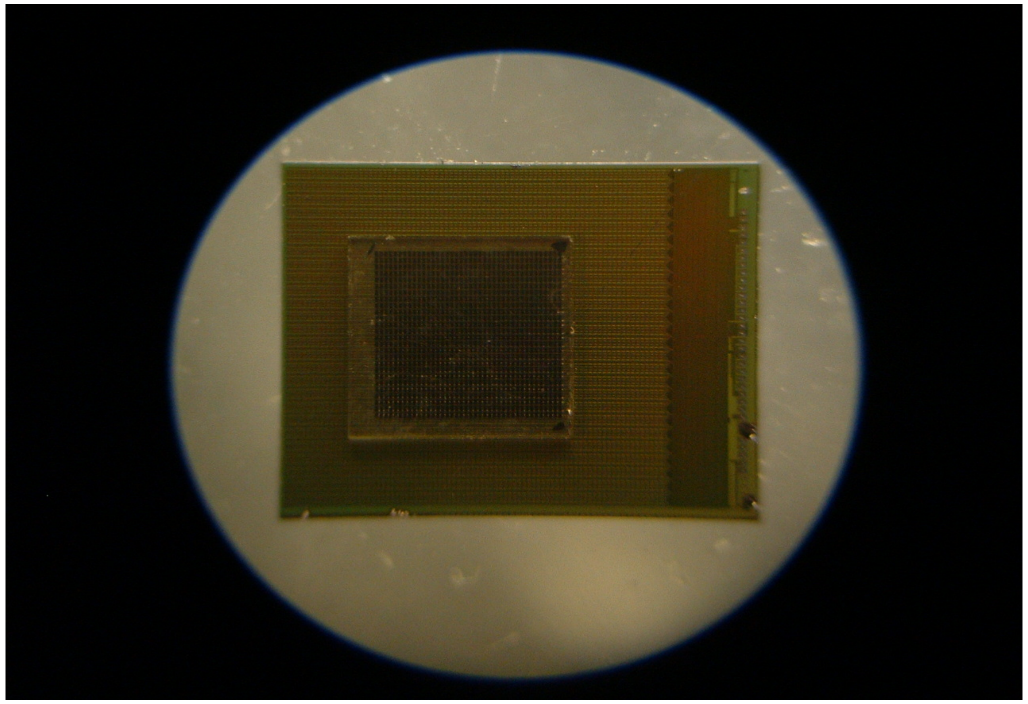
- **The details of the process are the same as for the diamond, except:**
  - ➡ **Process the quarter wafer instead of a single chip, hence do not use frame.**
    - **Alignment is easier if sacrifice the corner chips.**
  - ➡ **Sputter TiW right before Indium.**
    - **Use the same pattern**
    - **No annealing step before Indium.**
  - ➡ **Dice out the chips after the bumps are on.**

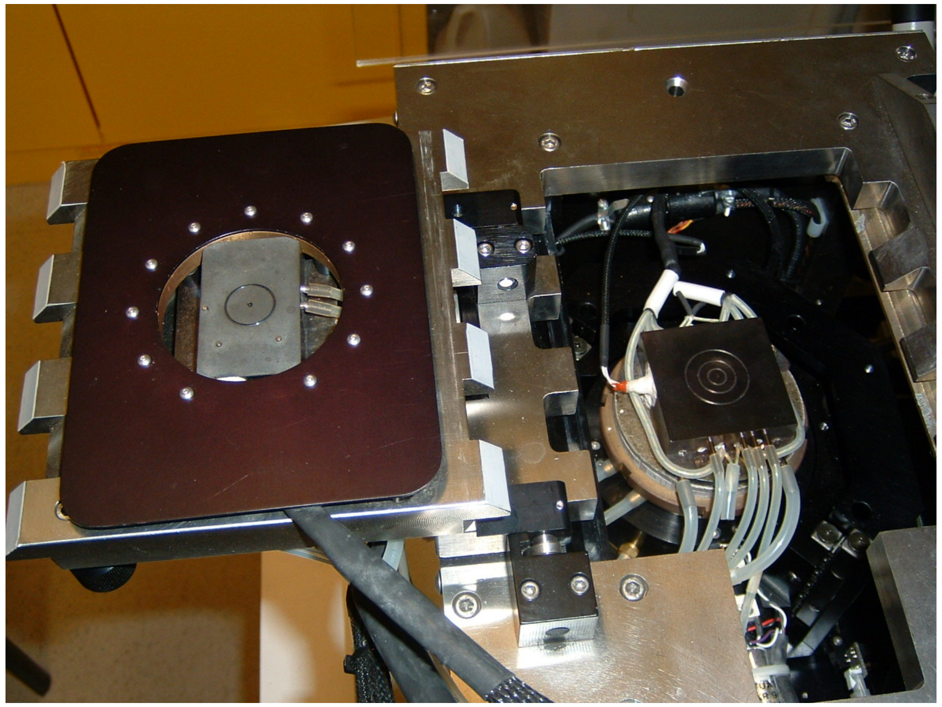


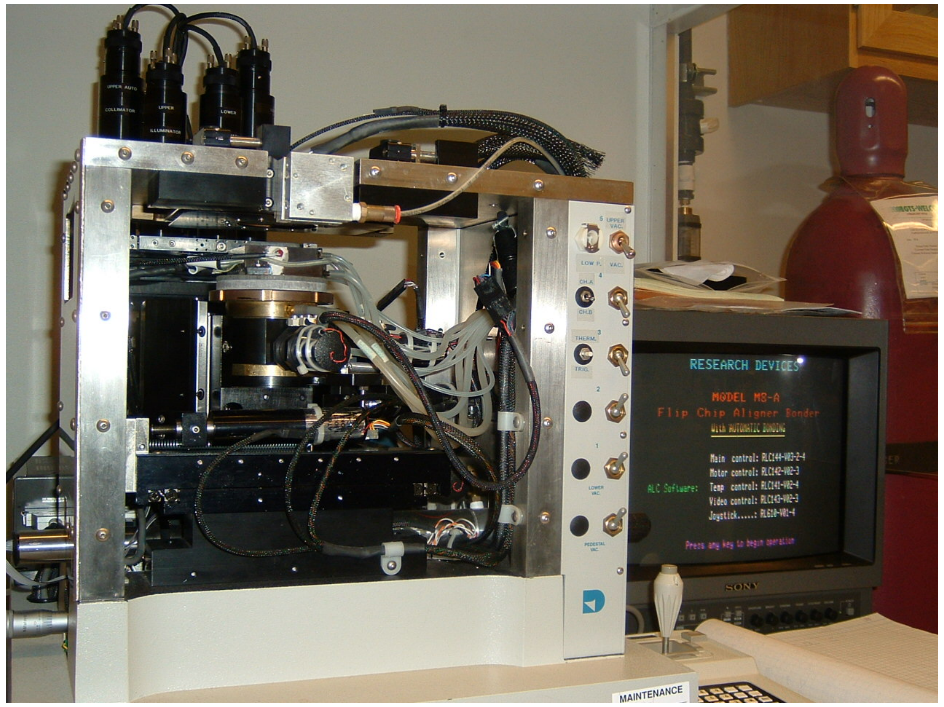


Bump-bonding

- Calibrate using glass die achieving better than 2um accuracy.
- Load diamond and ROC.
- Load bonding profile into the bonder (5Kg @ 30ºC).
- Align the respective contact bumps (X, Y, Z, Roll, & Pitch) of Diamond and ROC
- Run bond profile







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Tests

- Pull test.
  - ➡ recent result: destruct after 175g.
- Temperature cycling test
  - ➡ use dry ice.
  - ➡ range -20°C to +25°C
- Sr^{90} individual plane tests
  - ➡ pulse heights
  - ➡ efficiencies
  - ➡ occupancies

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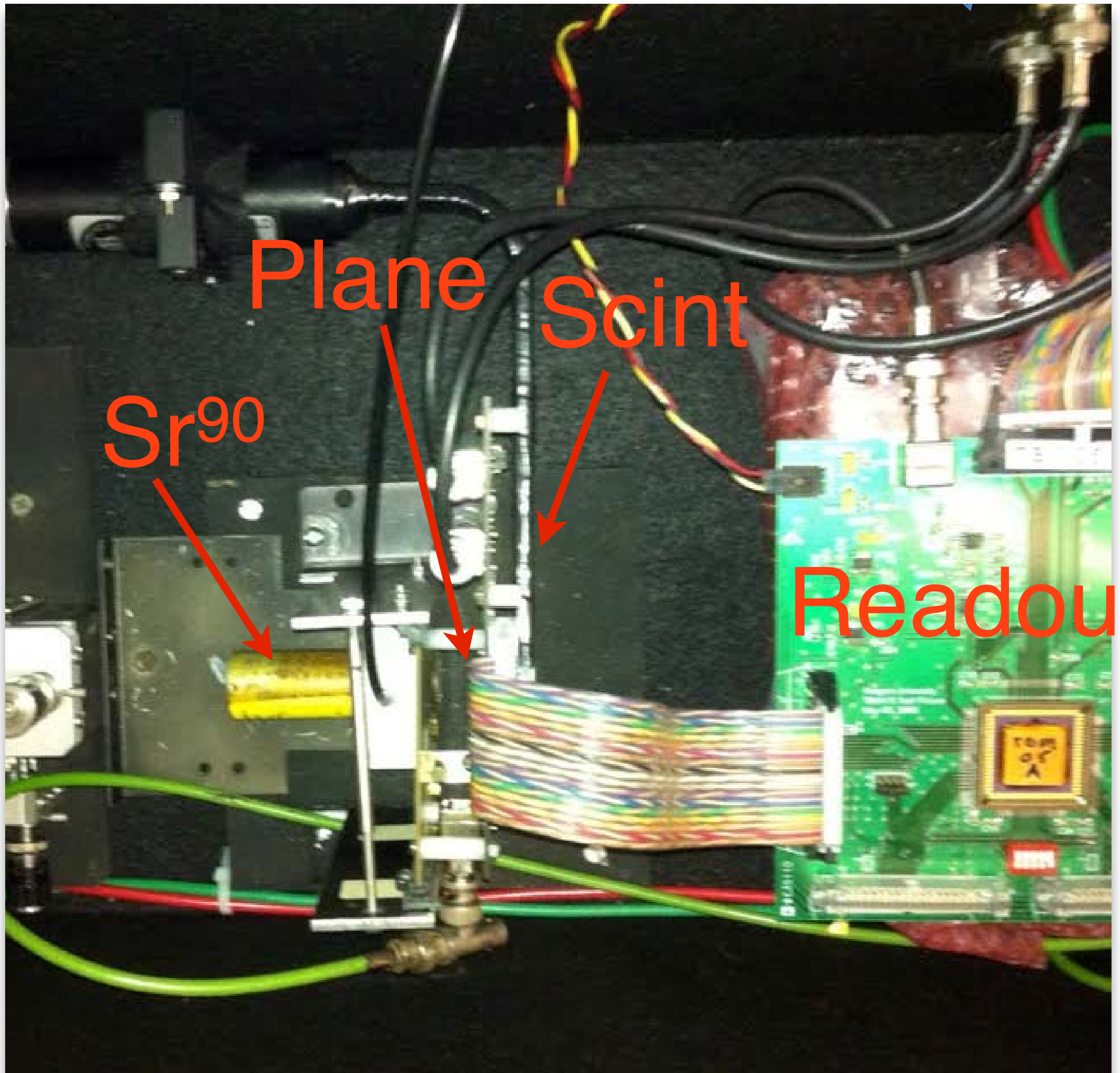
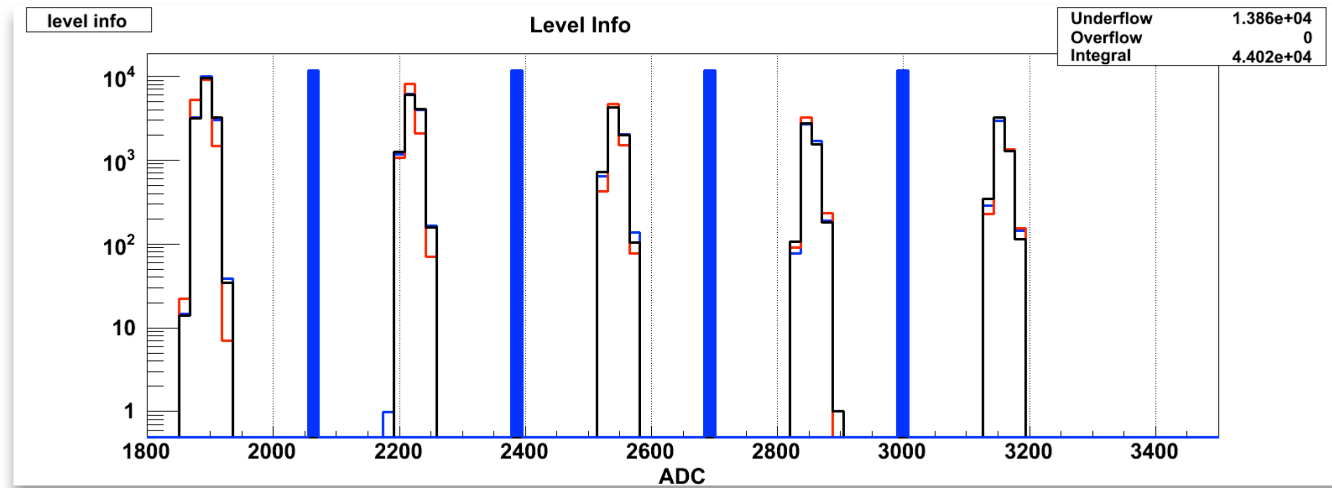
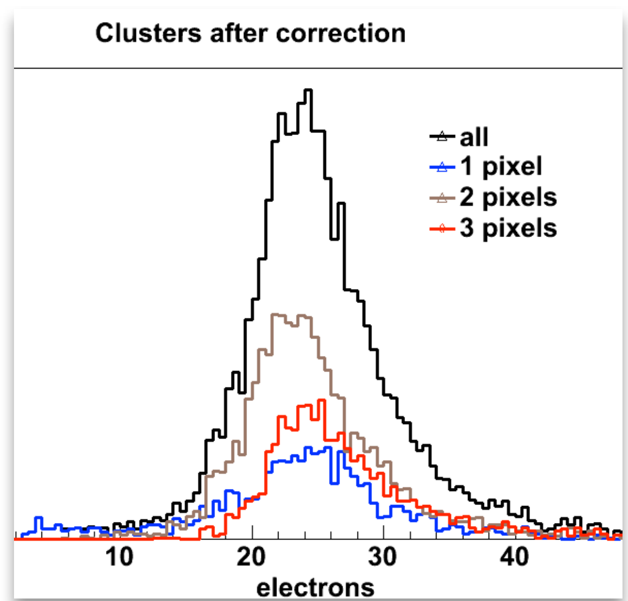
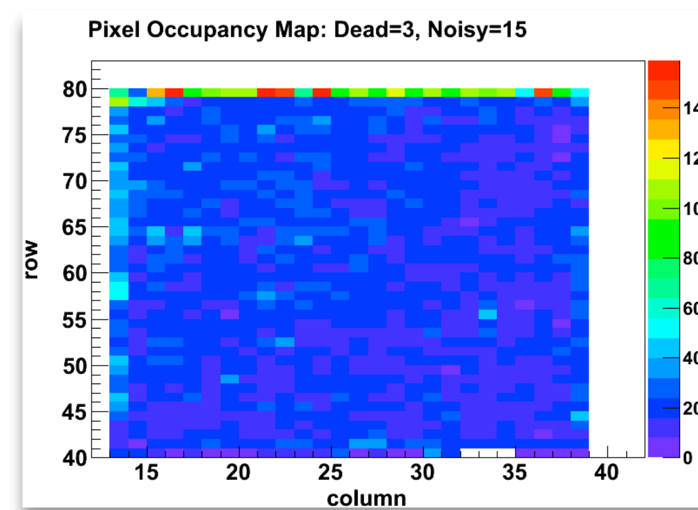
Sr^{90} plane testing setup









- Test individual planes after production.
- Similar setup is under construction at CERN.

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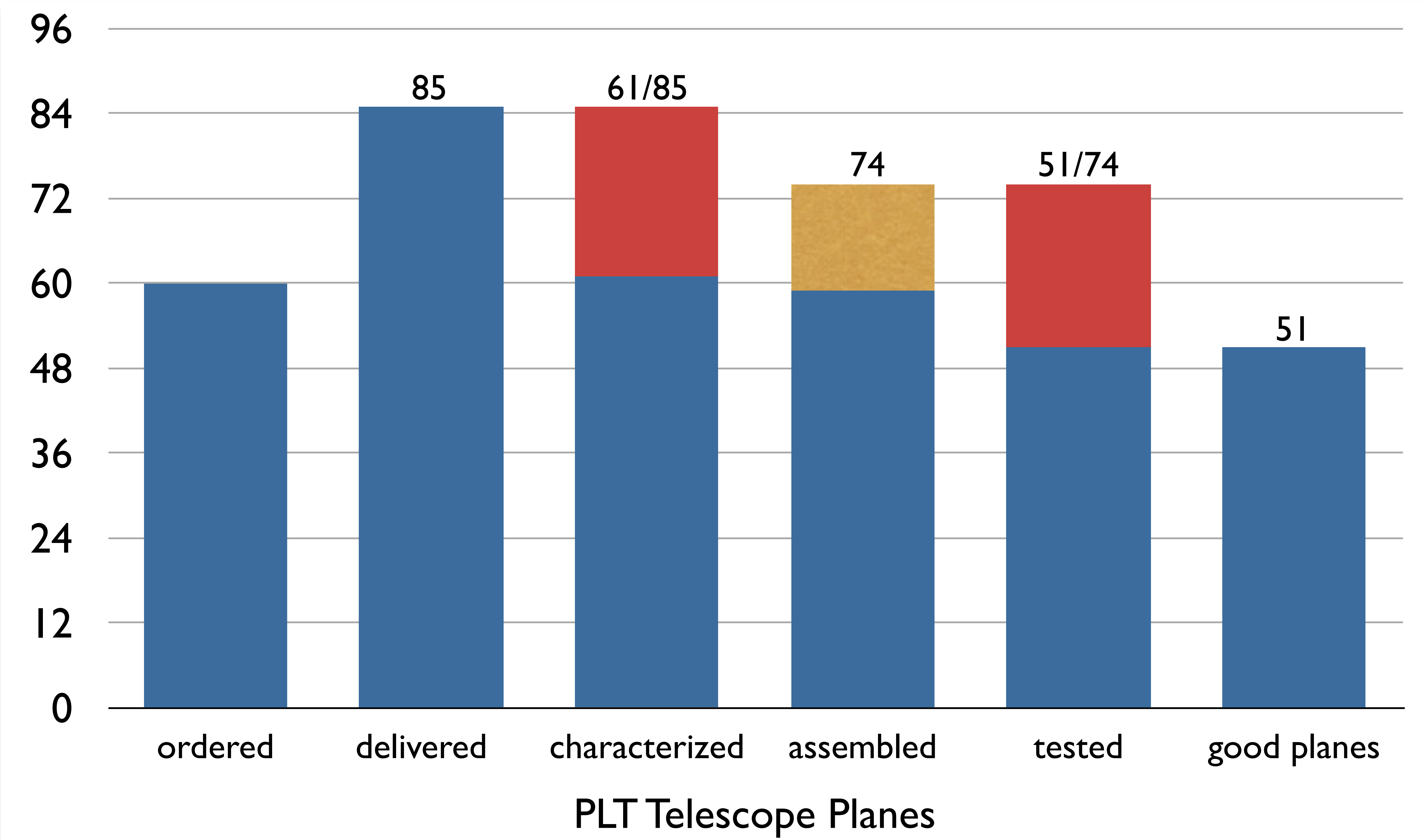
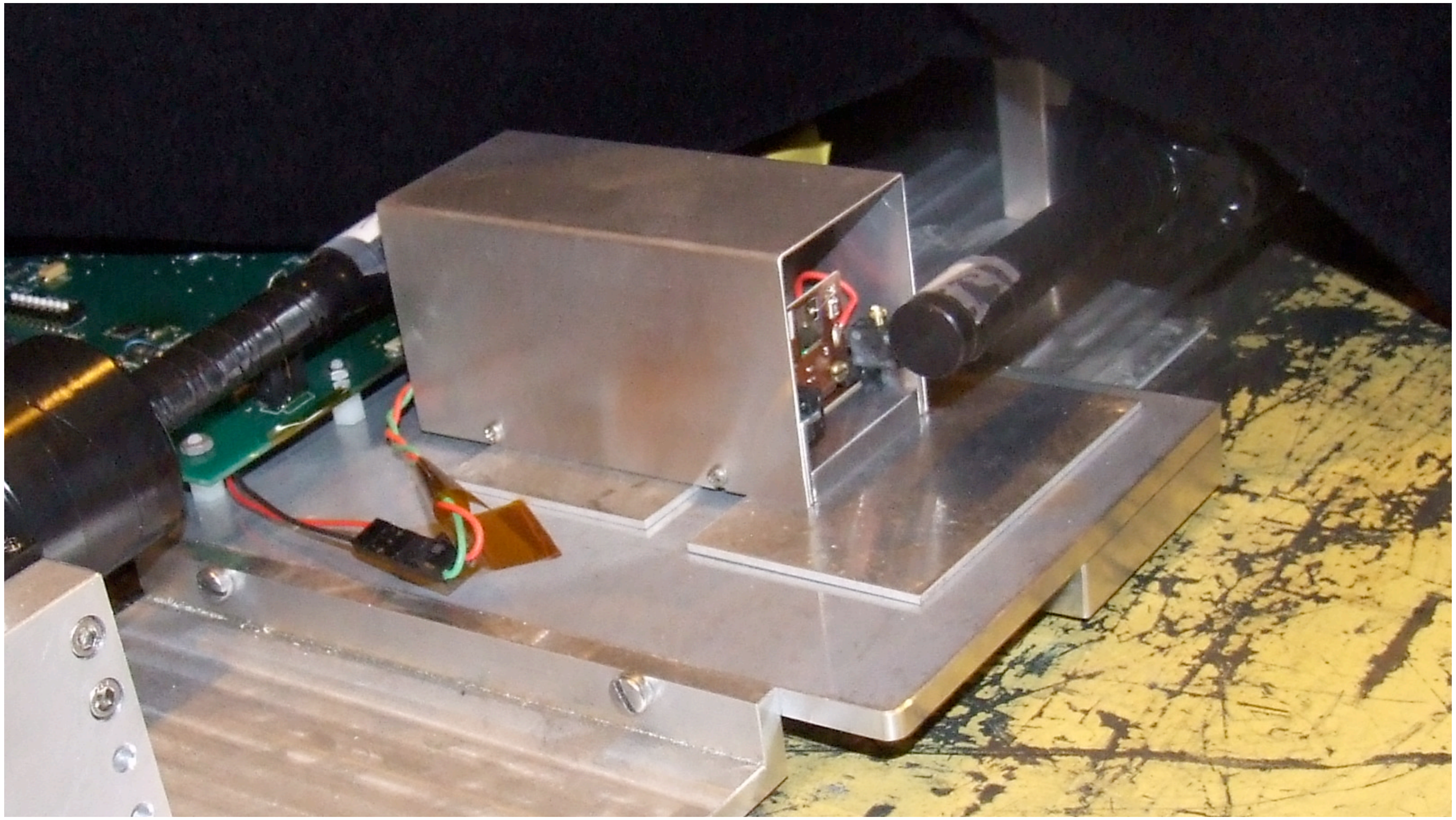
Status of PLT plane production



Test Beams

Test beam at SPS

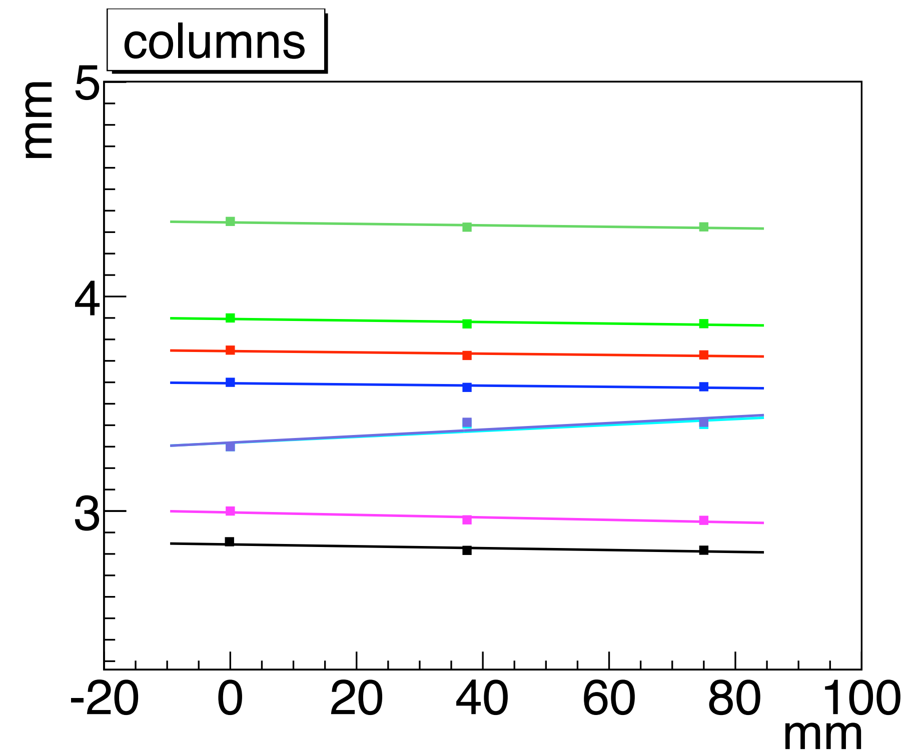
150 GeV/c π^+ H4 beam line at CERN SPS

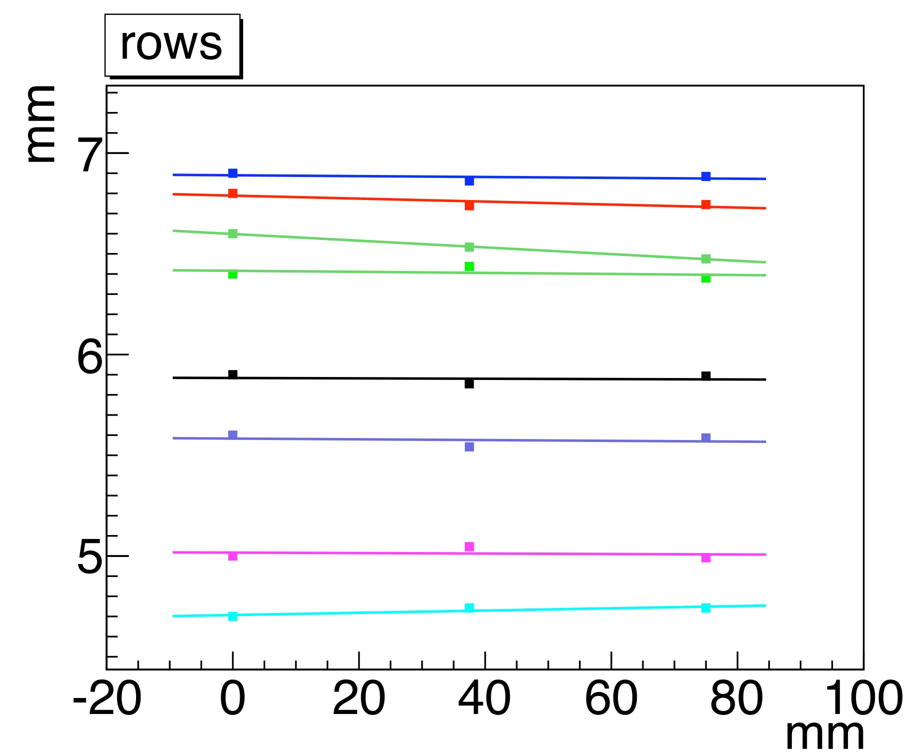


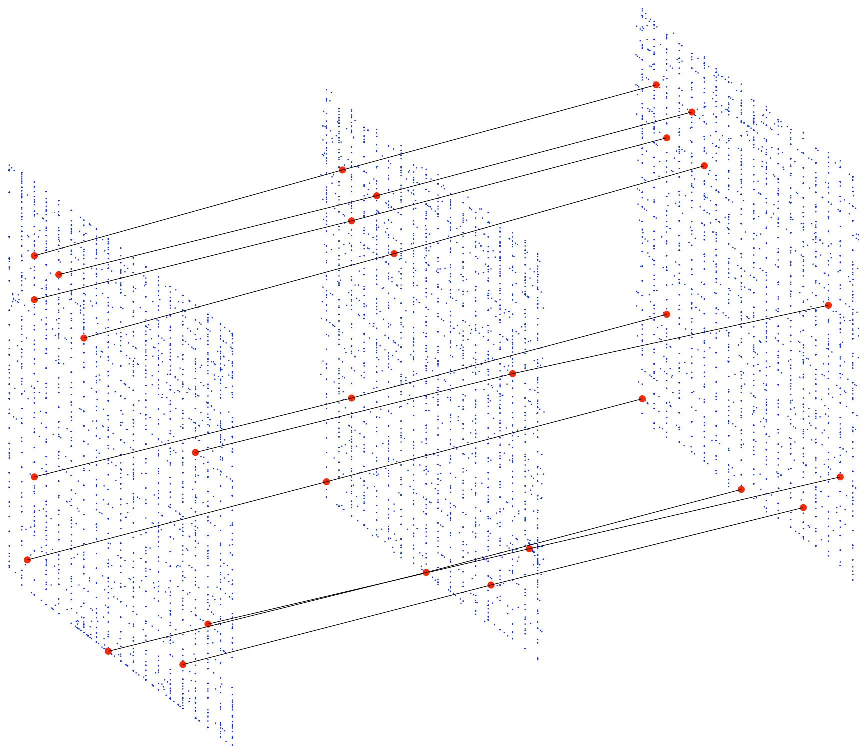
- Single telescope
- Electrical readout

Tracking

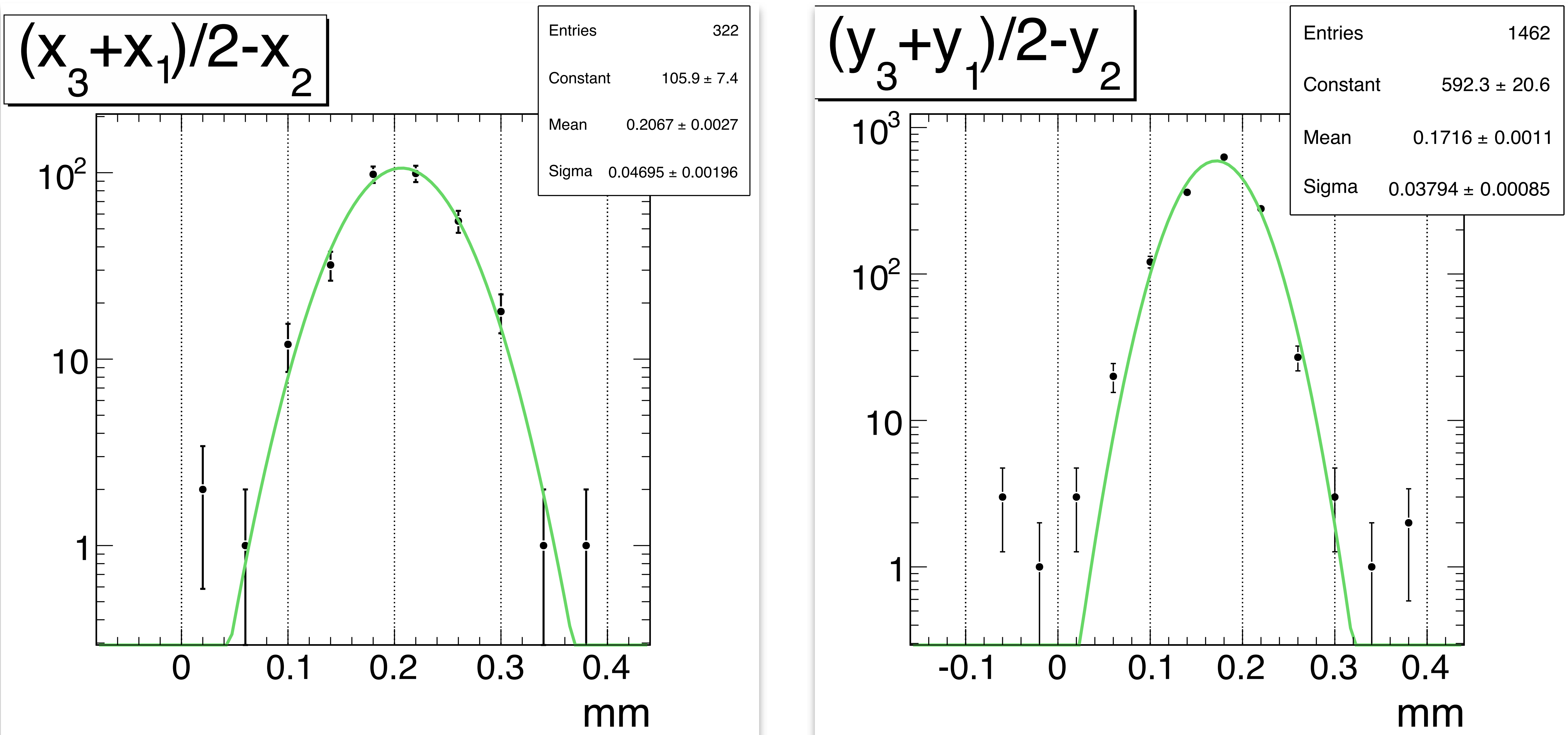
- Define cluster: group of neighboring “hit” pixels
- Define cluster position: center of gravity
- Correct for relative plane rotation
- Correct for relative plane offset
- Select events with one and only one cluster in each plane (89% of events with hits in all three planes)







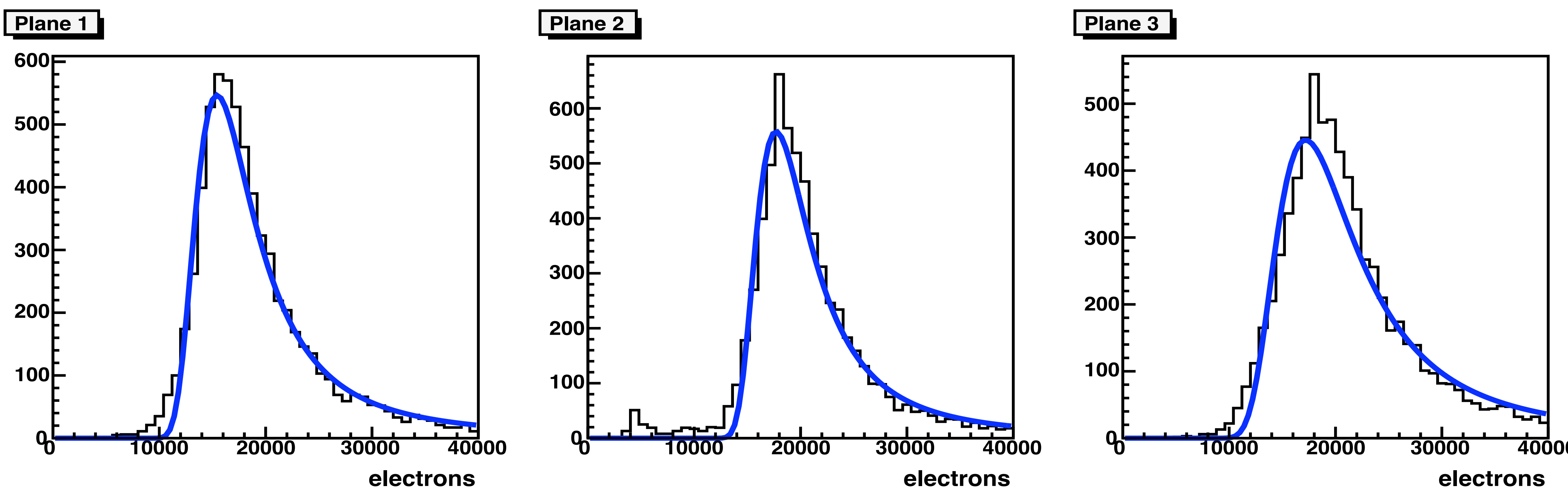
Residuals



- Only clusters with 2 pixels in the direction of the residual.
- Events with one cluster per plane.
- No eta correction, just center of gravity
    - sigma < pixel pitch

Pulse heights from MIPs

- Require single cluster in all three planes
- For Plane c, require hit in regions of Planes a and b such that track is certain to pass through fiducial region of Plane c
- Plot pulse height summed over cluster

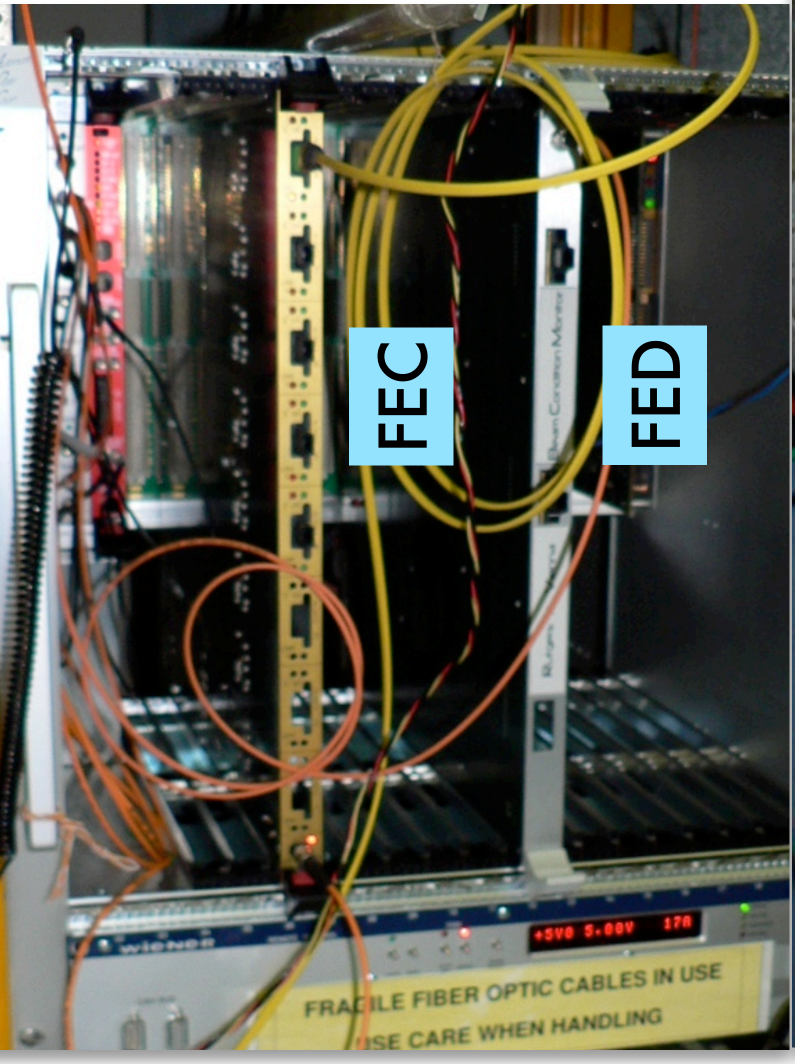


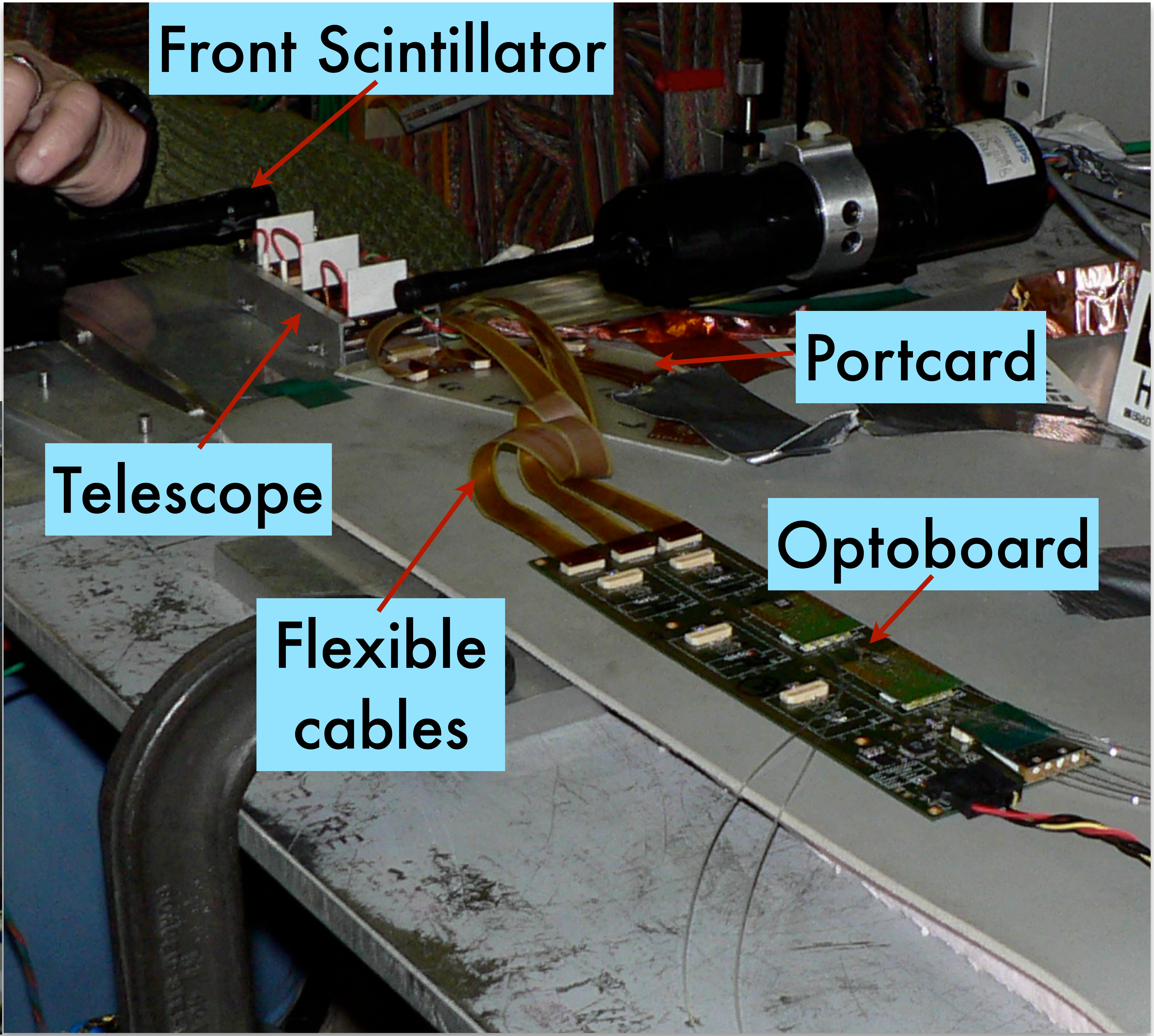
Most probable pulse heights:

Plane 1: 16,000e⁻ Plane 2: 18,500e⁻ Plane 3: 18,500e⁻

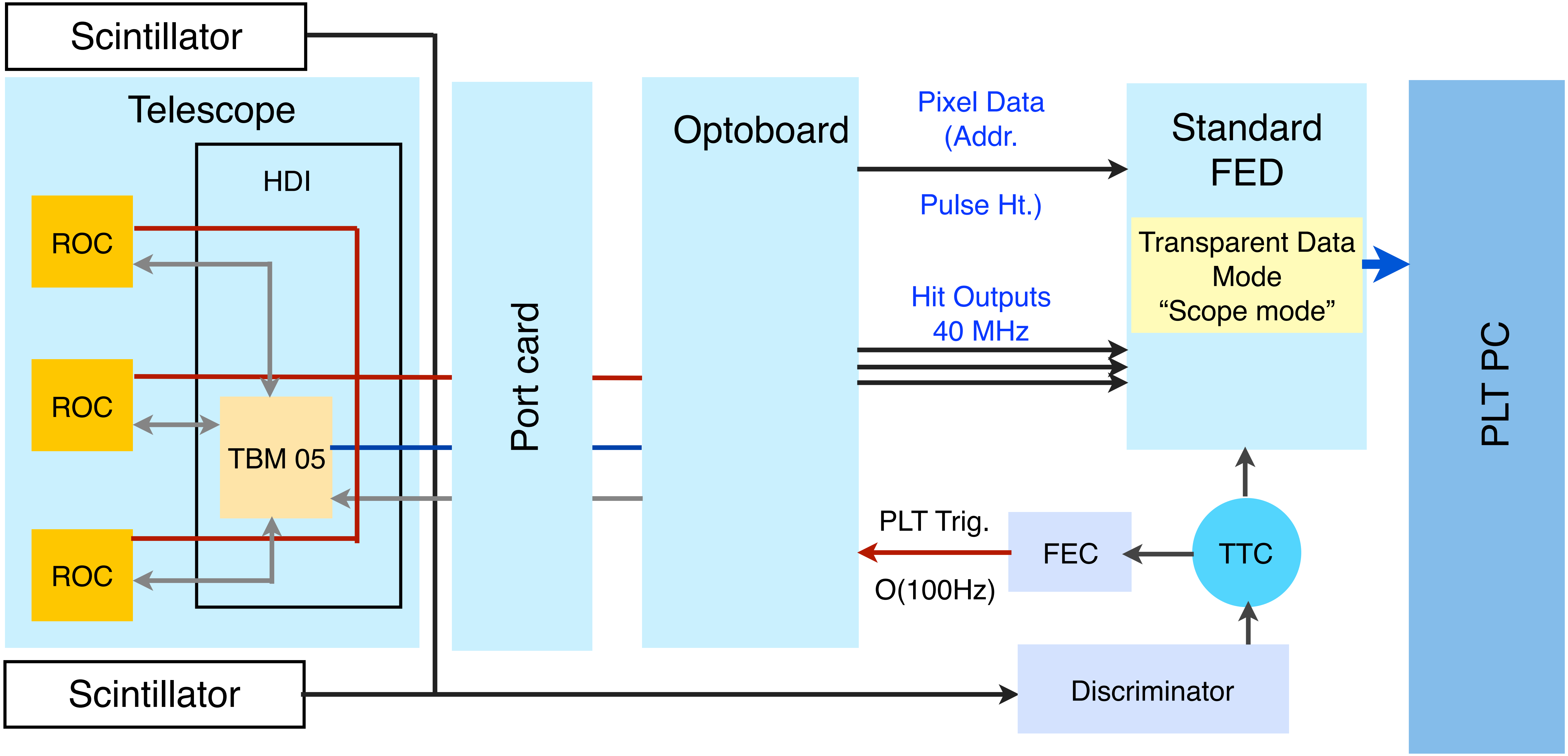
Test beam at Fermilab

- First test of optical readout.
- Testing the very first versions of opto-board, port-card, flexible interconnect cables.



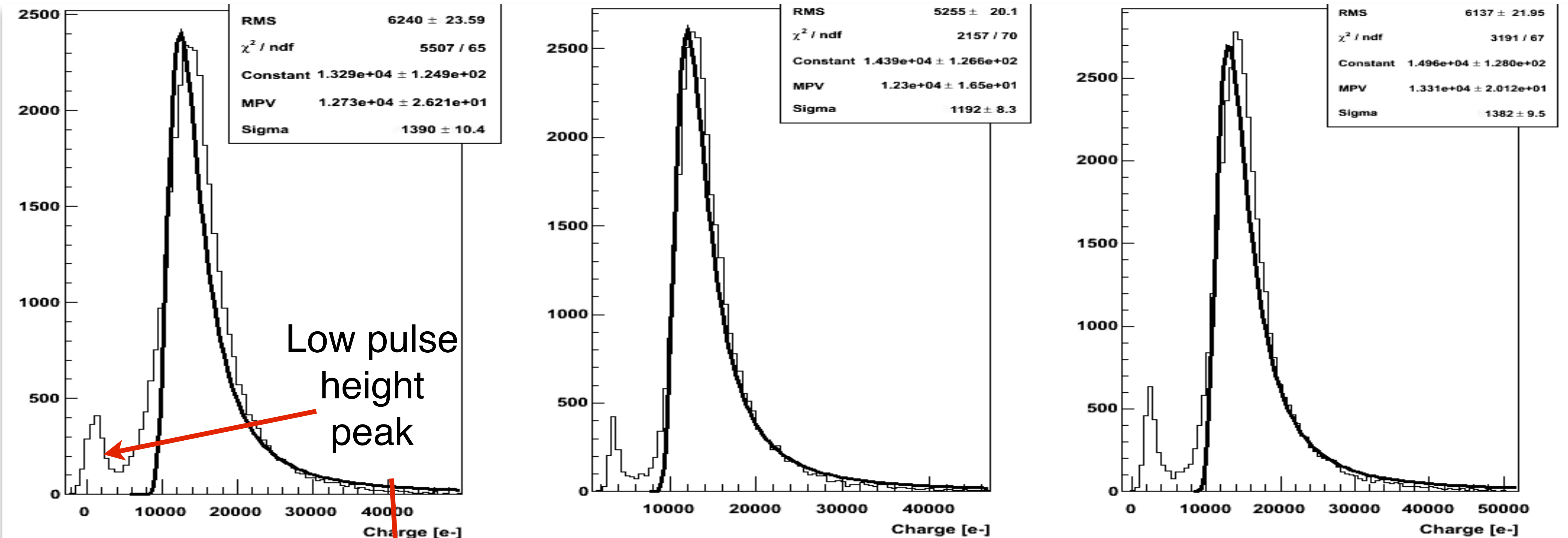


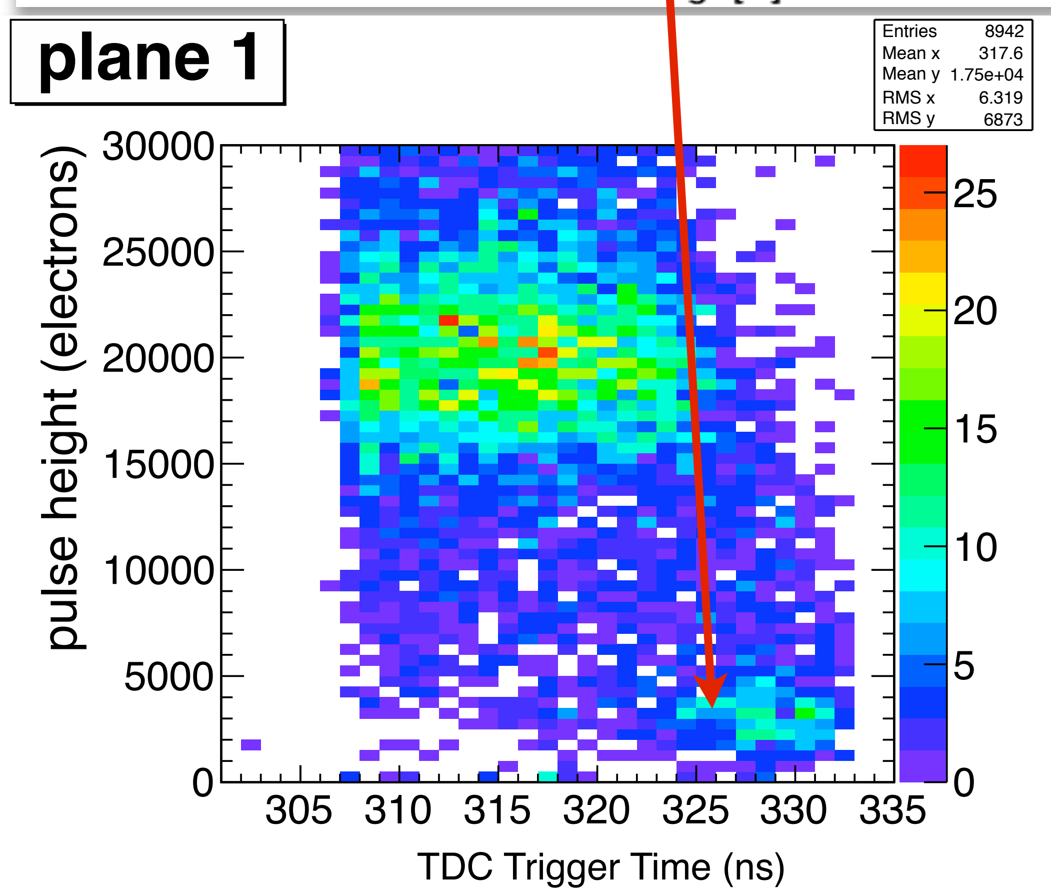
Readout diagram (Fermilab)



- Main objective of the test beam was to validate the Optical Readout Scheme.

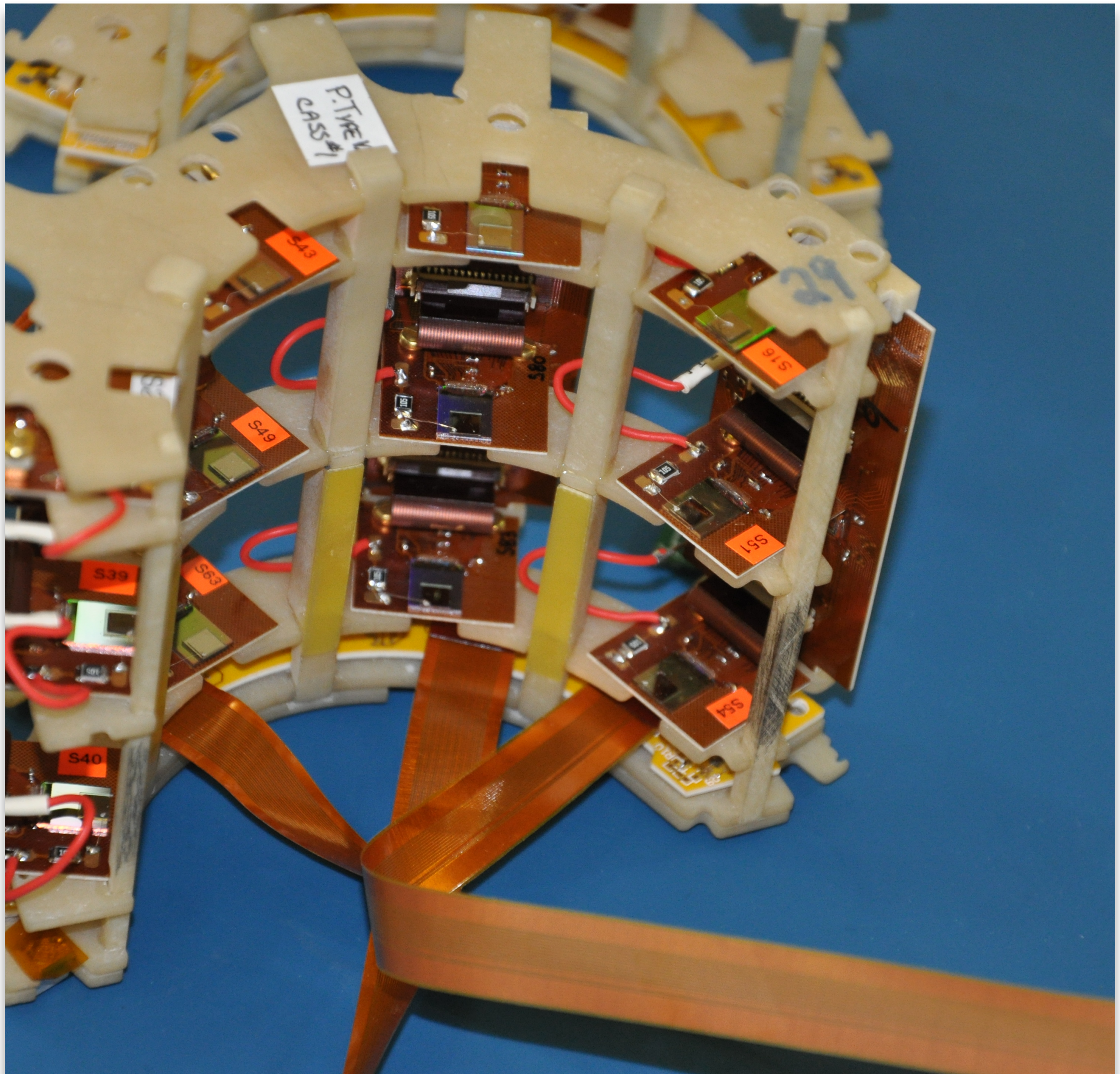
Pulse heights

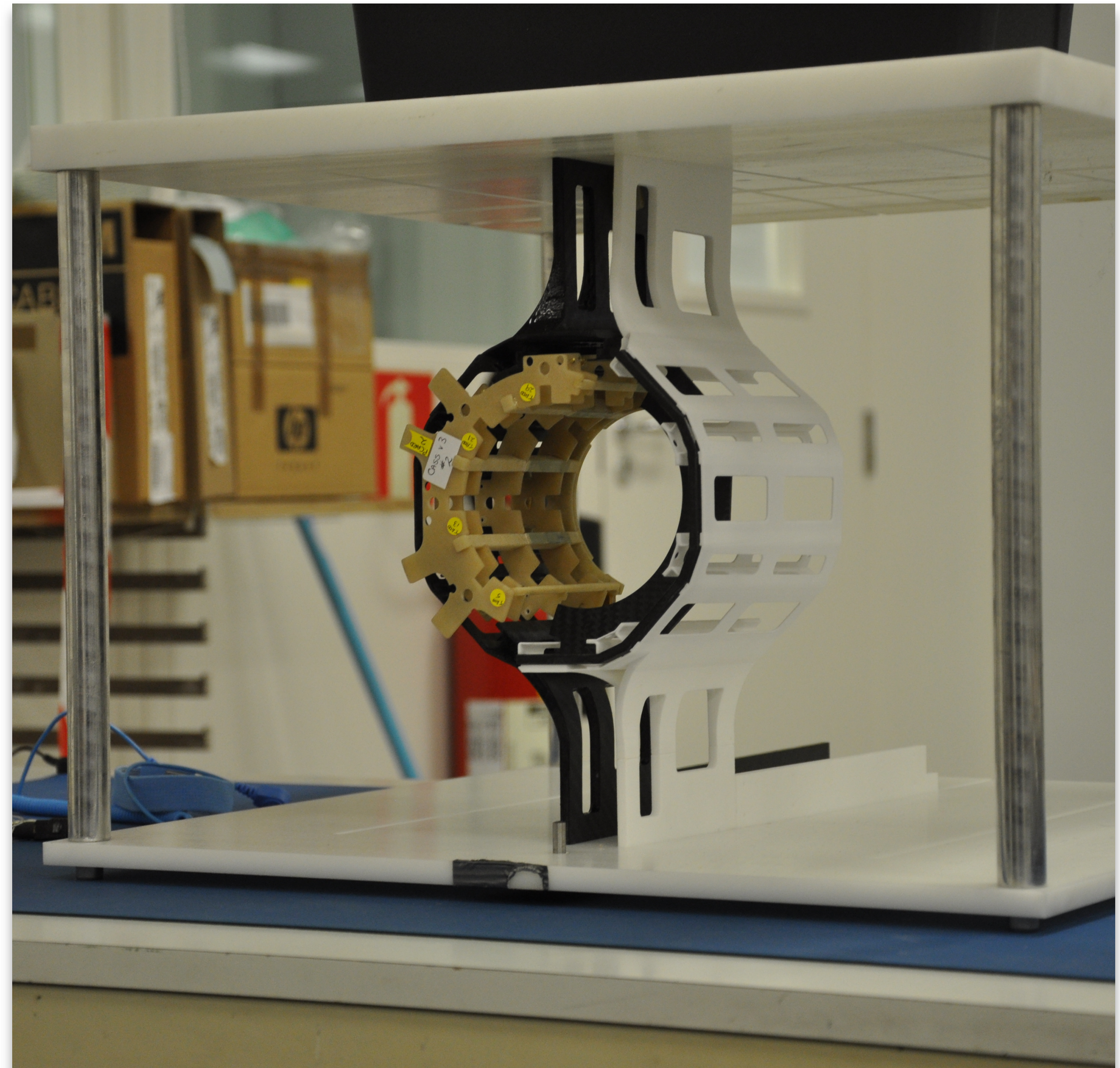




- Events with one cluster only (no limit on number of hits in clusters though).
- Lower peak is due to out of time triggers.

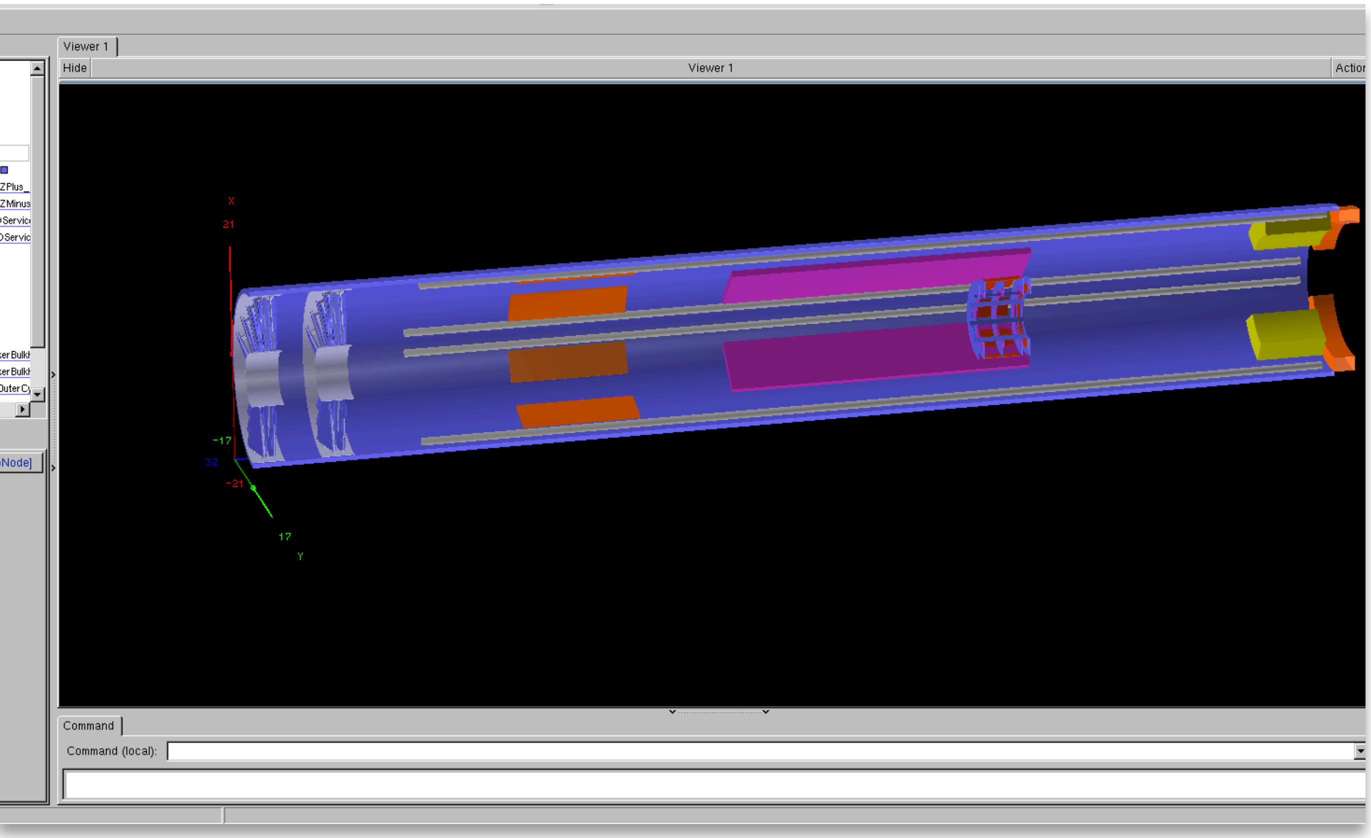
Next October 2011 Test Beam at PS

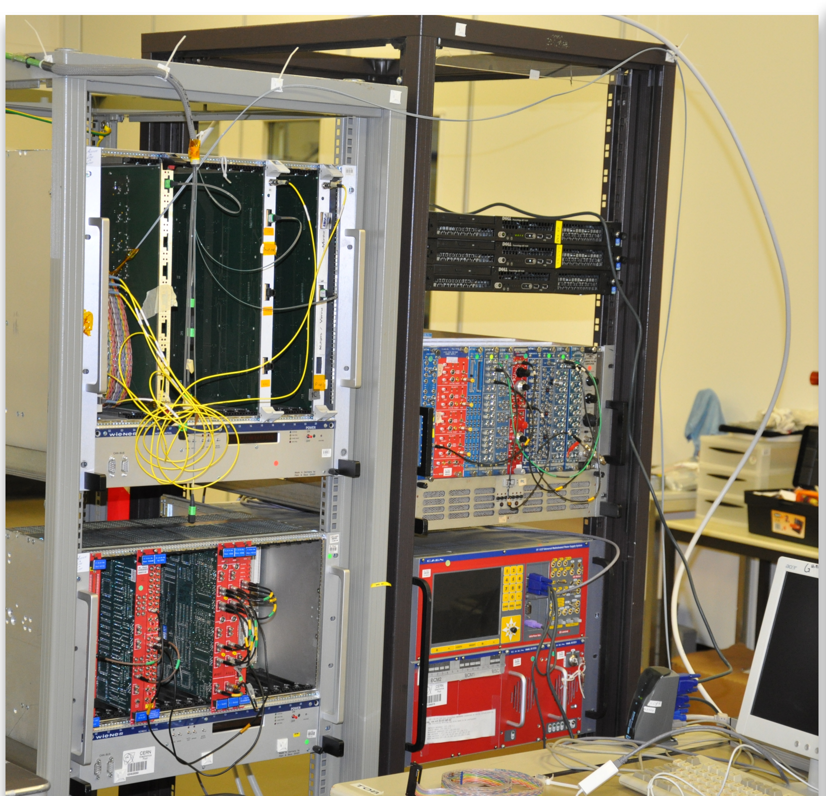


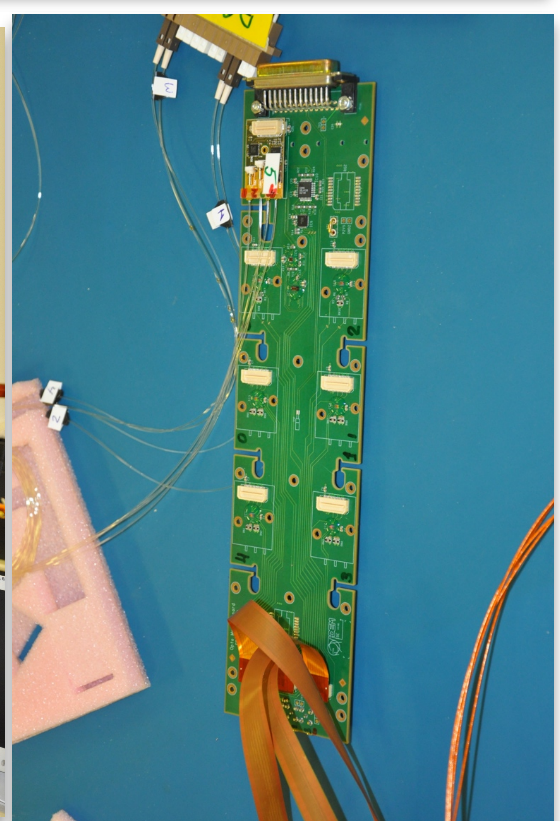


- 2 full cassette (1/2 of the PLT) test
- Latest version of the readout components

Current Work







- Incorporating PLT geometry into CMSSW
  - ➡ Full detector simulation with GEANT
- Testing PLT setup in TIF
  - ➡ New opto-board
  - ➡ powering and grounding schemas
- Testing new PLT software
  - ➡ calibration
  - ➡ trimming
  - ➡ readout
  - ➡ diagnostic
- Creating and maintaining PLT documentation.
  - ➡ https://twiki.cern.ch/twiki/bin/view/CMS/BrmPlt

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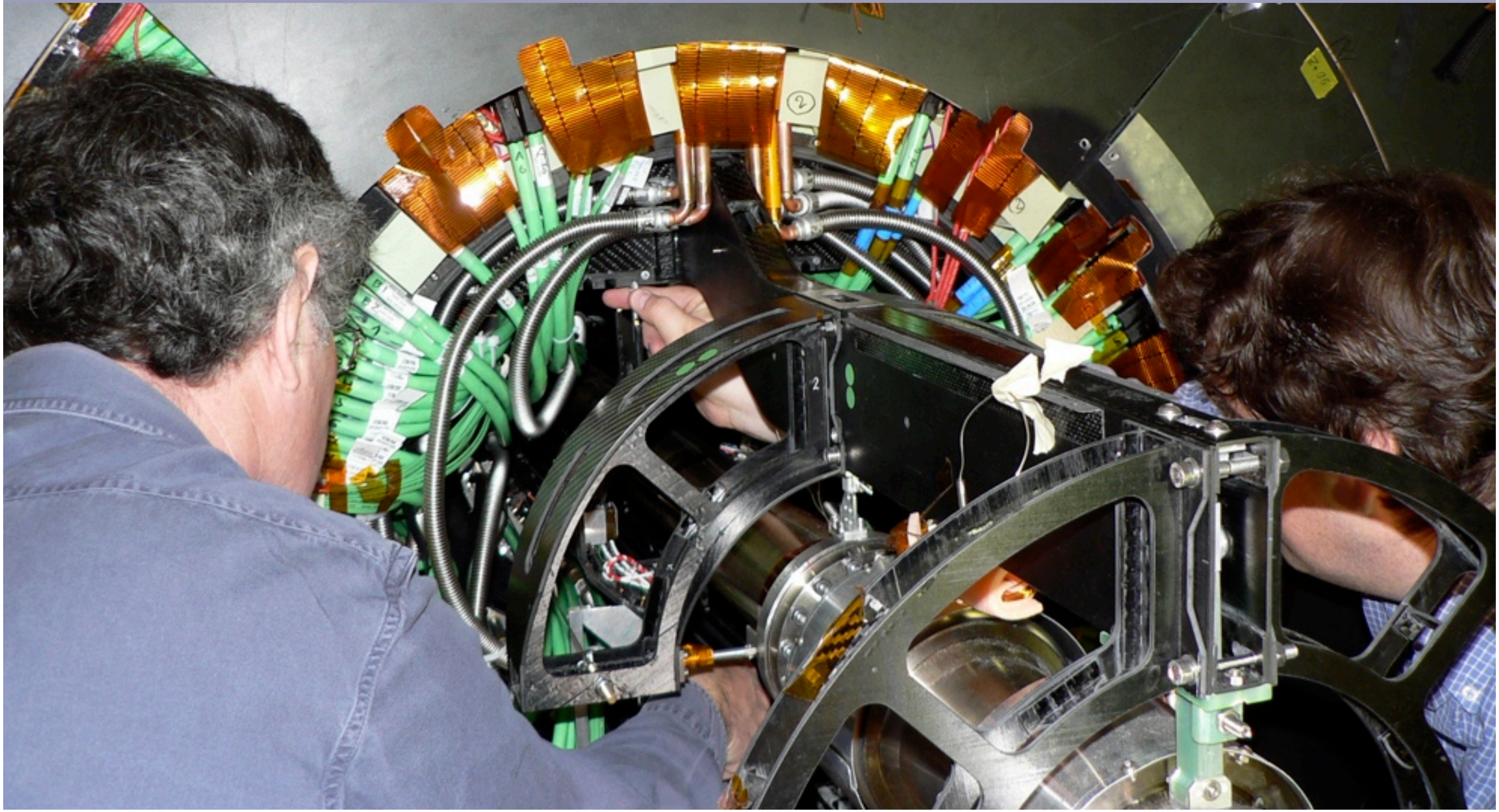
Summary

- PLT -single crystal pixelated diamond detector dedicated for measuring luminosity in CMS
- My main contribution was development of the bump-bonding process.
- In addition I have contributed to organizing test beam experiments and analyzing test beam data.
- Currently I am involved in overall testing of the final PLT system at CERN and developing the simulations of the PLT.
- We are preparing for complete system test of the 1/2 of the PLT with the latest readout components.

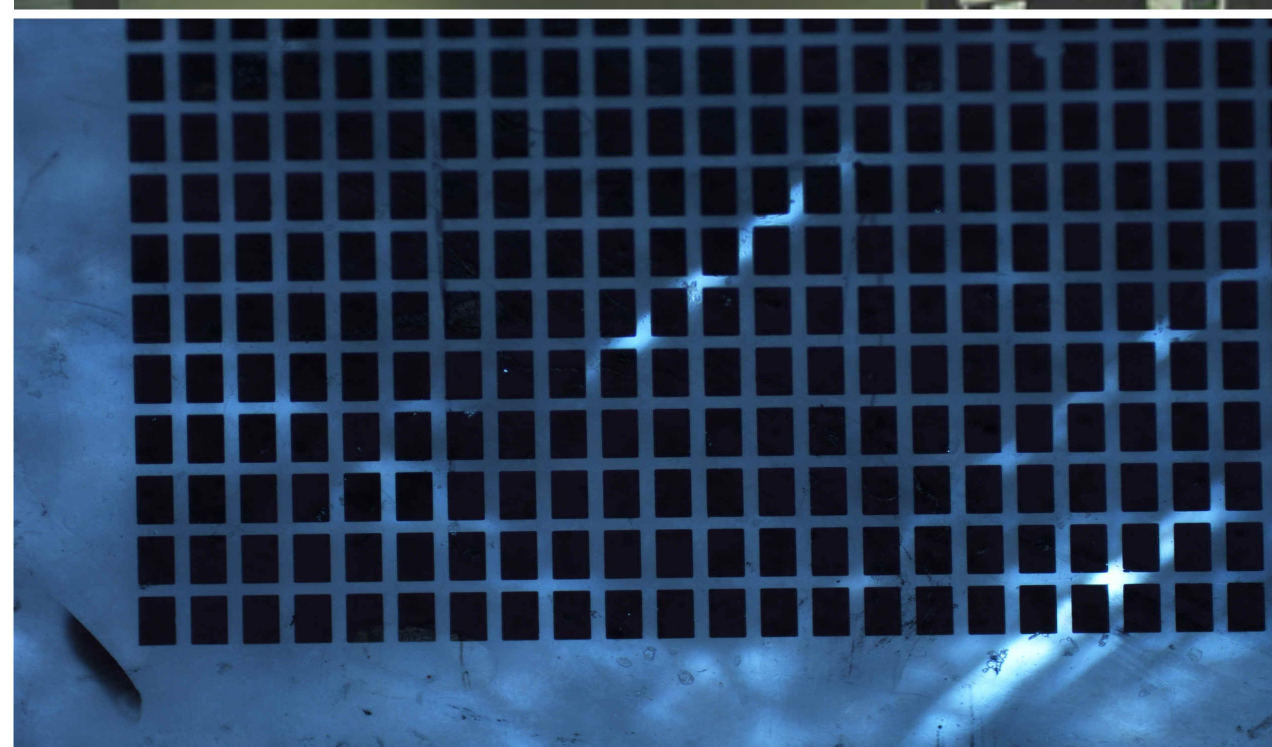
On course for PLT installation
during 2012-2013 shutdown
a quarter of the PLT will be installed on the castor table during 2011-2012 shutdown



BackUp slides

Ti/W metallization

- **Pattern diamond (Photolithography)**
  - Clean and Moisture Bake (110 ºC for 10 Minutes)
  - Spin on HMDS (4000RPM 40 sec)
  - Spin on resist (AZ-5214) 4000RPM for 40 sec)
  - Soft-Bake (on hotplate) 90ºC for 60 sec
  - Pattern Expose using the MA-6 (2.0mW/Cm) for 90 sec
  - Develop in 1:1 with DI:AZ312MIF for 60 sec
  - Inspect.
  - Post Exposure Bake (on hotplate) 110ºC for 60 sec
  - Plasma de-scum.
- **Sputter TiW - Angstrom Engineering Metal Sputterer**
  - Load diamond into shadow mask holder.
  - Sputter ~150Å of TiW onto diamond
- **Liftoff**
  - Acetone Soak overnight.
  - Ultrasound 5 second.
  - Rinse with clean acetone then Isopropanol.
  - Blow dry with N_2.
- **Anneal at 400C in O2 atmosphere.**



Indium bump process (details)

- Clean and Moisture Bake (110 °C for 10 Minutes)
- Spin on HMDS (4000RPM 40 sec)
- 1st Layer (6-7um)
  - Spin resist (spr-220) @ 250RPM for 15sec then 1200RPM for 40sec
  - Soft-Bake (on hotplate) Ramp 60ºC to 100ºC (Hold @ 100ºC for 2 min)
  - Flood Expose on MA-6 (2.0mW/cm2) for 400s
  - Hold for resist setup overnight (24hrs)
  - Post Exposure Bake (on hotplate) ramp: 20ºC to 90ºC @ 180ºC/hr, hold @ 90ºC for 2 min)
- 2nd Layer(6-7um)
  - Spin resist (spr-220) @ 250RPM for 15sec then 1200RPM for 40sec
  - Soft-Bake (on hotplate) Ramp 60ºC to 100ºC (Hold @ 100ºC for 2 min)
  - Pattern Expose on MA-6 (2.0mW/cm2) for 400s
  - Hold for resist setup overnight (24hrs)
  - Post Exposure Bake (on hotplate)
  - Ramp: 20ºC to 90ºC @ 180ºC/hr, hold @ 90ºC for 2 min)
- Develop in 1:1 with DI:AZ312MIF
  - 2.5 to 3 minutes
- Plasma de-scum
- Deposit 7-10um of Indium
  - Rate = 50Å/sec
- Thickness = 70 -100KÅ
- Liftoff
  - Acetone Soak overnight
  - **No ultrasound!**