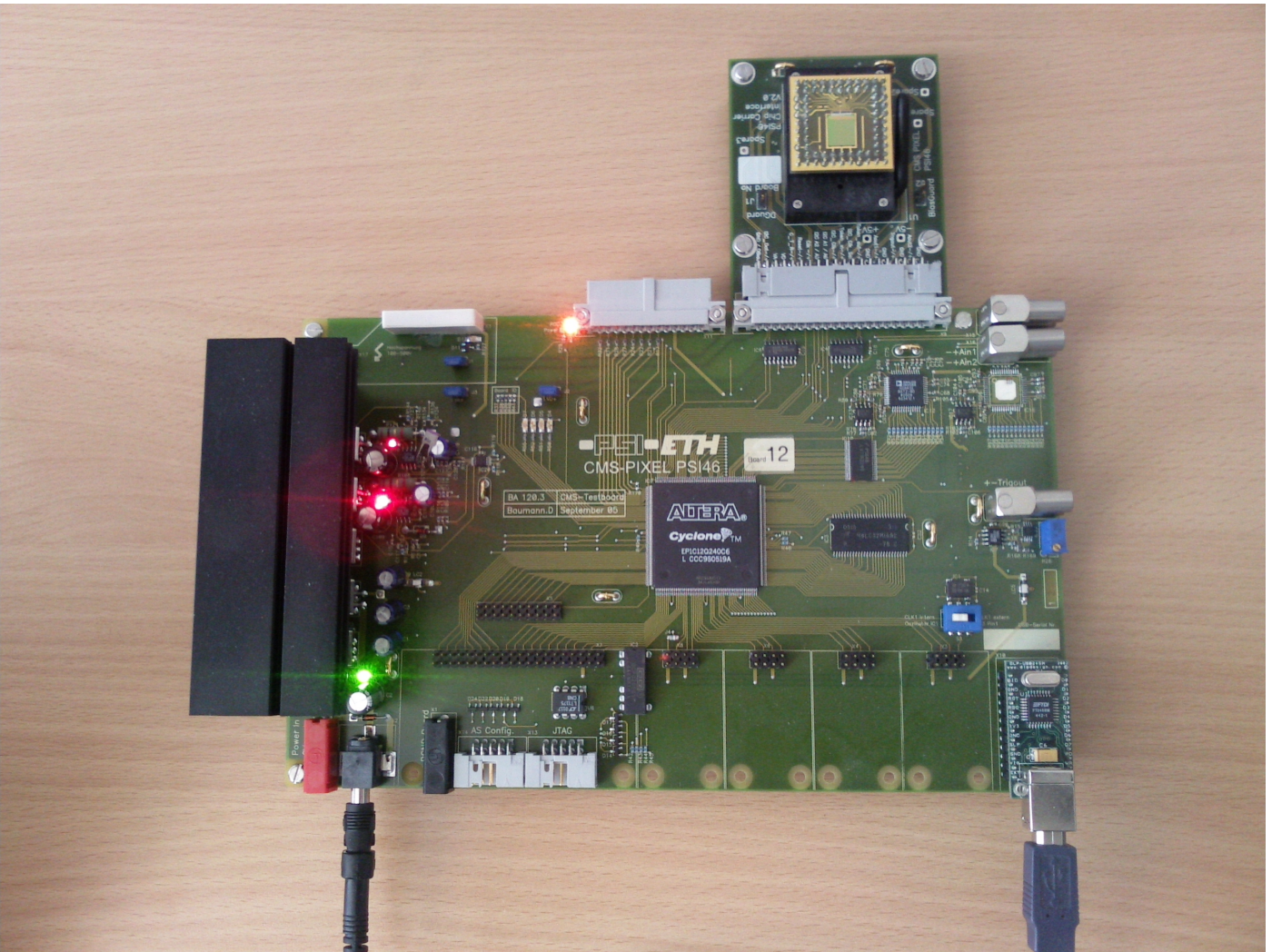
Pixel test plans

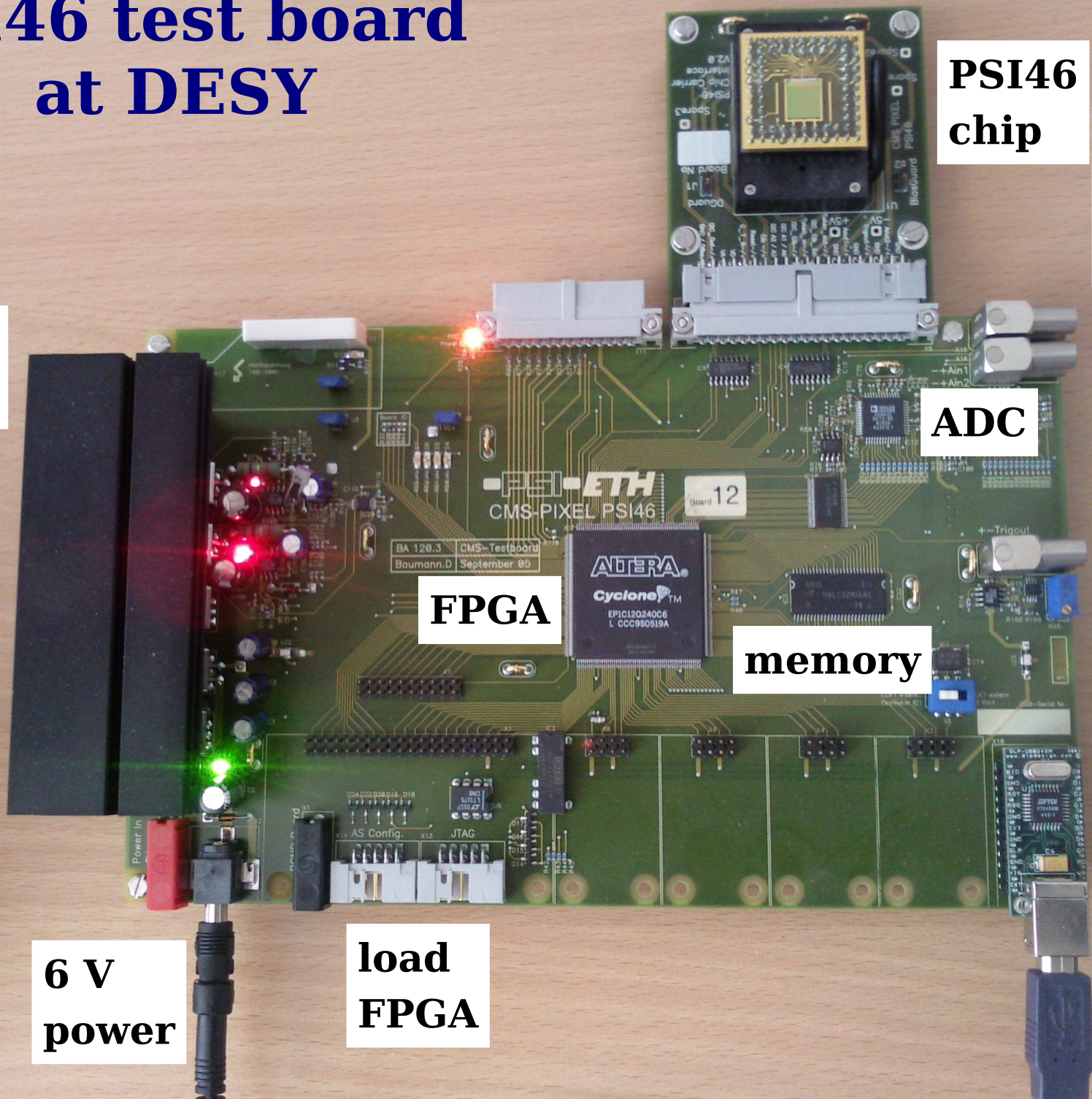
Daniel Pitzl, DESY

Pixel upgrade, 18.10.2011



- goals
- plan
- problems
- tasks
-

PSI46 test board at DESY



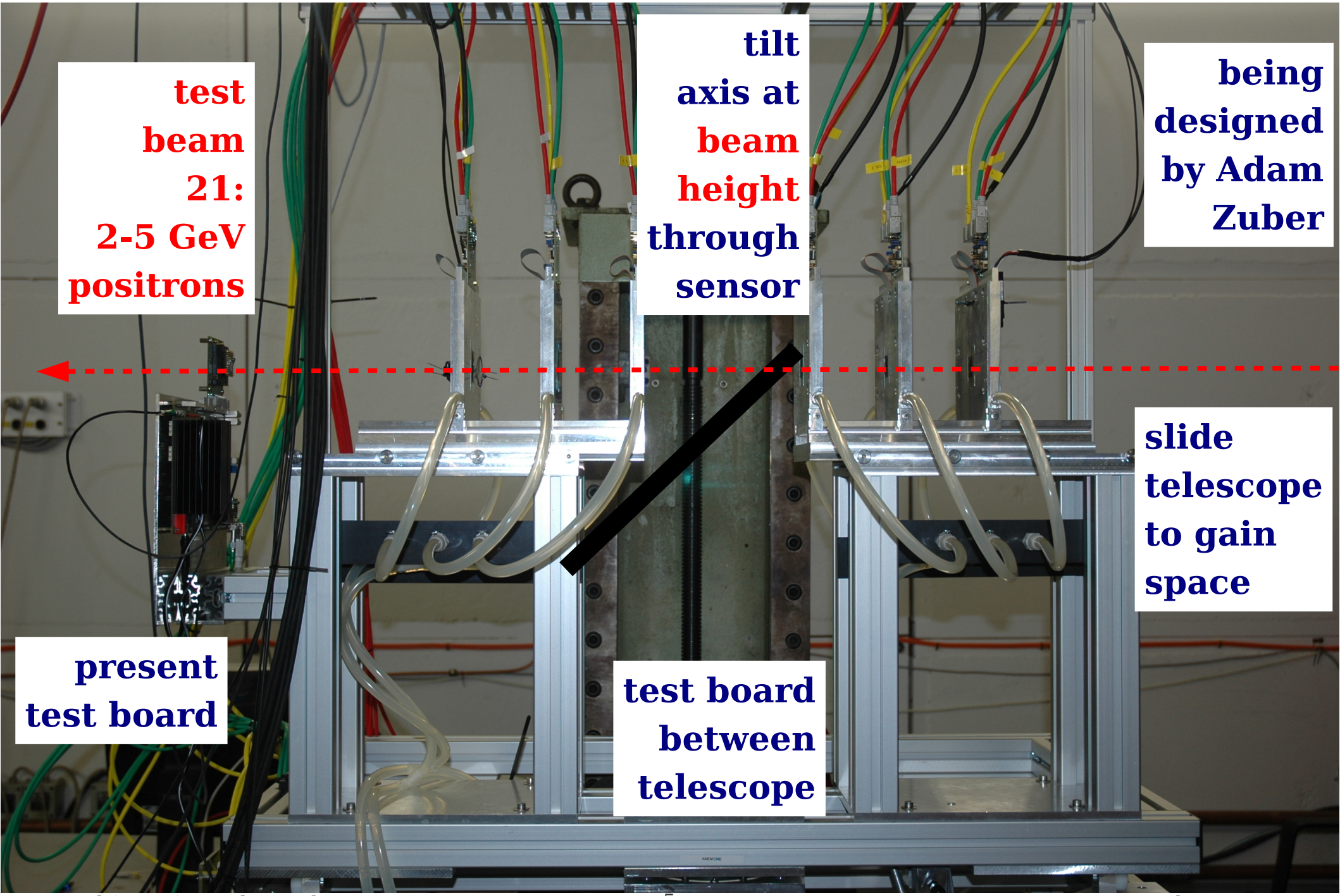
testing goals

- establish chip testing
  - determine operation parameters for new chips — well advanced
  - bare module test with probe card — to be done
- stand-alone source and test beam — established
- efficiency:
  - pixel w.r.t. to telescope — to be done
  - eff(x,y,dac) = hits / tracks — to be done
- resolution:
  - pixel residuals w.r.t. telescope tracks — to be done
- low temperature testing: — cold box being designed
- X-ray test — Uni HH

near term plan (Autumn/Winter)

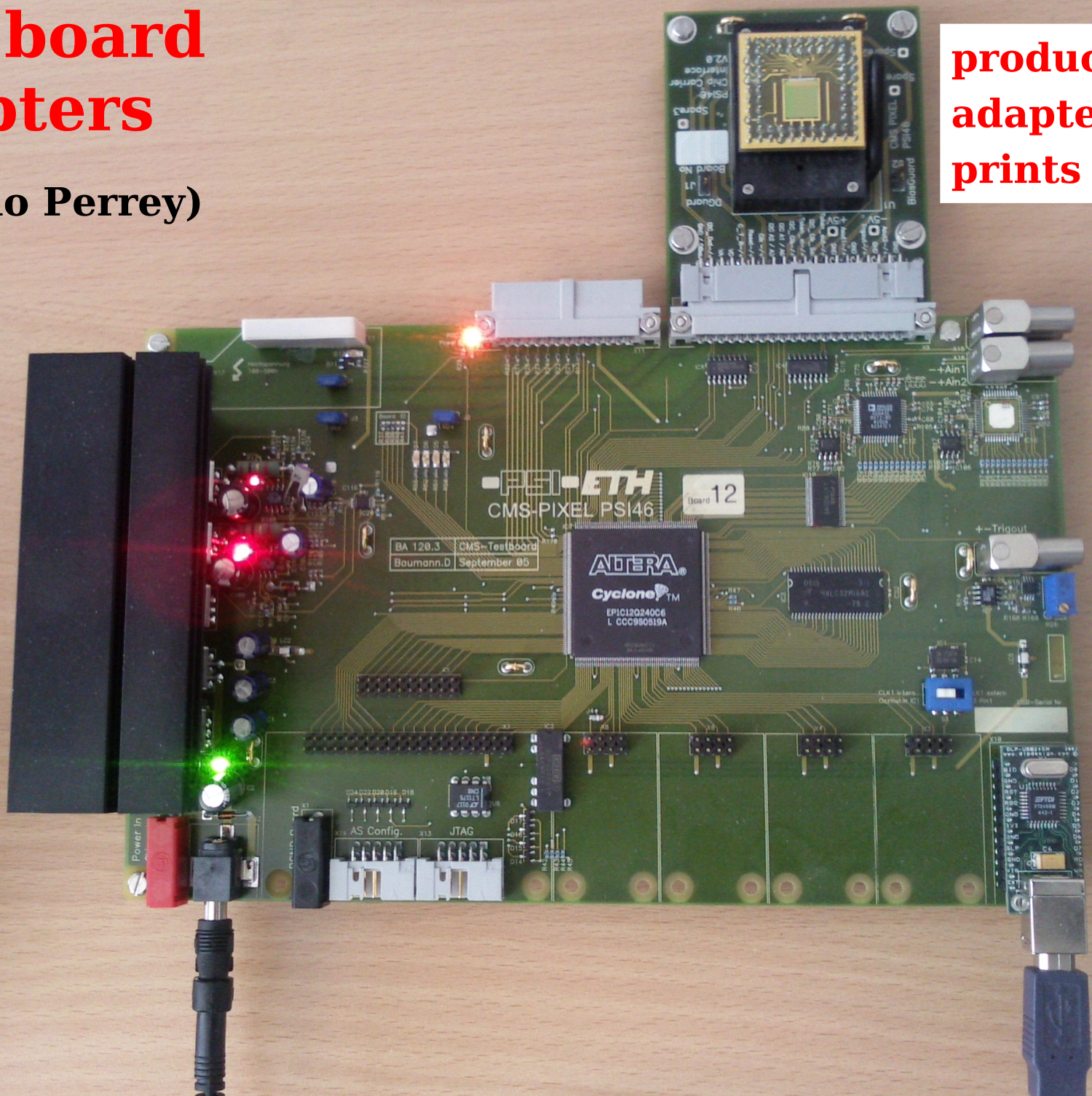
- test beam:
  - synchronize clock to beam: need PLL — Daniel
  - common readout with EUDET telescope — Hanno, Shiraz
  - support for tilted sensor — Adam Zuber, Holger Maser
- Pixel in E-lab 1b:
  - set up Ru source test stand — Daniel
  - establish Marlon self-trigger — Shiraz
  - try ROCs without sensor: takeData at low threshold — Alexey
  - time walk at lowest threshold (vs Vana, vs VrgPr) — Alexey
  - power vs dynamic load — Alexey
- produce more test board adapters:
  - get print design from Silvan Streuli, add Vbias connection — Hanno

Tilted support for the CMS Pixel Testboard in the EUDET telescope



test board adapters

(Hanno Perrey)



problems with psi46expert software

- UB-B-LD:
  - is fine when TBM emulator is disabled
  - UB overwritten by TBM header in emulator mode (Beat Meier)
- PreTest:
  - requires TBM emulator → UB problem
- Trim:
  - works with 10 triggers/point, unstable at 20 ?
- takeData:
  - WBC scan unreliable
  - corrupt data — cured with smaller USB block size?
- visit to PSI in Dec or Jan ?

old slides

Configuration at DESY

- 6 single ROCs (wire bonded to chip carrier).
- 3 ROCS with single-chip sensor (different ROC versions).
- PSI test board, with Aug 2010 FPGA firmware (binary file from Beat Meier downloaded using ALTERA USB Blaster via JTAG connector)
- run in 40 MHz mode
- Dell laptops running Ubuntu 10.10 (or 11.04) Linux.
- psi46expert software compiled using gcc-4-5-2 in AMD 64 bit.
- libftd2xx1.0.2 for USB interface from FTDI: http://www.ftdichip.com/Drivers/D2XX.htm
- Some code changes in USBInterface.h (long → int).

PSI46expert software at DESY

- Several new routines written:
  - DAC scans, noise maps, address decoding...
- Steer psi46expert by command script instead of interactively:
  - faster, reproducible, self-documenting.
- DAC settings for 9 ROCs determined (3 with baby sensor).
- Analysis in ROOT:
  - gain map, threshold map, noise map
- Fast efficiency determination on the FPGA does not work:
  - Configuration problem (single ROC test, no TBM)?
  - Not fixed by FPGA firmware update (Aug 2010 version).
  - Have to use slower USB access...

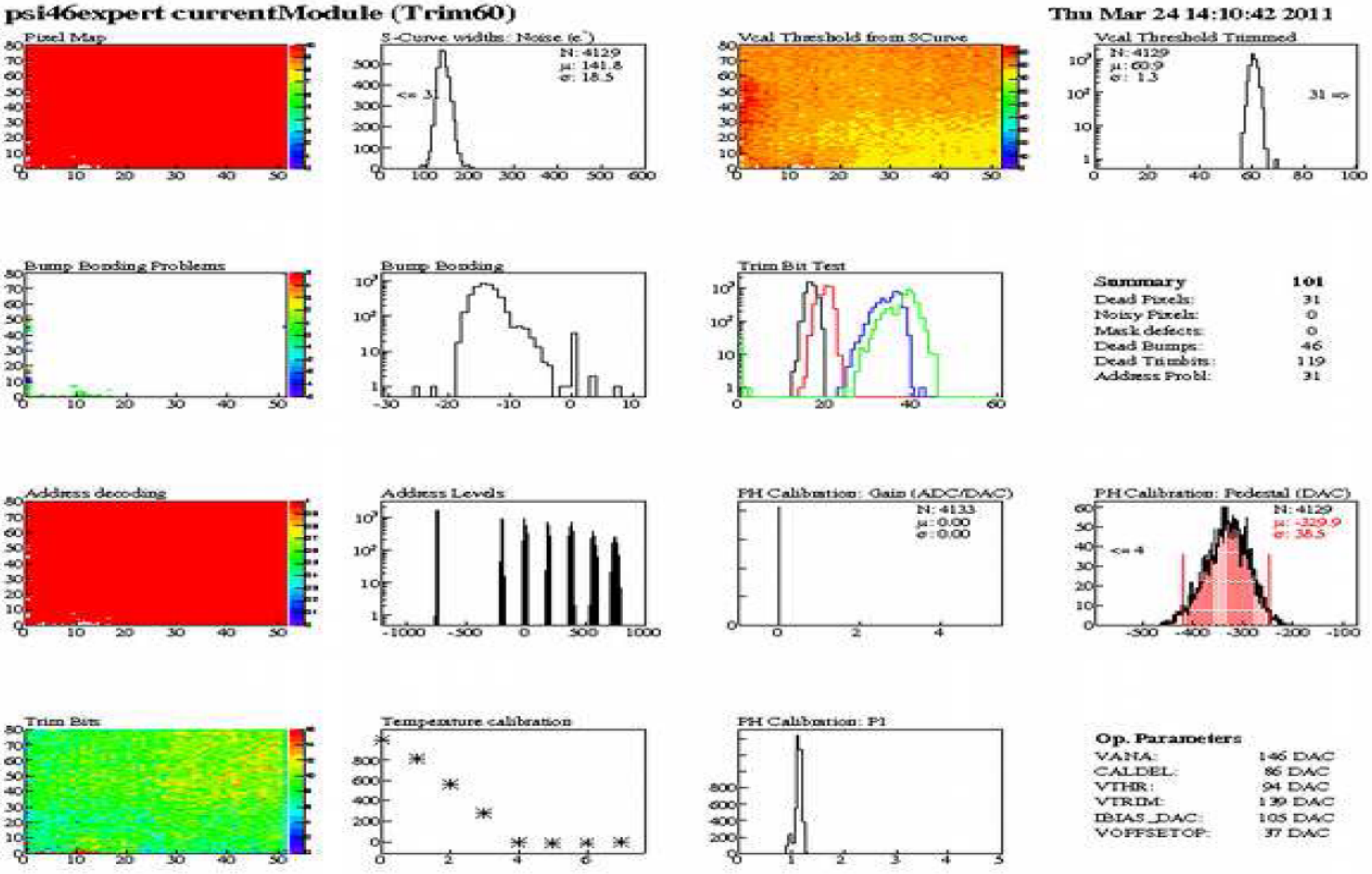
Test board in Karlsruhe

- PSI46 Testboard, firmware version 6.1 (from 27.08.2010)
- Using standard psi46expert software, including some modification by T. Rohe for local trigger
- Running on Scientific Linux 5 32bit
- root version 5.08/00b
- libftd2xx version 4.13

Thomas Weiler
11.5.2011

https://indico.desy.de/conferenceDisplay.py?confId=4352 (protected)

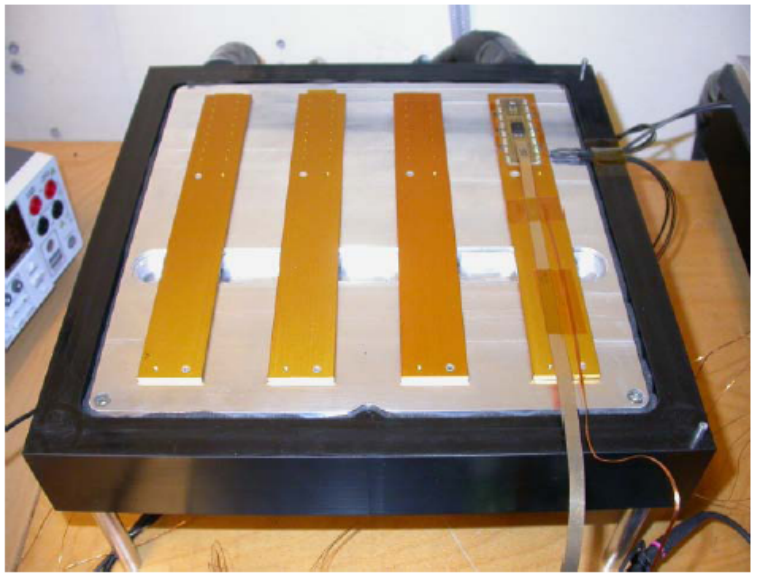
Test board in Karlsruhe



Thomas Weiler

Cold test box in Aachen

- Cold box for 4 modules → workshop
- Peltier element or chiller
- Air dryer, to flush box
- Small vacuum pump to suck modules onto cold plate
- 4 x PSI test system (module adapter plus advanced test board)



Aachen cold box,
PSI test system

Katja Klein
11.5.2011

https://indico.desy.de/conferenceDisplay.py?confId=4352 (protected)

Test board activists in Germany 2011

- DESY:
  - Daniel Pitzl daniel.pitzl@desy.de
  - Alexey Petrukhin petr@mail.desy.de
  - expect student, summer student
- Karsruhe:
  - Thomas Weiler Thomas.Weiler@iekp.fzk.de
- Aachen:
  - Jan Sammet jan.sammet@physik.rwth-aachen.de
  - Katja Klein Katja.Klein@cern.ch
- Hamburg:
  - Georg Steinbrück georg.steinbrueck@desy.de
  - possible student

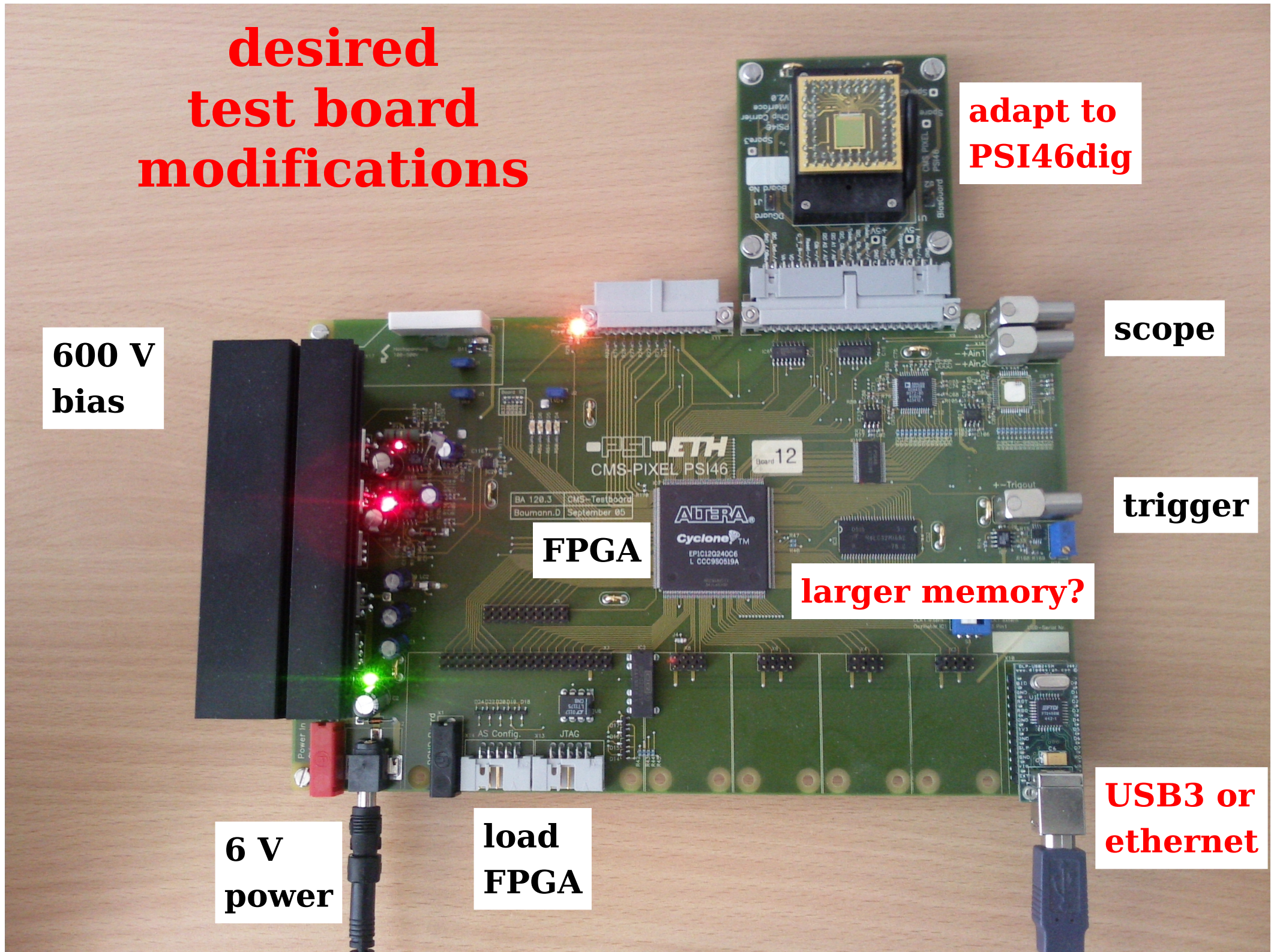
Test board needs in Germany

task	HH	Ka/Ac	D
development	2	2	
bare module test	2	2	
module testing	2	2	
rework	1	1	
cold calibration	4	4	
X-ray calibration	1	1	
high rate test	1	1	
layer system test	2	0	
sum	15	13	28

test board desirables

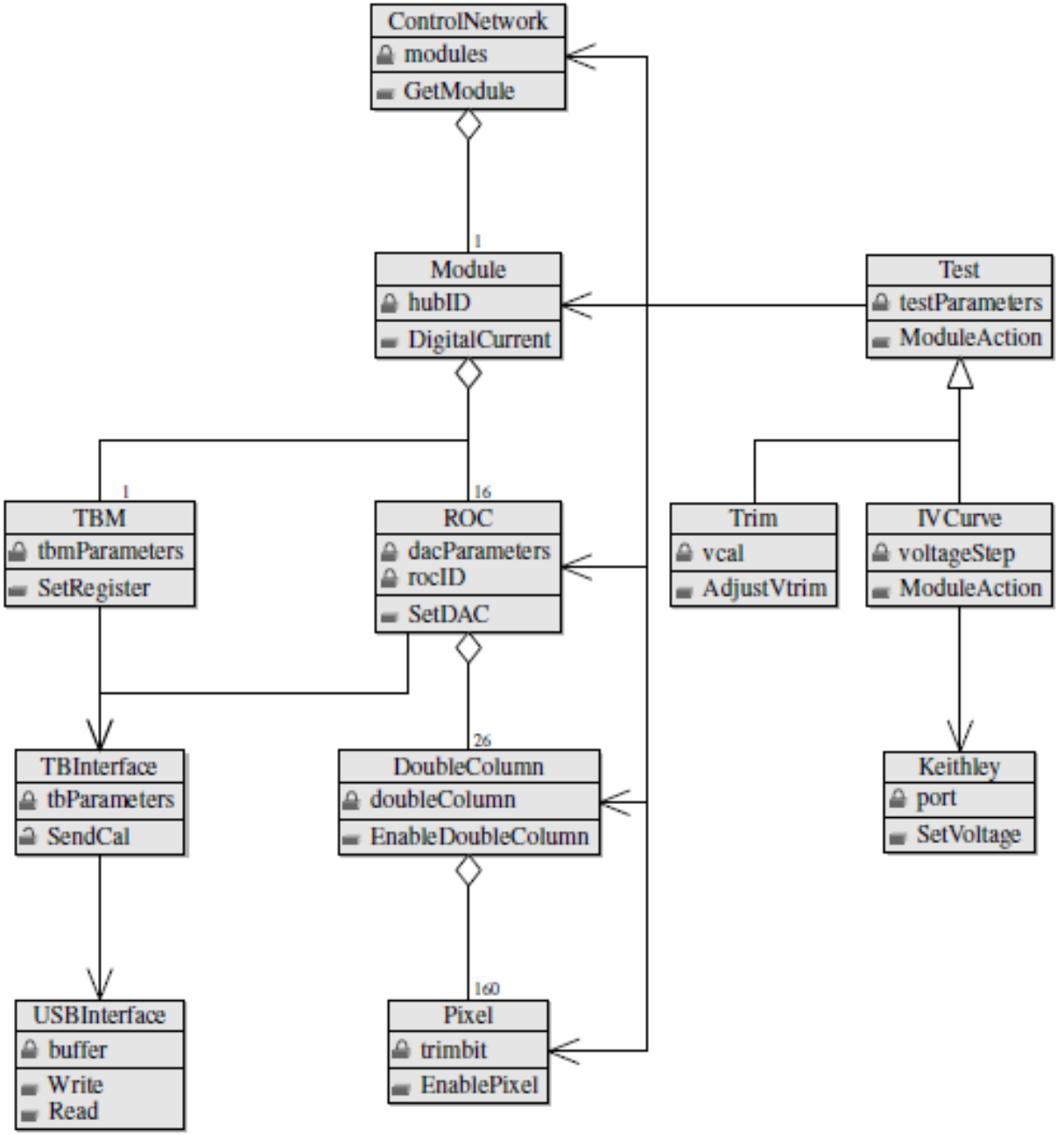
- interface for the digital protocol
- faster interface (USB3 or Ethernet):
  - for pixel-wise tests
- larger memory:
  - for Xray, high rate and beam tests

- More ROCs and full modules for education and code development soon.
- common software base
  - central SVN repository?
- Common test procedures and acceptance criteria
- Common data base
- Common module identification scheme


desired
test board
modifications
adapt to
PSI46dig
600 V
bias
scope
trigger
FPGA
larger memory?
6 V
power
load
FPGA
USB3 or
ethernet
PSI-ETH
CMS-PIXEL PSI46
ALTERA
Cyclone
AS Config.
JTAG

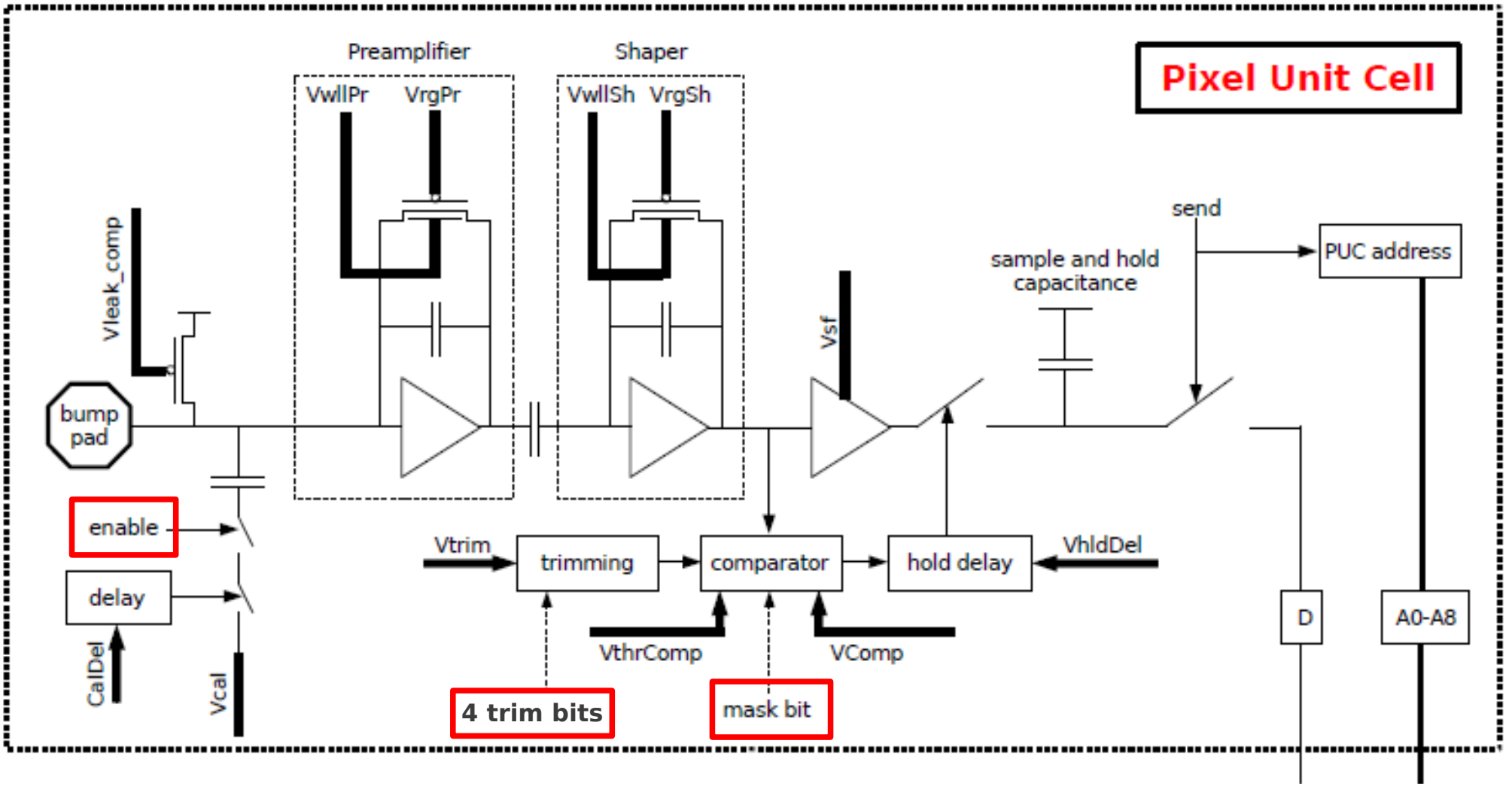
some ROC test results from DESY

psi46expert software



- C++ class library.
- Written by Peter Trüb (ETH, 2005-2007) for Scientific Linux (32 bit).
- Now compiled with g++ 4.4.5 under Ubuntu 10.10 (64 bit).
- USB interface required some changes (long → int).
- Lot's of code – only a small portion explored so far...

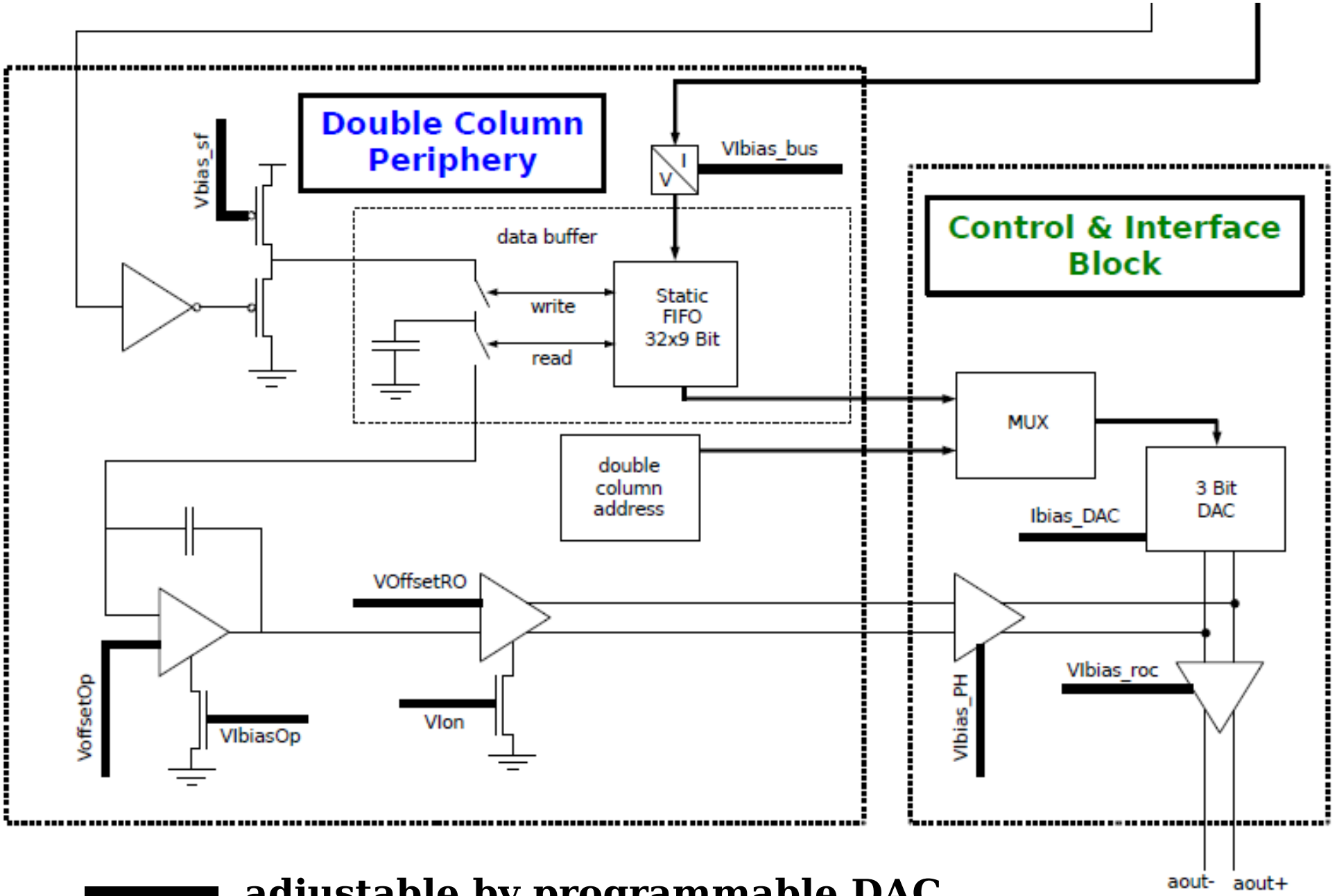
psi46 pixel readout chip



adjustable by programmable DAC, per ROC

programmable register, per pixel

psi46 pixel readout chip



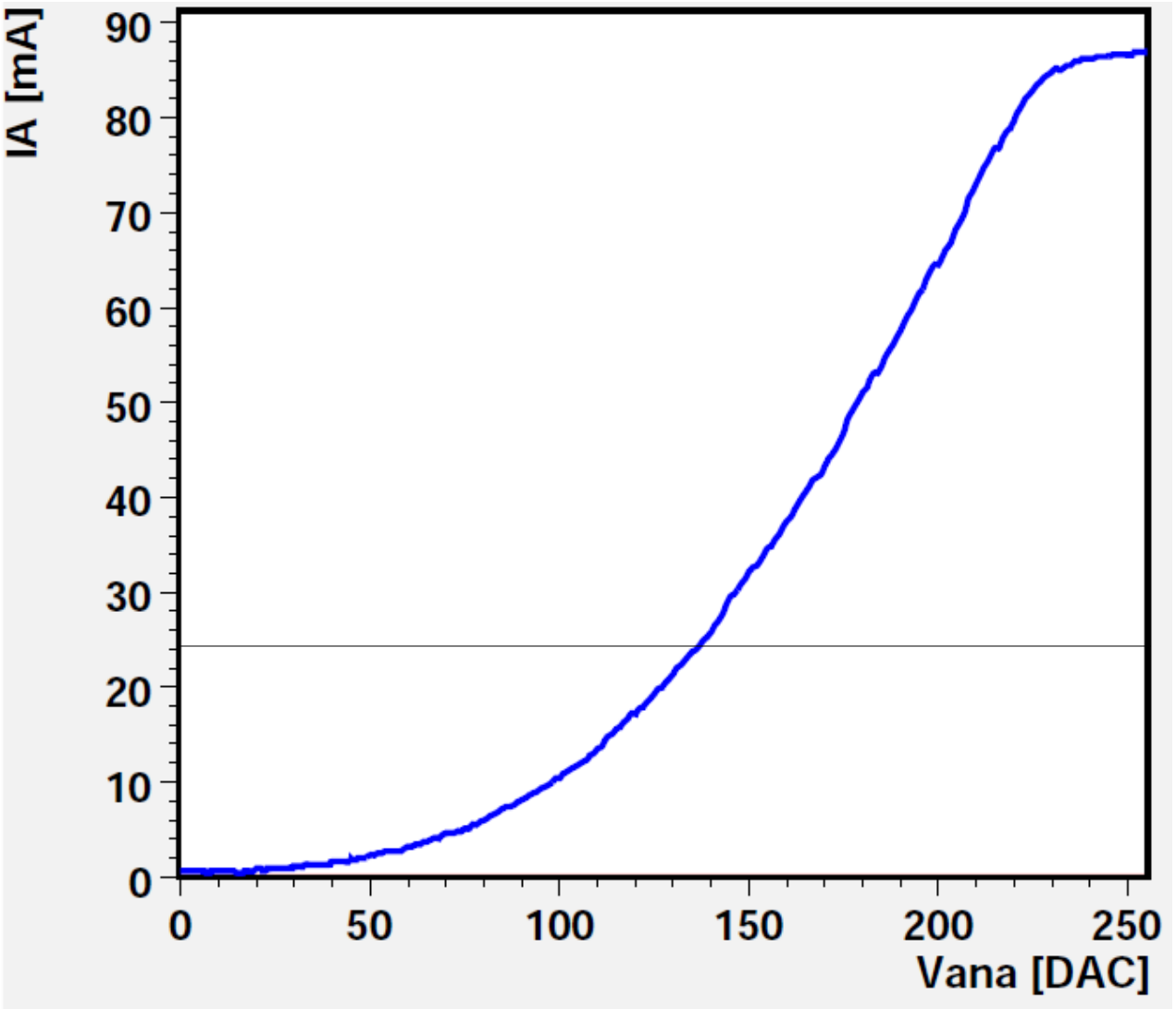
adjustable by programmable DAC

psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

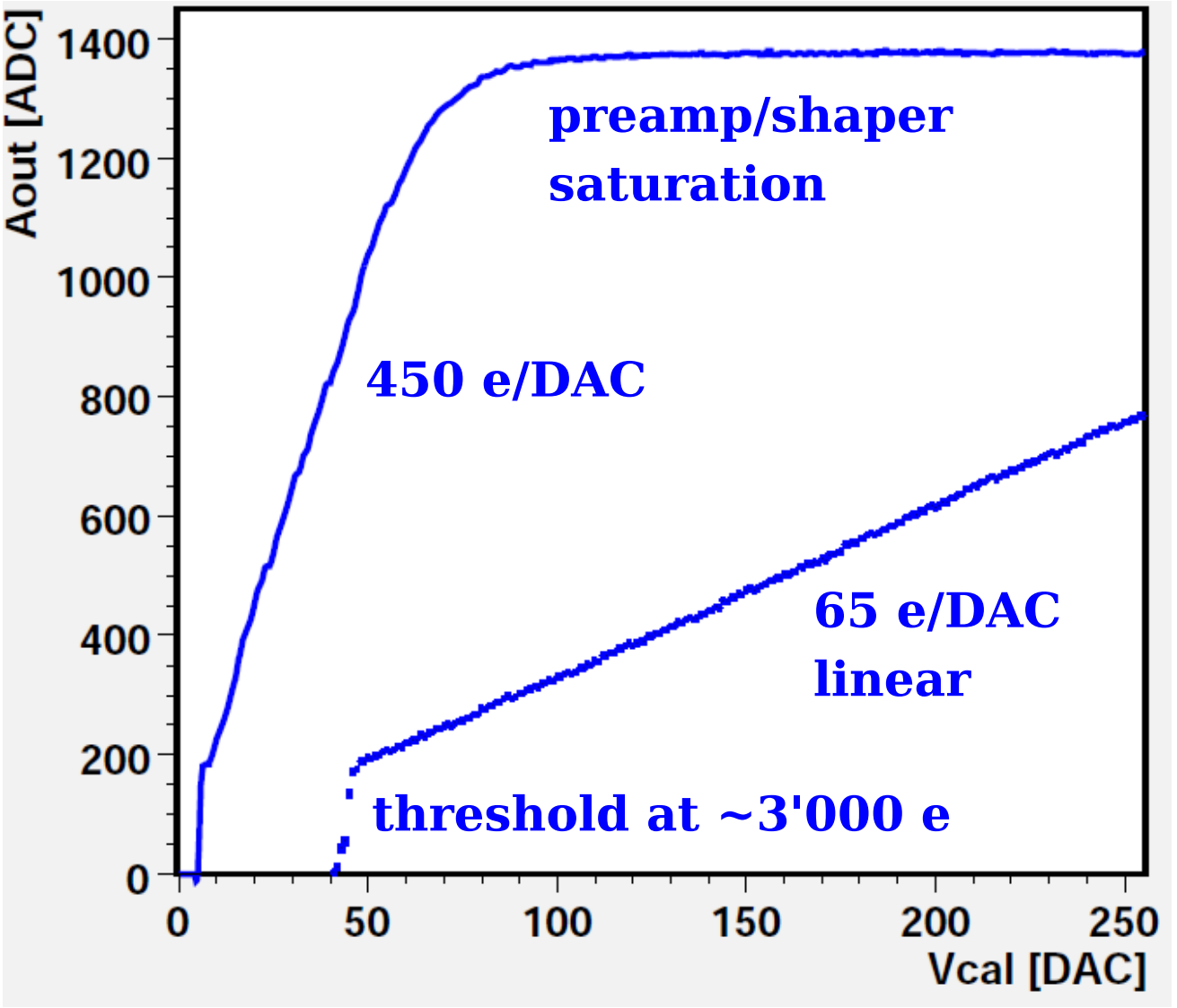
power



currents measured on test board.

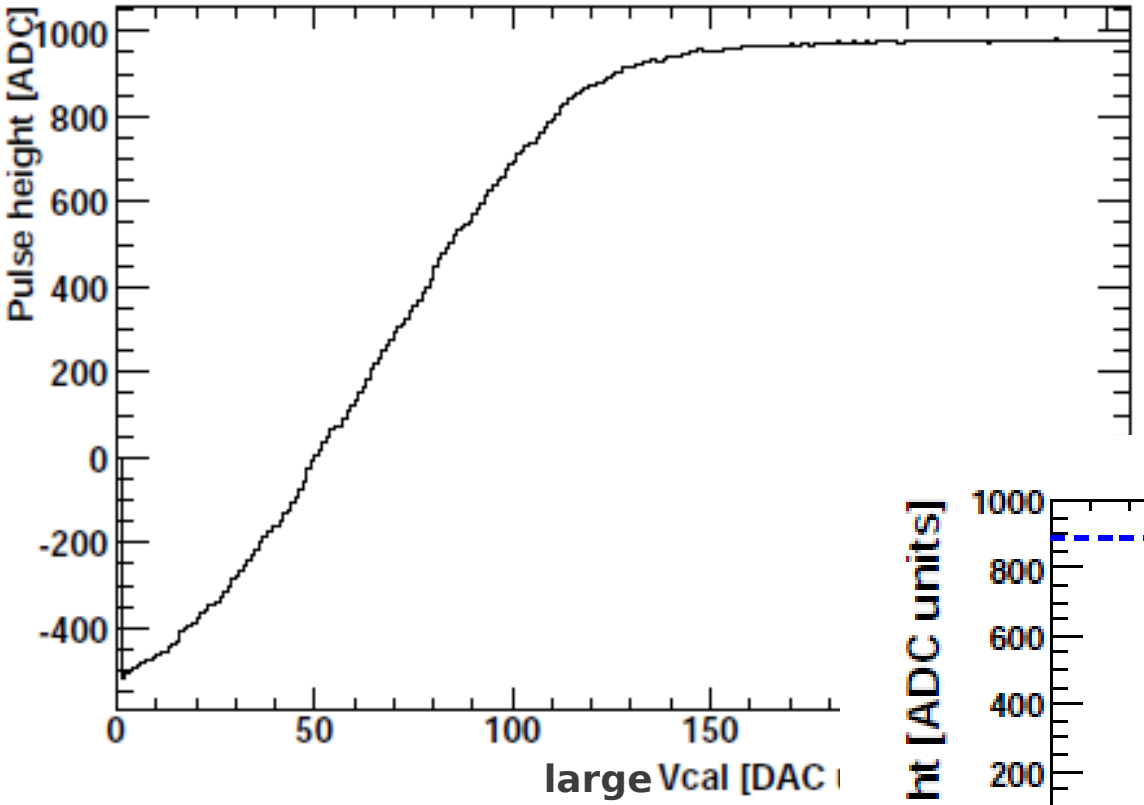
- External supply:
  - VA = 1.7 V,
  - VD = 2.5 V.
- Analog and digital voltage can be further regulated on chip.
- PSI:
  - IA = 25 mA,
  - ID = 35 mA.
  - total 130 mW / chip
  - 31 µW / pixel,
  - 2.1 W/module,
  - 1.5 kW for Barrel.

gain and linear range



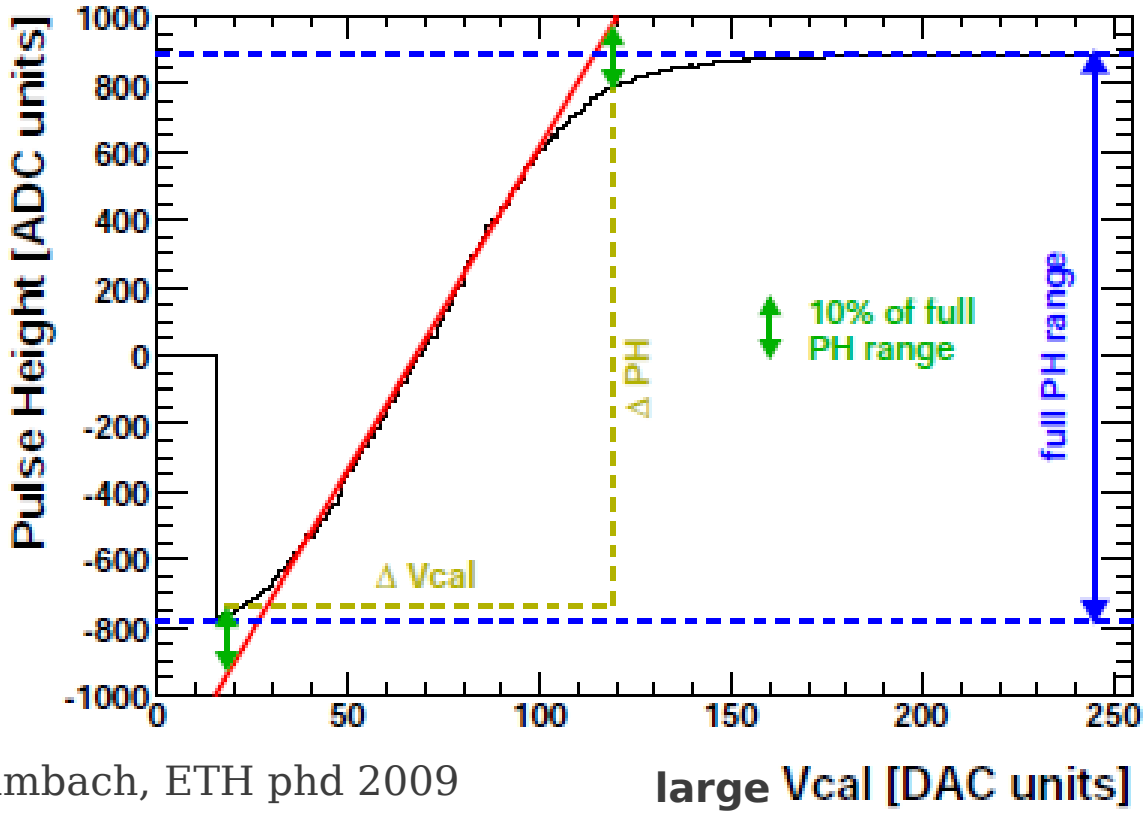
- One pixel.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.
- Linearity for small pulses important for spatial resolution using charge sharing.
- Saturation around 36'000 e (~1.5 MIP).

linear range and saturation at PSI



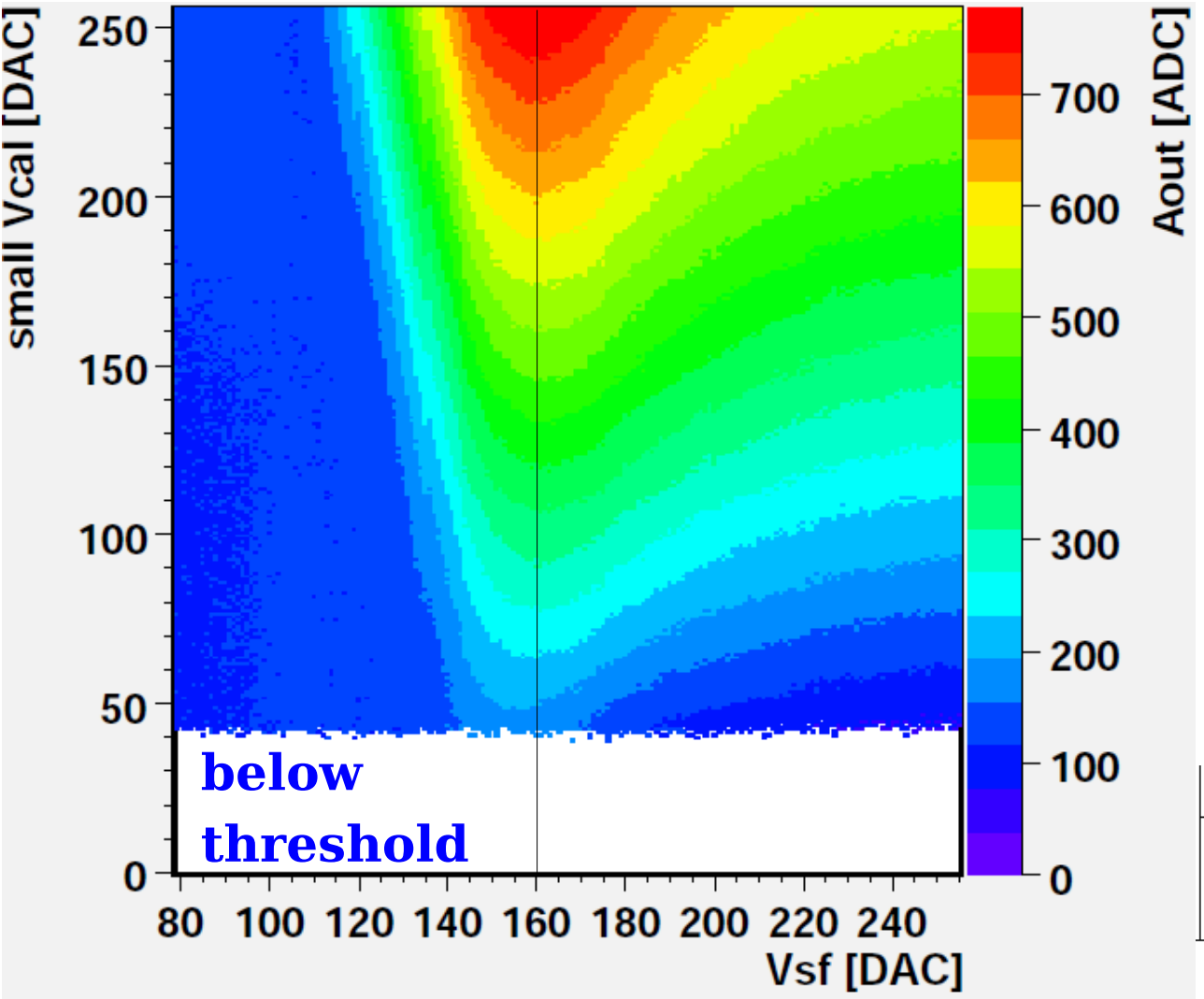
P. Trüb, ETH phd 2008

- Taken at PSI:
  - looks similar.
  - somewhat larger linear range
  - different working point?

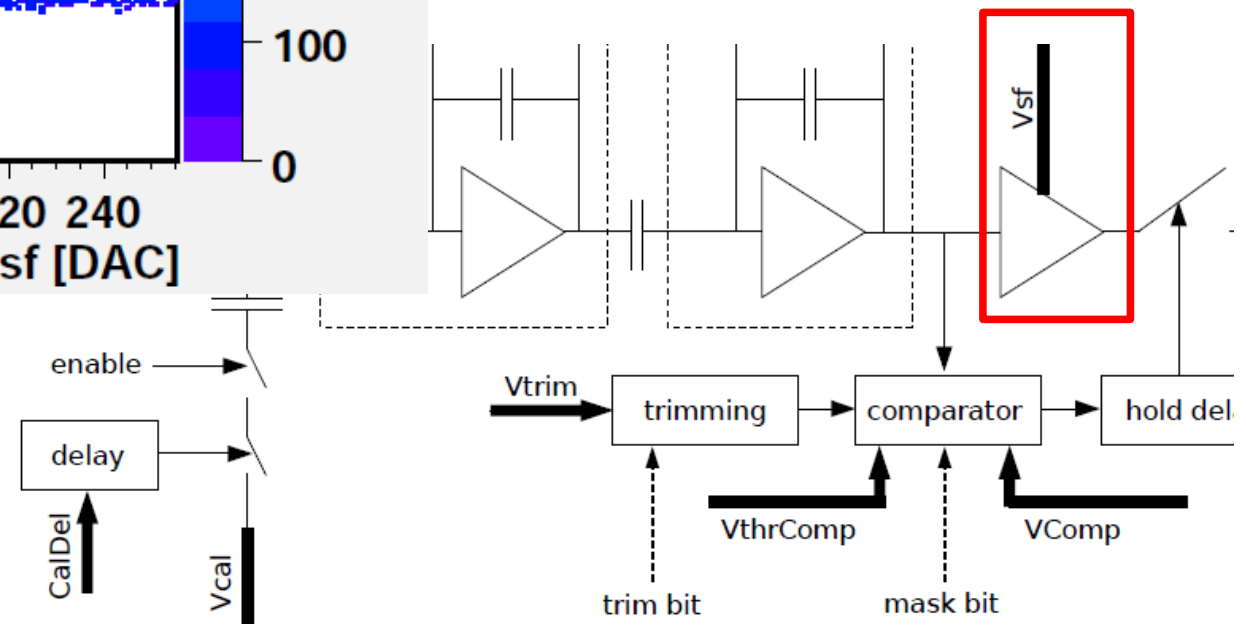


S. Dambach, ETH phd 2009

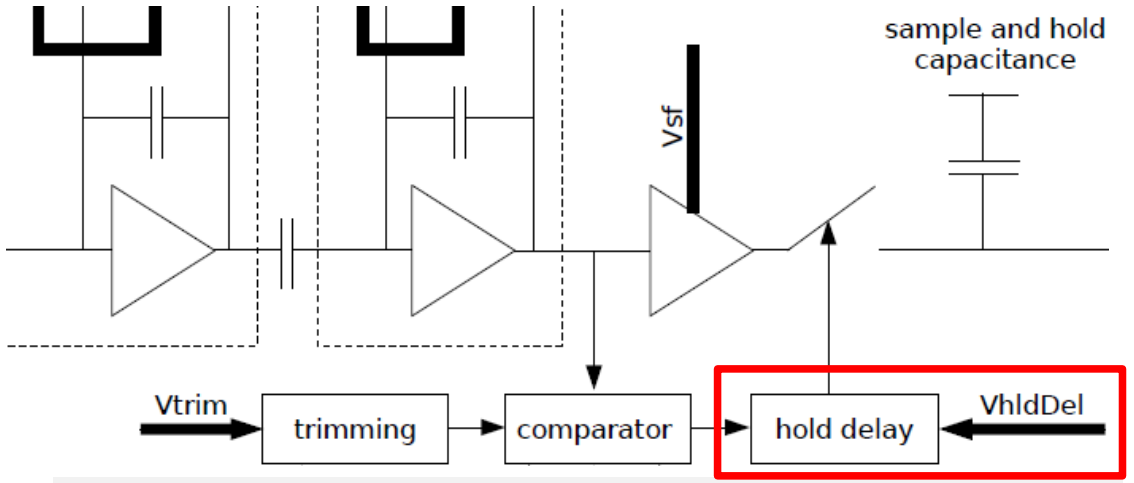
Linear range vs Vsf

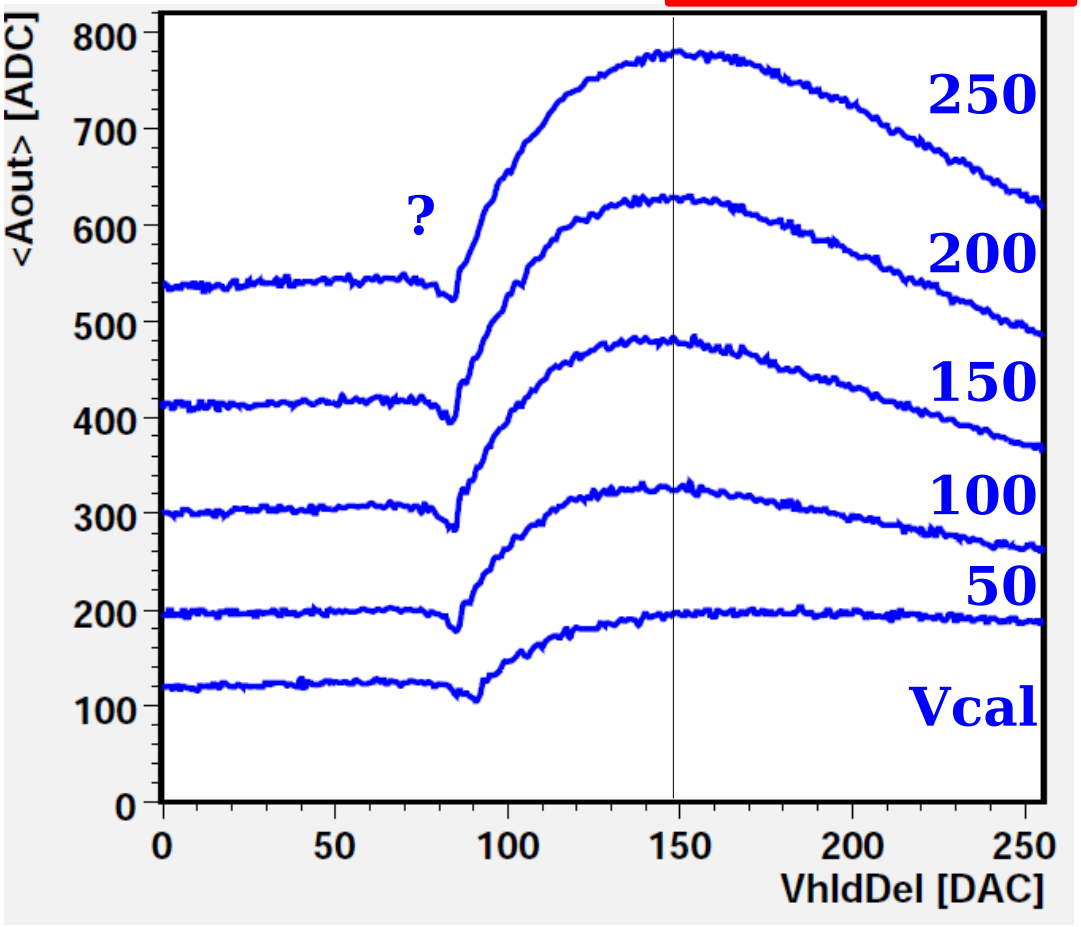


- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Best linearity in valley.



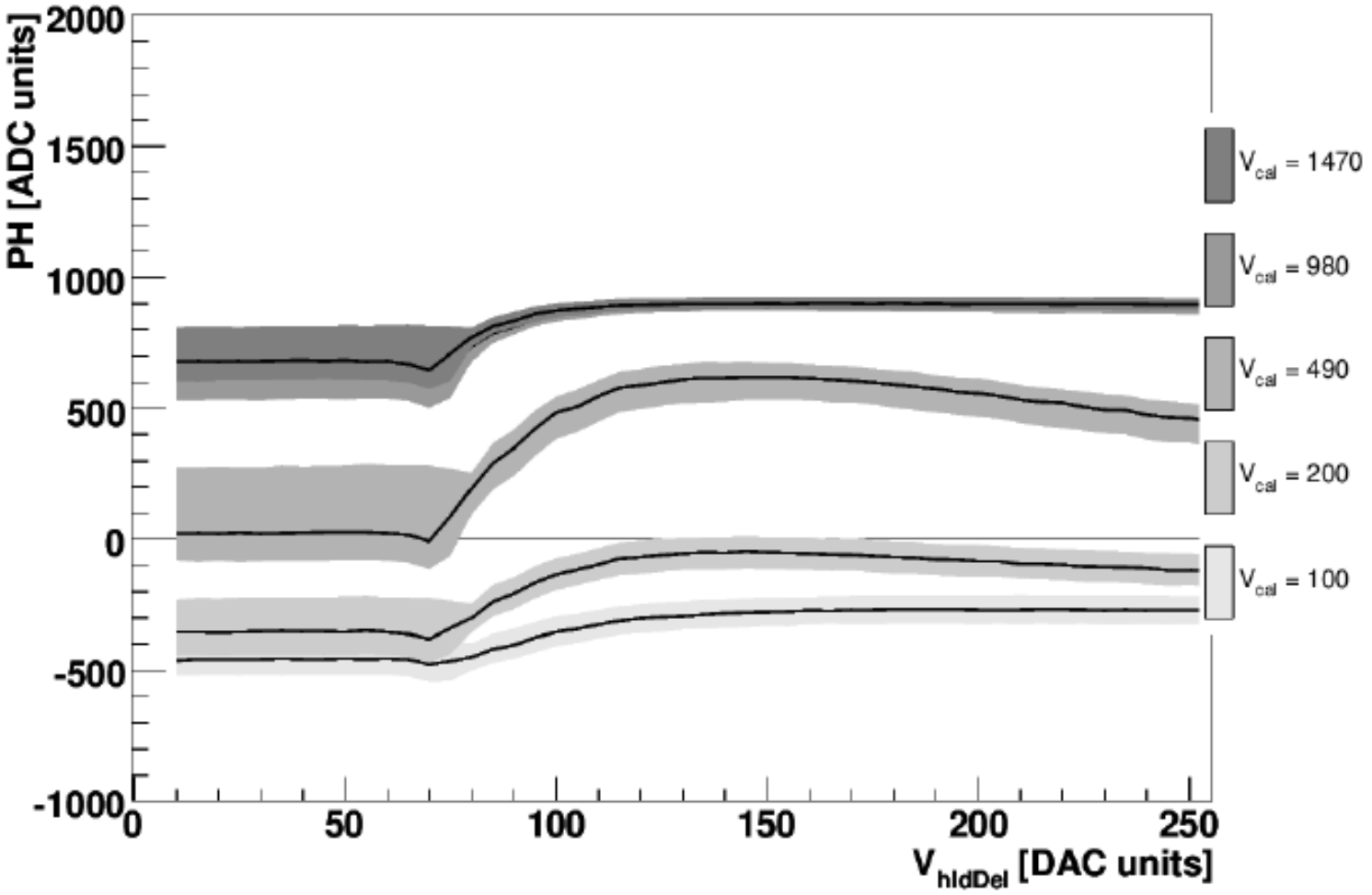
Sample and hold timing





- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 150 is compromise

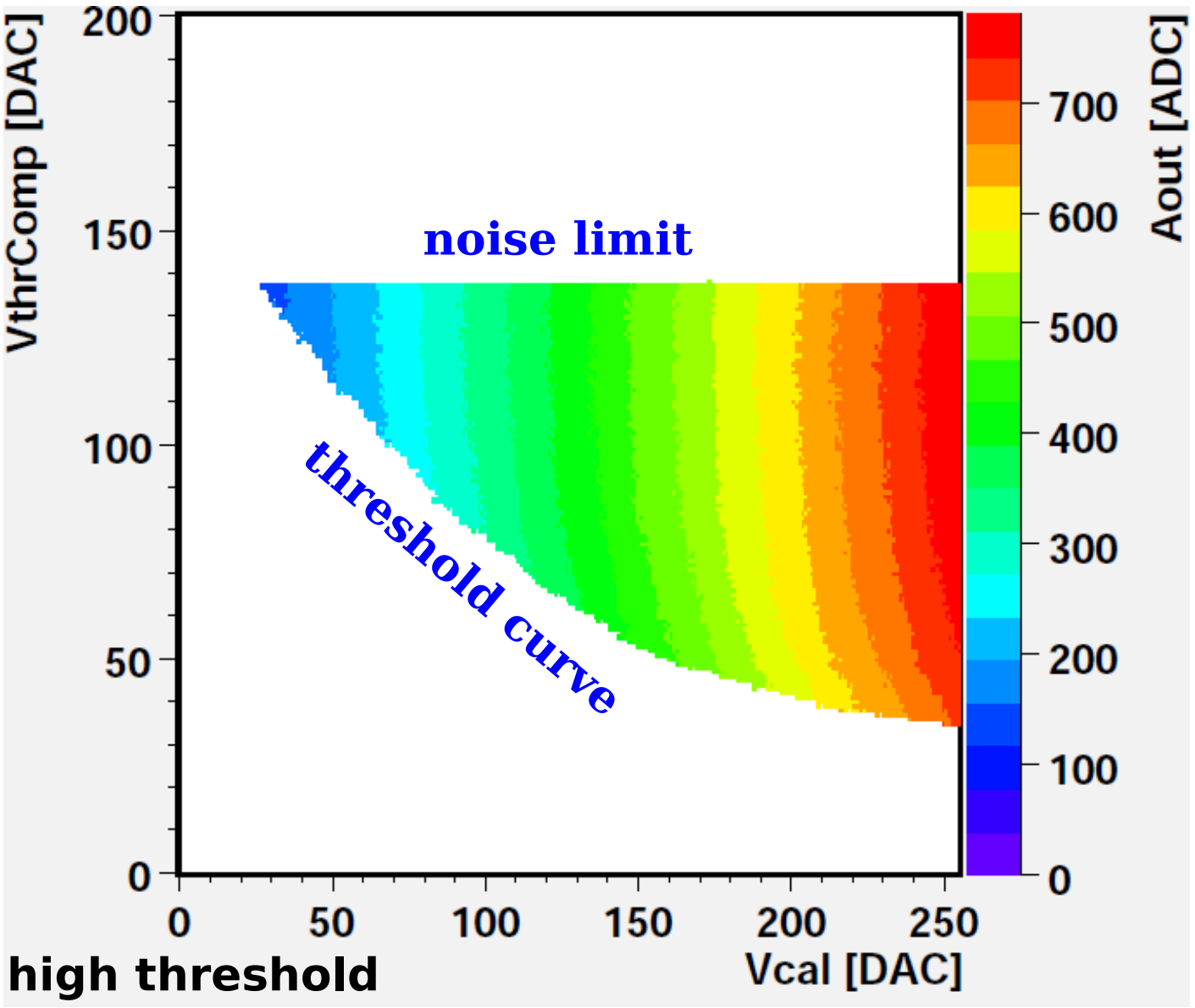
Sample and hold timing at PSI



- Similar observations
- Somewhat different working point.

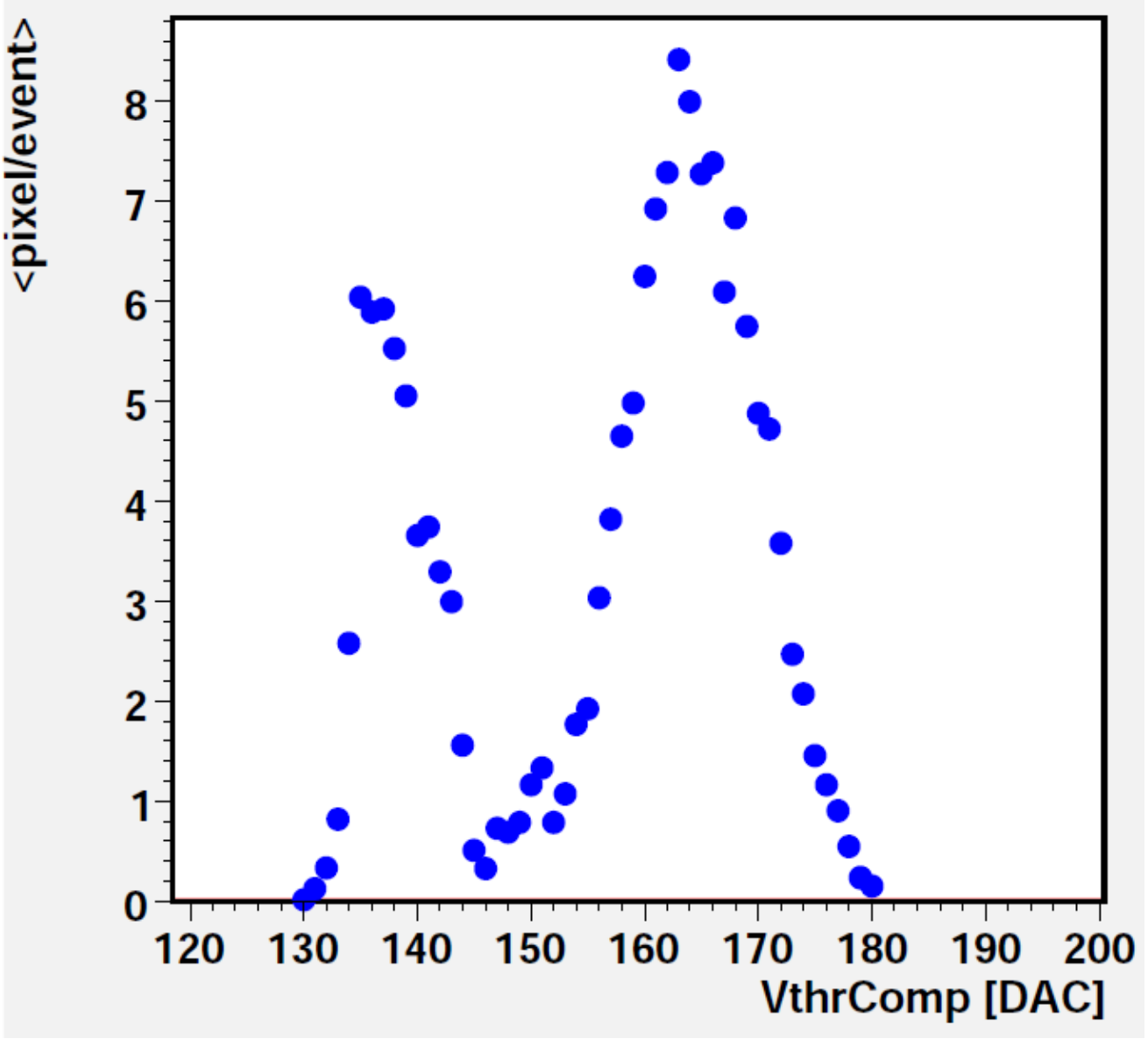
S. Dambach, ETH phd 2009

Comparator threshold



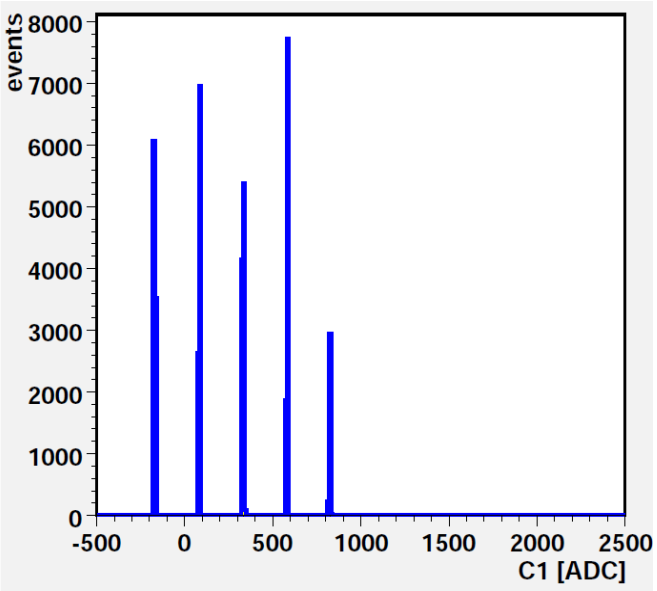
- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

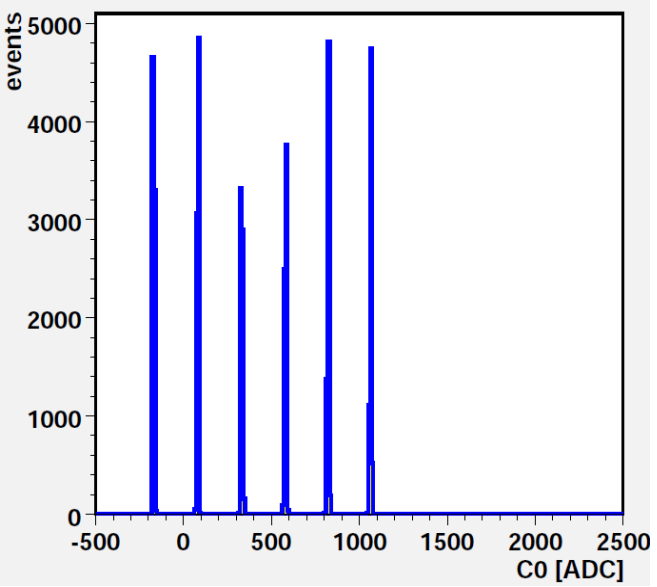
Noise limit



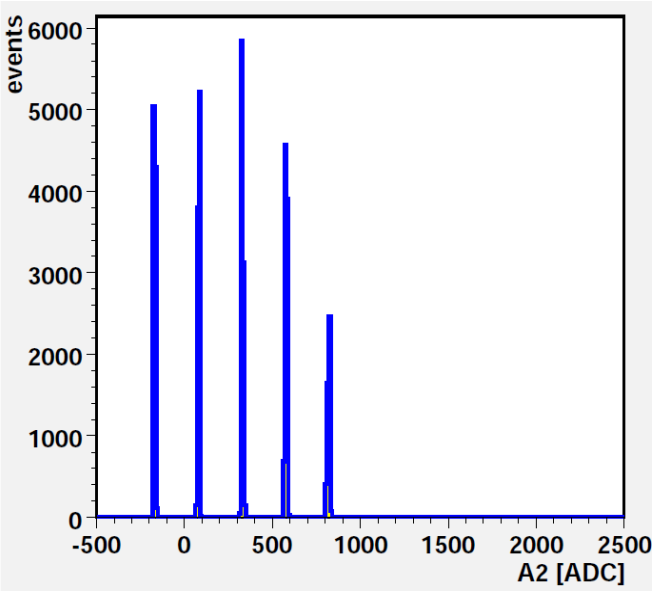
- Activate all 4160 pixels!
- Take random trigger (50 Hz).
- Count pixels.
- Scan threshold.
- Chip is quiet for thresholds below 130.
- 2 noisy regions around 138 and 166.
- Comparator does not work for thresholds above 180.

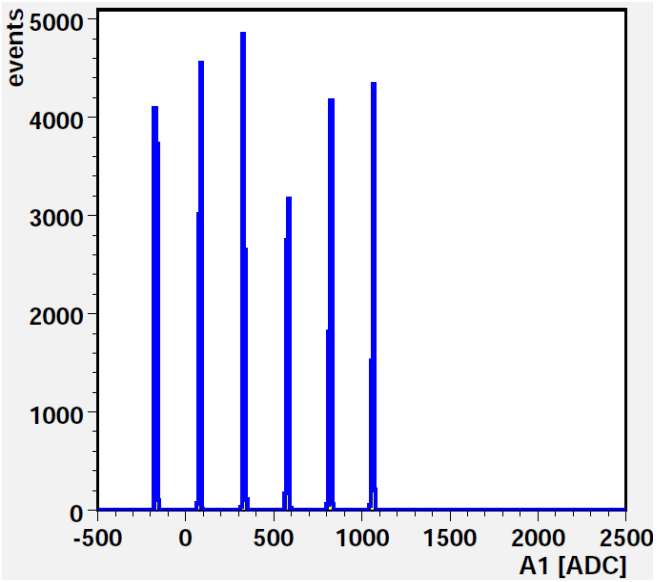
Pixel address

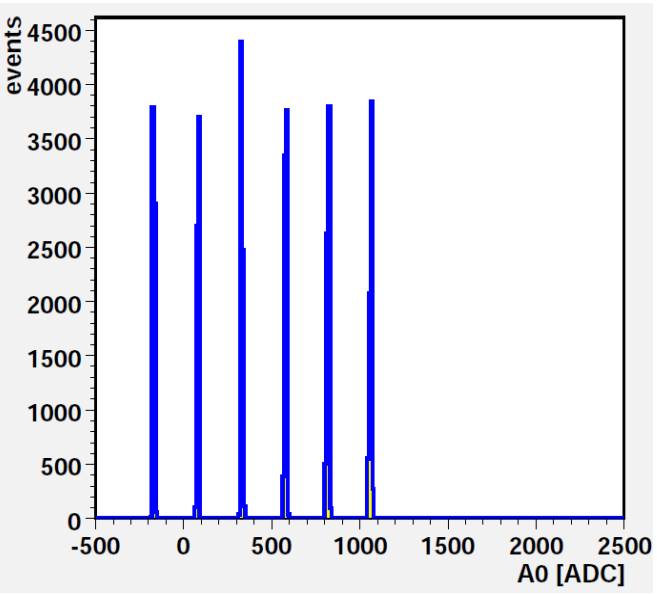




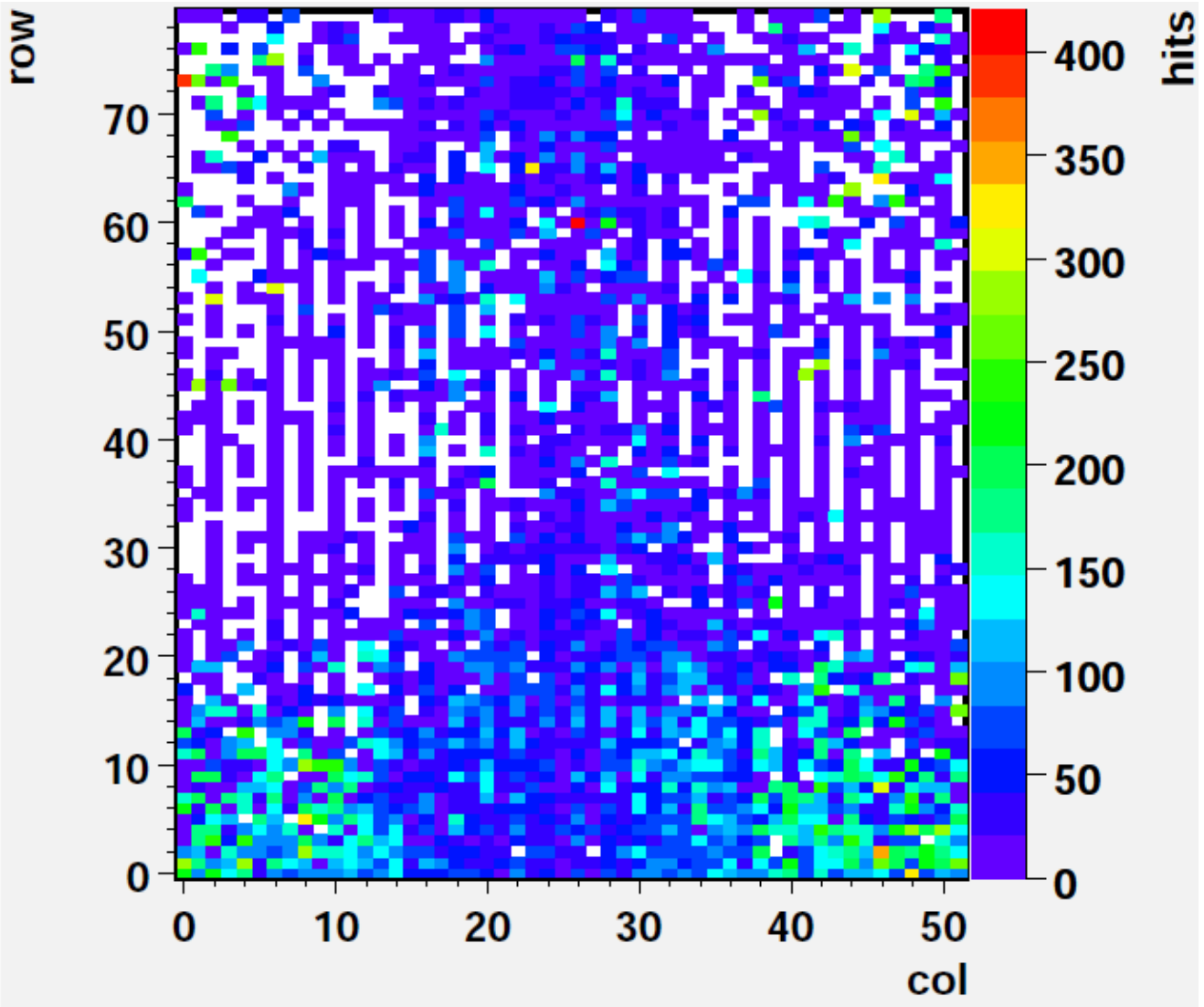
Pixel address in 5 data:
C1,C0 d-columns 0..25
A2, A1, A0 rows 0..159
each with 6 analog levels (2.5 bit).
All well separated.
Decode → col, row.





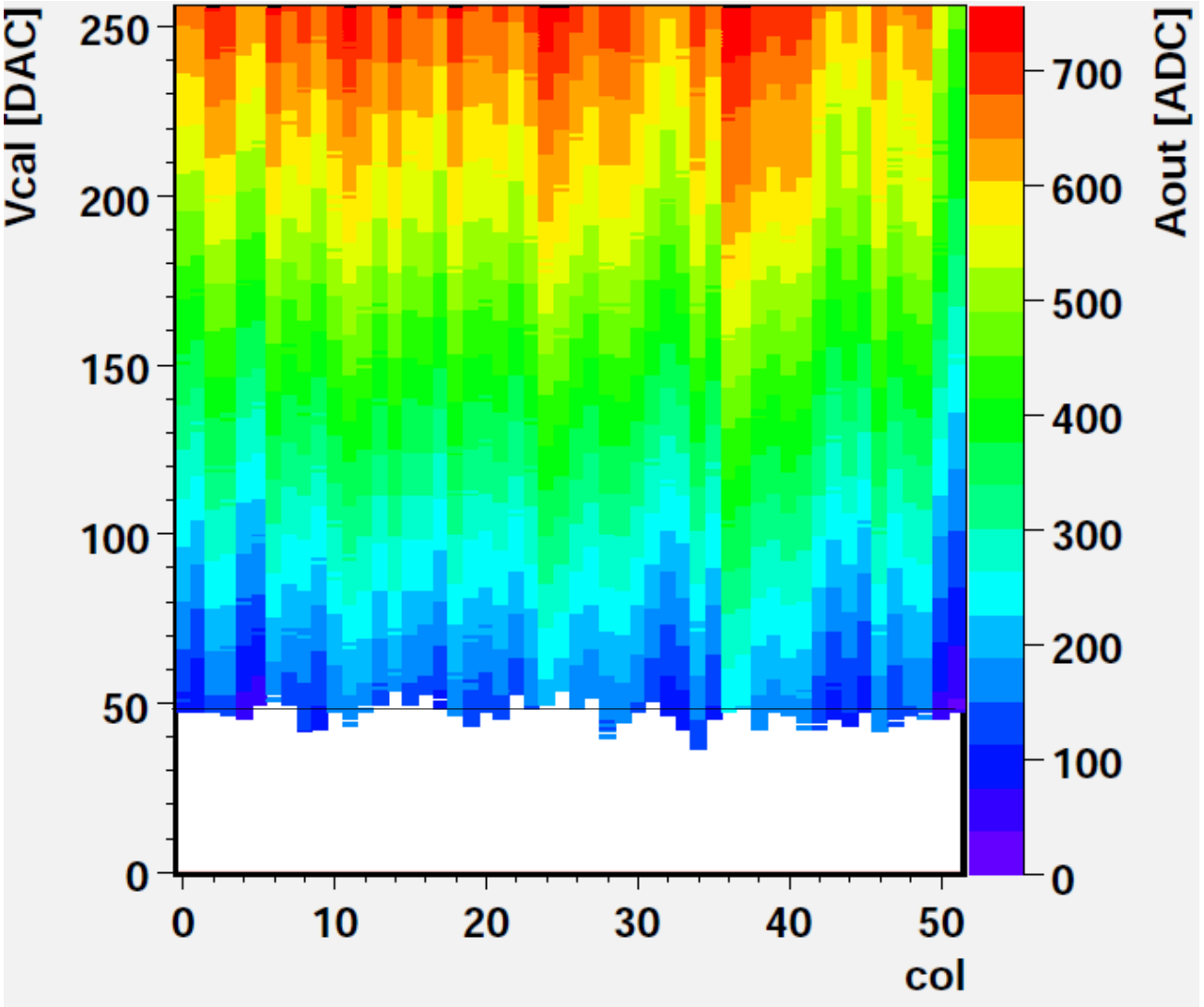


Noise map



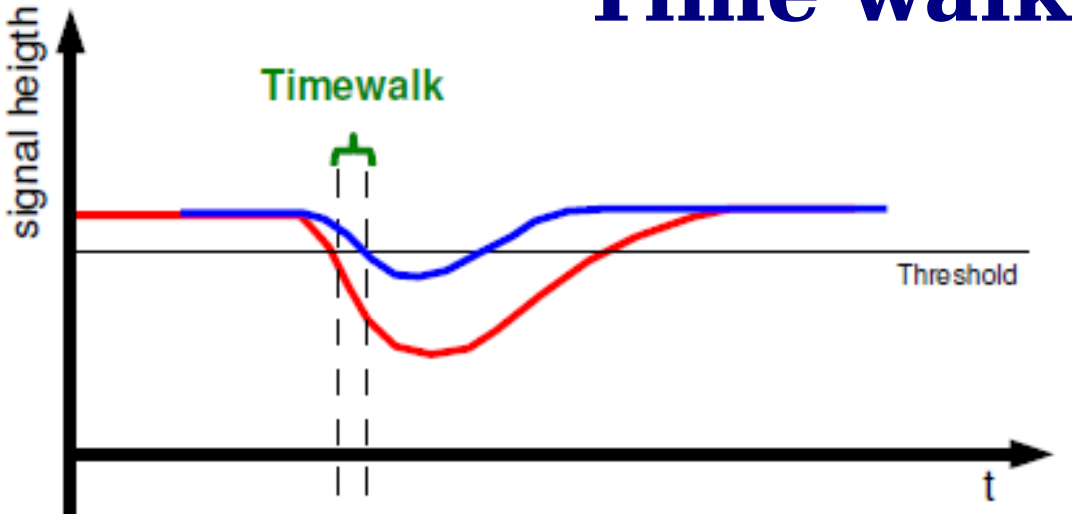
- Activate all 4160 pixels!
- Take random trigger (50 Hz).
- Scan threshold.
- Decode pixel address.
- White regions are quiet?
- Even-odd column pattern?
- Noisy regions vary with threshold.

Threshold variation

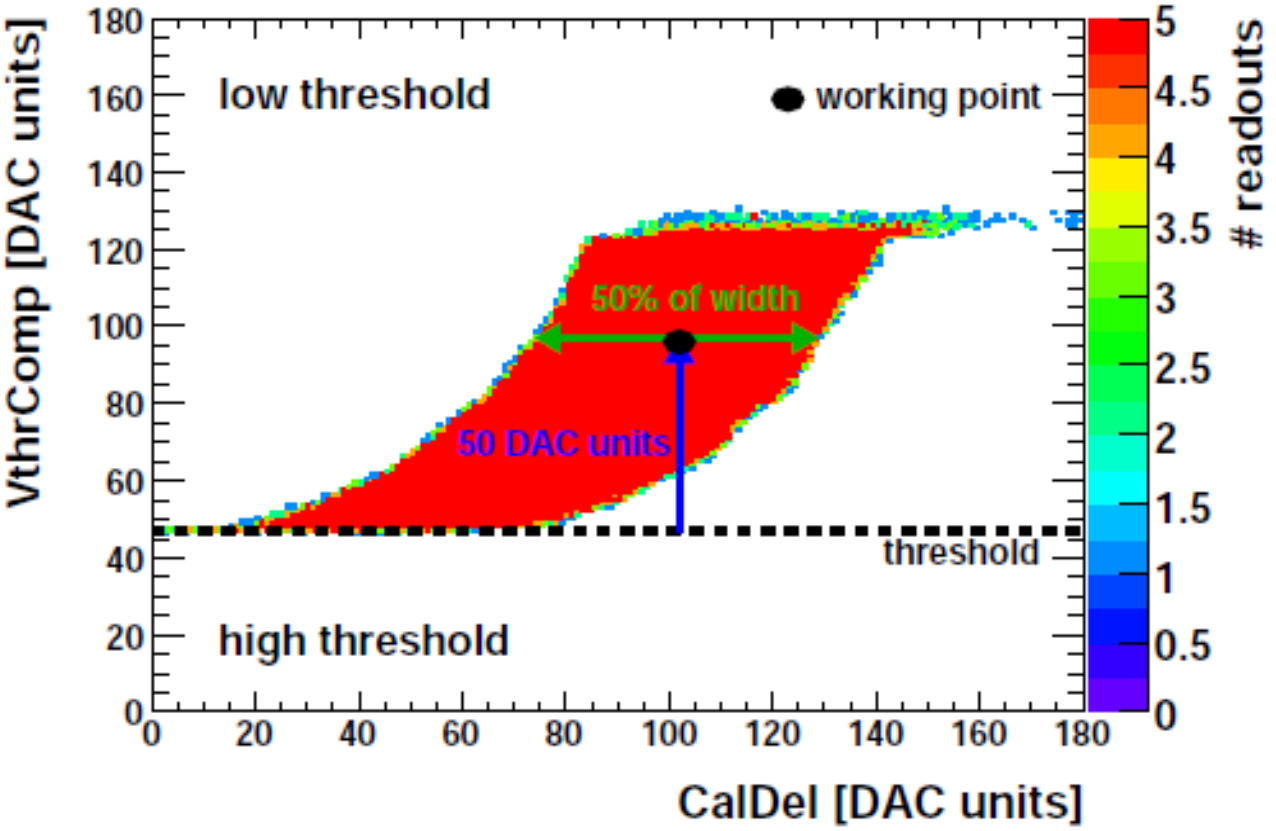


- Vcal scan for pixel 4 in each column 0..51.
- White region: no signal.
- Threshold varies by about ±5 DAC:
  - spread can be reduced by trimming.
- Columns 50, 51 have low gain.
  - systematic feature?

Time walk at PSI

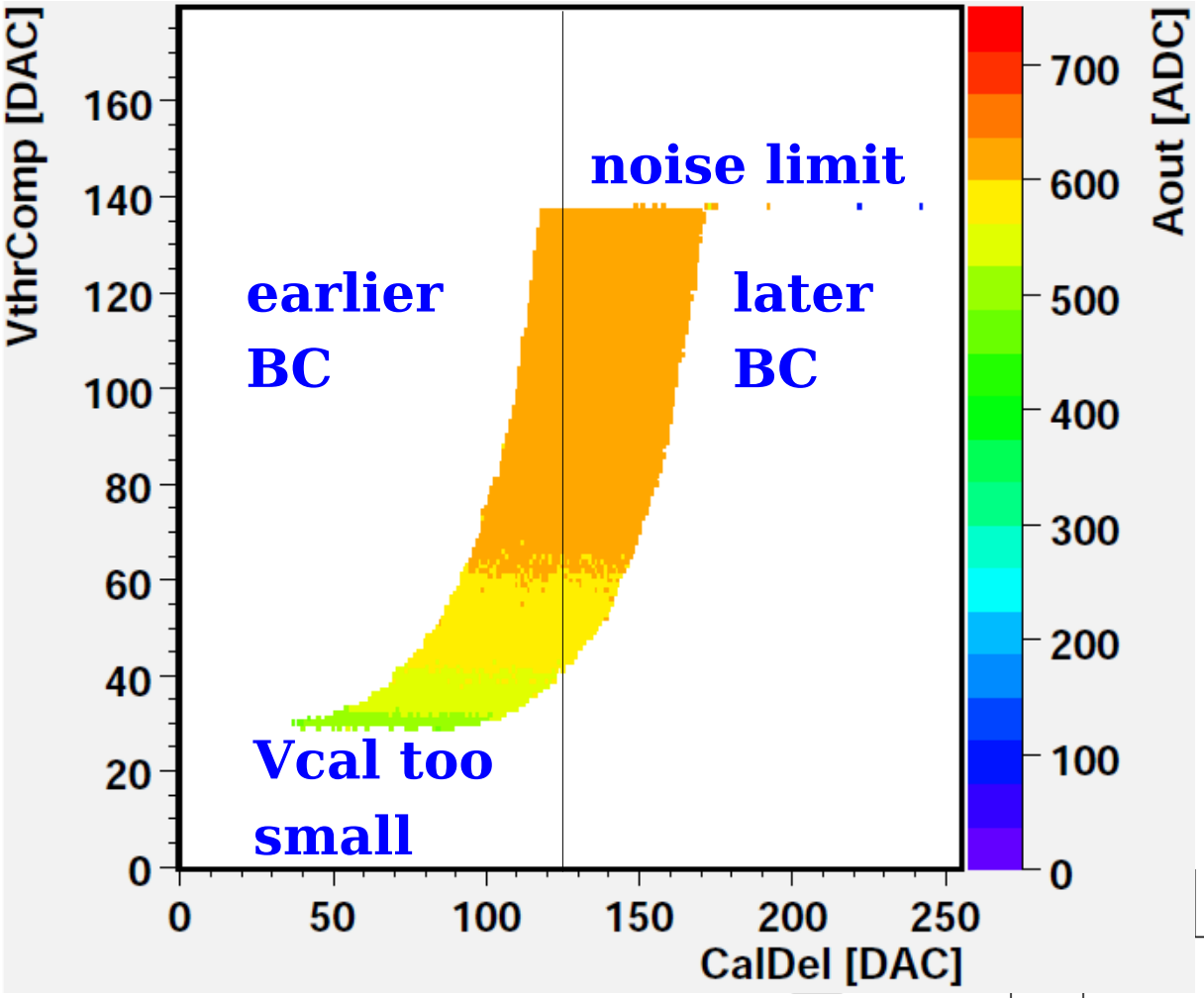


- A
  - t
- L

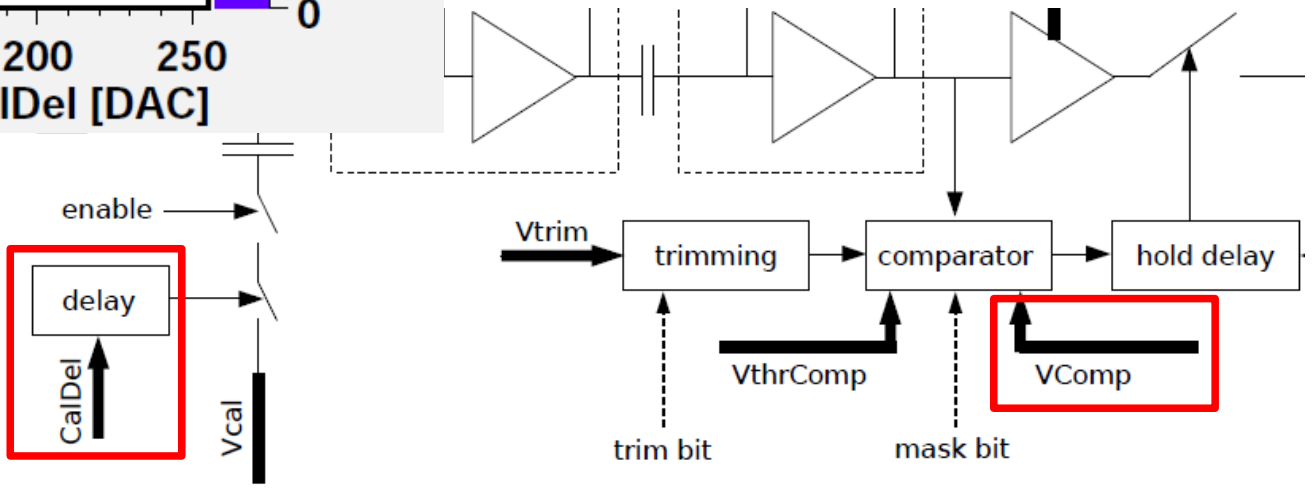


S. Dambach, ETH phd 2009

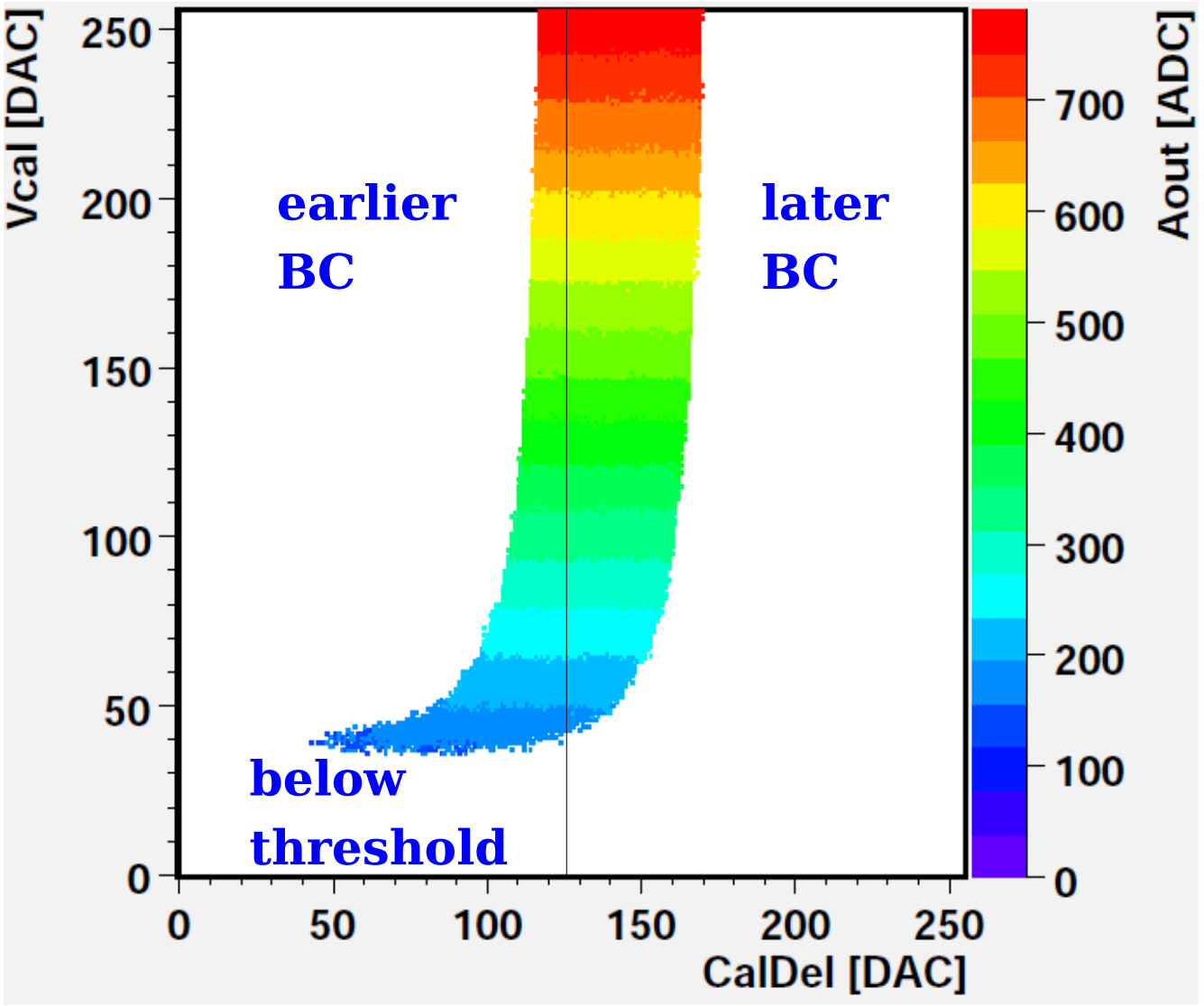
Time walk

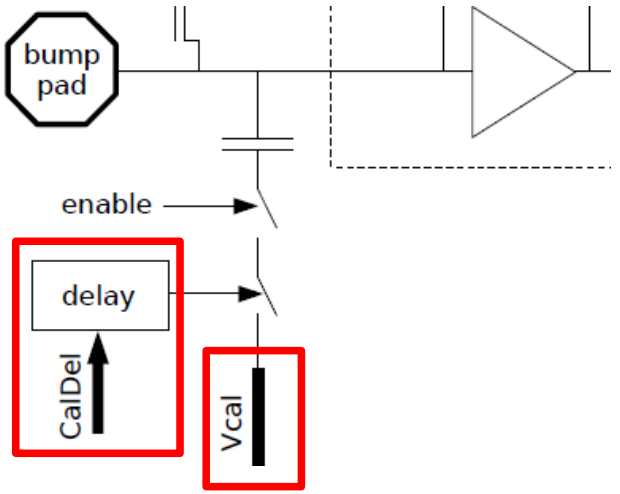


- One pixel.
- Vcal 200 small DAC.
- Moving the threshold shifts the timing:
  - time walk.



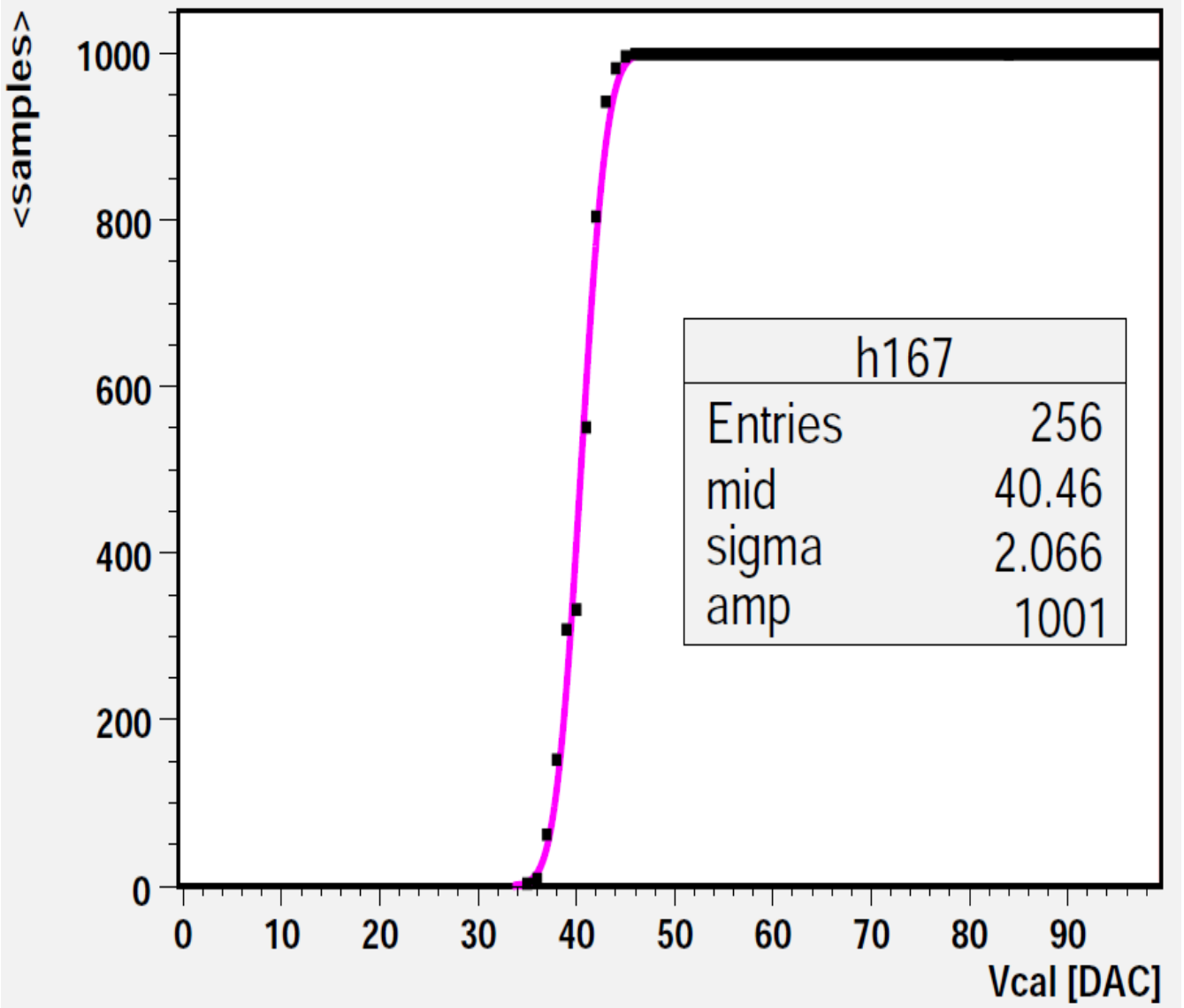
Calibrate timing





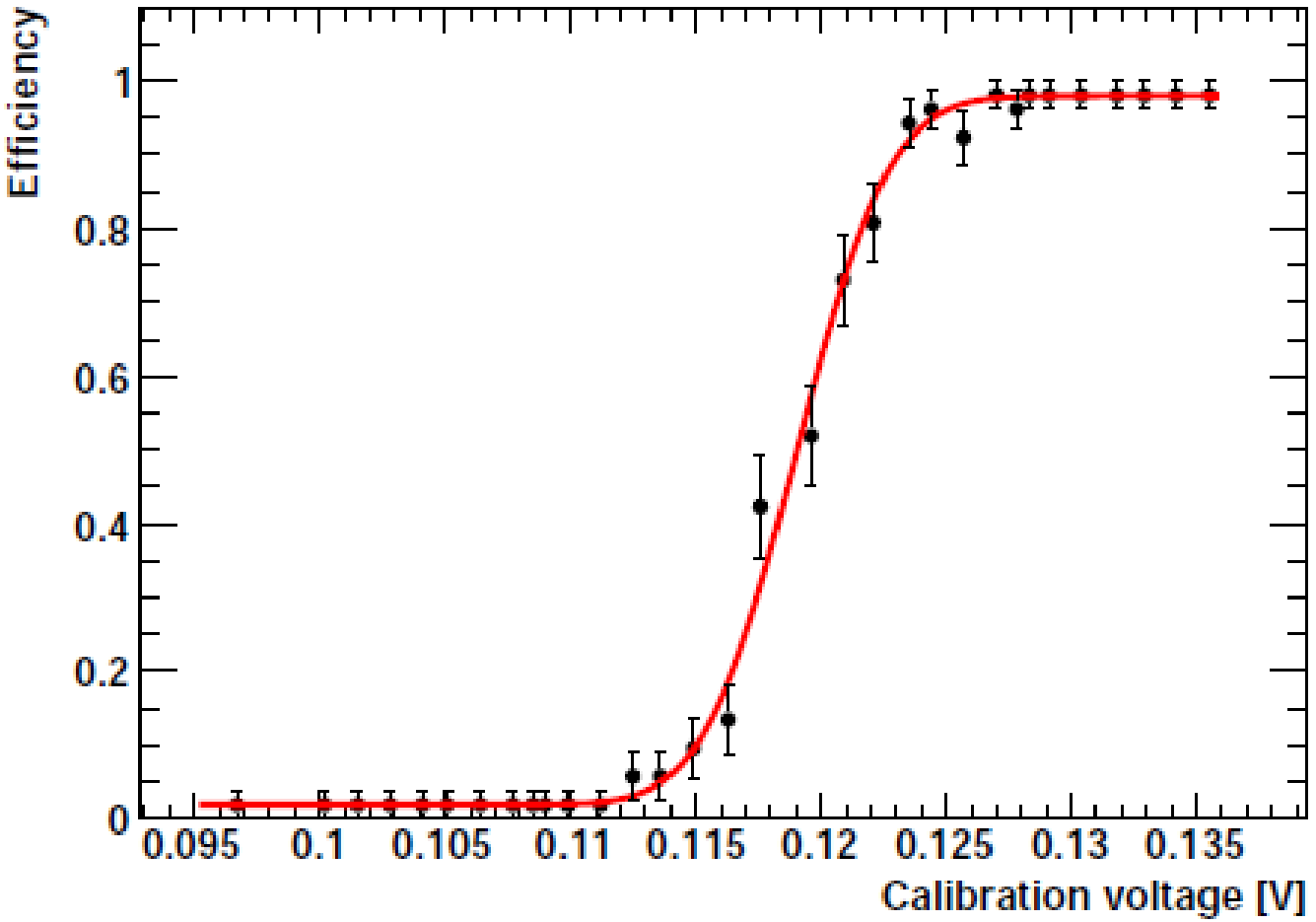
- One pixel.
- Threshold set close to noise limit.
- Window is 1 BC wide.
- We choose 125.
- Small pulses:
  - time walk.

Threshold curve



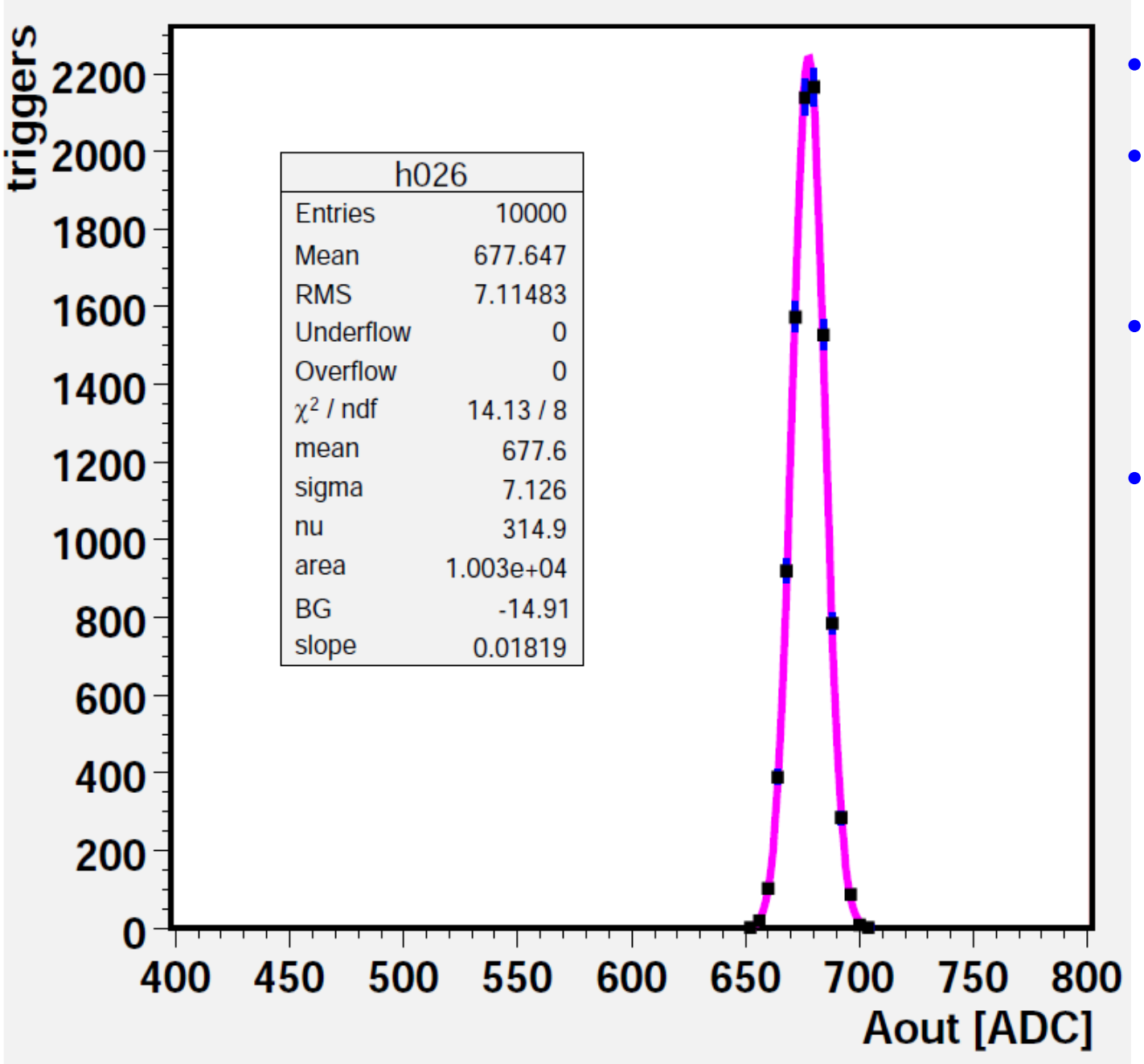
- One pixel.
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 2.1 DAC
  - = 130 electrons.
  - (bare chip without sensor).

Threshold curve at PSI



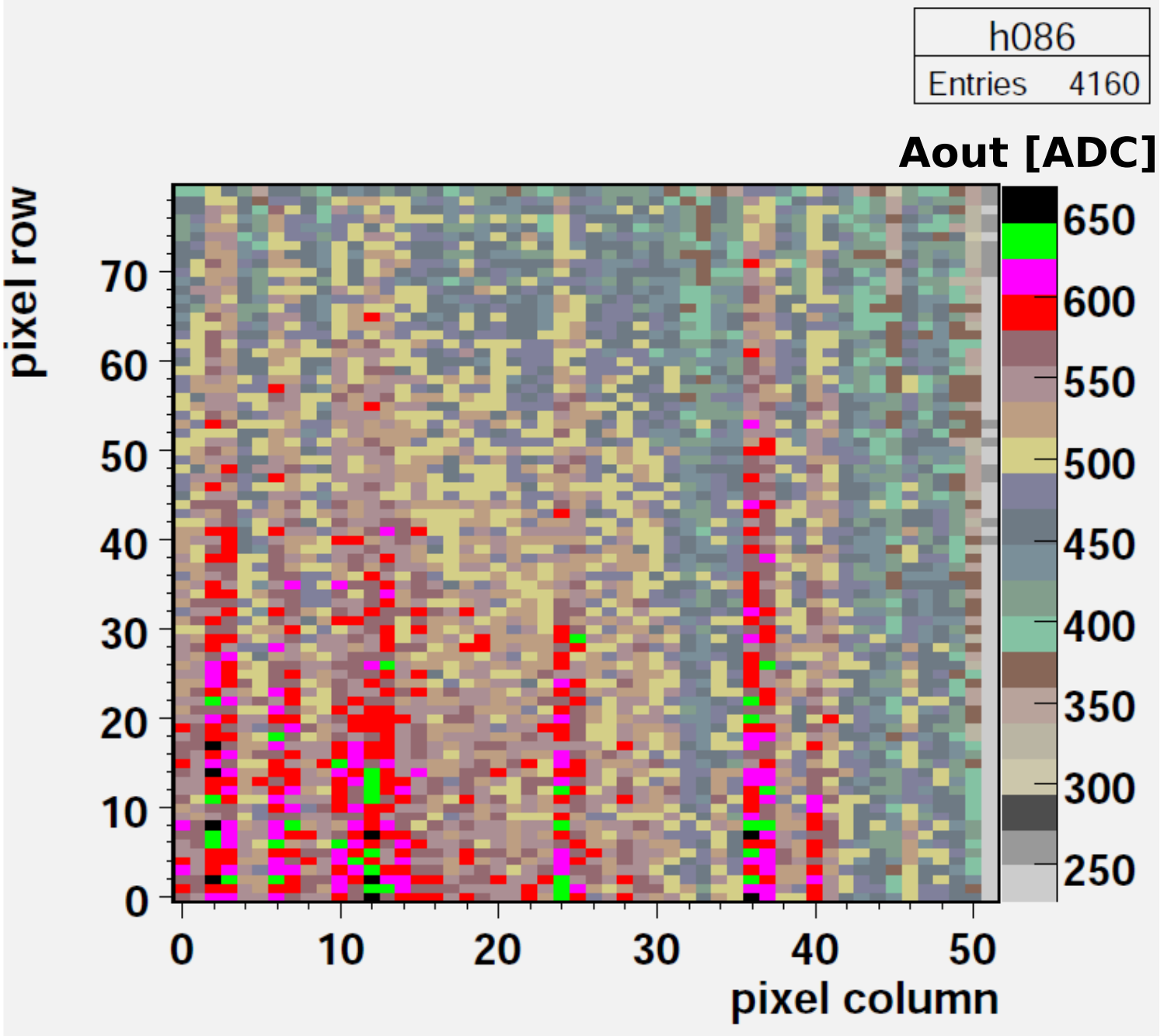
P. Trüb, ETH phd 2008

one pixel with test pulse



- one pixel.
- 10k triggers:
  - at 100 Hz = 100 s.
- Calibrate 200 small DAC = 13'000 e (PSI).
- Width = 7 ADC counts:
  - thermal noise,
  - perfect Gaussian,
  - 135 e (no sensor).
  - agrees with threshold scan!

Pixel map



- 52 × 80 = 4160 pixel per chip.
- Vcal = 200 DAC
- VthrComp = 80
- Strong pulse height variation:
  - gain?
  - timing?