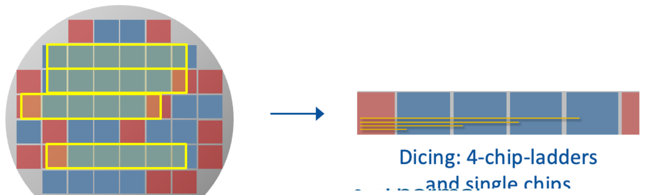
Si-D Activities Bonn

All-silicon modules for DMAPS (Bonn, TU Dortmund, Göttingen, Siegen, HLL)

Bonn: A. Ulm (PhD student), M. Vogt, H. Krüger, J. Dingfelder

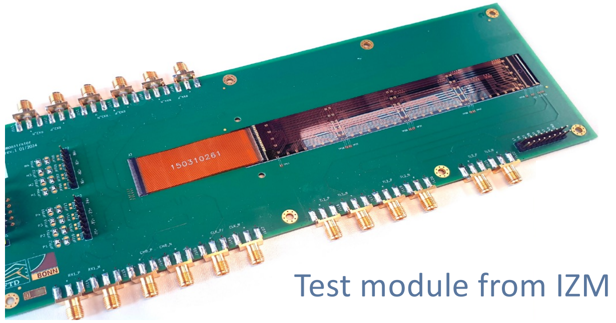
- Ultra-light module design
- Integration of power and readout lines directly on wafer (RDL)
  - Test measurements with RDL demonstrator module produced at IZM (thermal and electrical measurements)
  - Building all-Si modules at FTD: Metallization process set up (Al sputtering and etching)

All-silicon ladder approach



Dicing: 4-chip-ladders and single chips

Post-processing of ladder candidates

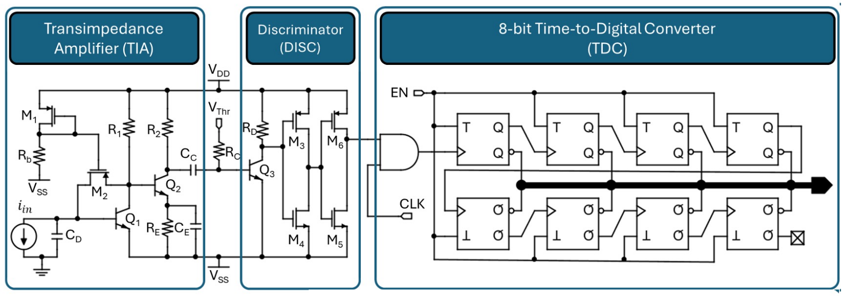


Test module from IZM

Timing with 3D sensors (Bonn, Freiburg, MPP, DESY)

Bonn: H. Krüger, J. Dingfelder in collaboration with U. Thessaloniki: A. Michailidis, V. Gogolou, T. Noulis

- Design of dedicated readout ASIC with high-bandwidth analog FE adapted to large sensor capacitance
  - 130 nm SiGe BiCMOS technology
  - First design studies
  - Tape-out of first test structures planned for summer 2025



Design/simulations by A. Michailidis