Monolithic sensors, fast electronics, and silicon photonics for future tracking detectors

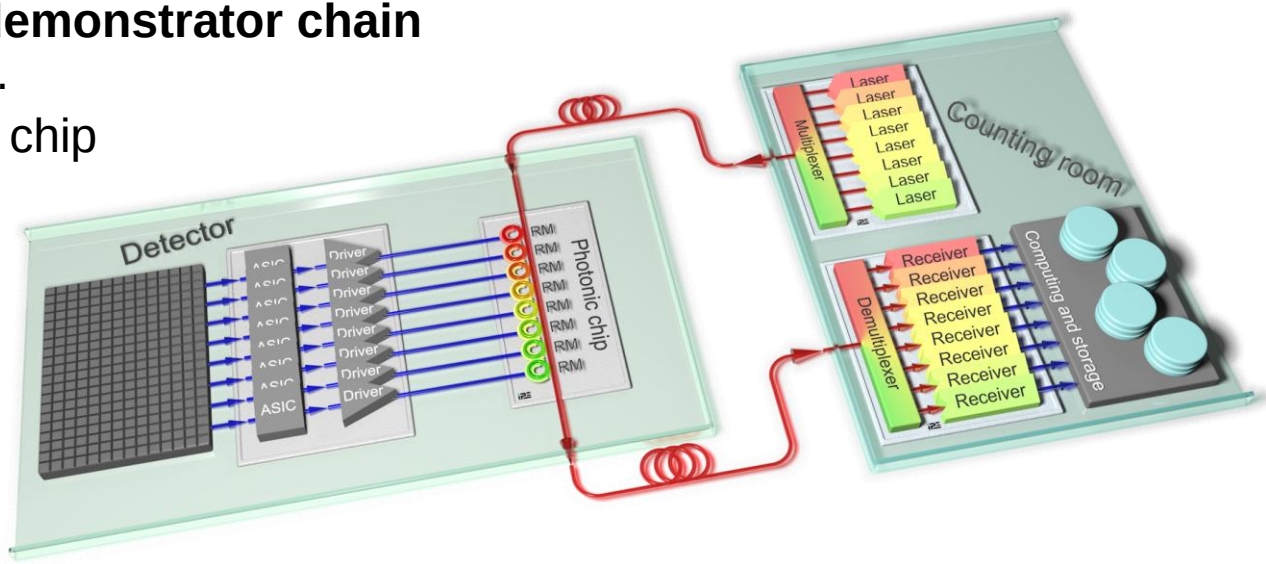
Coordination: Alexander Dierlamm, ETP/IPE
Project leader: Ulrich Husemann, ETP
MAPS: Ivan Perić, IPE-ADL
Fast electronics: Çağrı Ulusoy, IHE
Photonics: Marc Schneider, IPE

+ further experts, technicians and students…

ETP: Institute of Experimental Particle Physics
IPE: Institute for Data Processing and Electronics
IHE: Institute of Radio Frequency Engineering and Electronics

The Vision

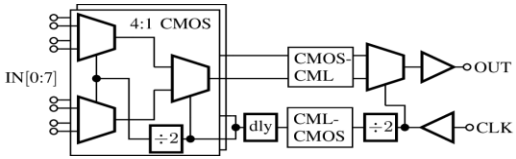
- We aim for developing an **HV-CMOS pixel detector for high particle rate** environments featuring **high-bandwidth links** together with an optical link consisting of a **driver chip** and **photonic ring modulators**.
- We want to establish a **demonstrator chain** from sensor to back-end.
- For both pixel and driver chip we want to explore IHP's SiGe BiCMOS technology

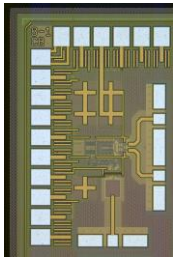


WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

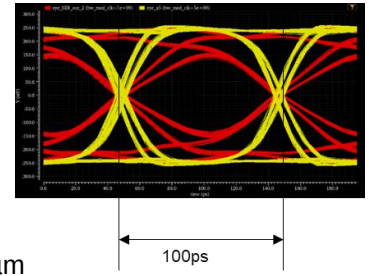
HV-CMOS Pixel Detector

- We will develop high resolution sensors (25µm x 25µm pixels) for high rates (100 particles per 25 ns and cm² = 4GHz/cm²) and a high-speed serializer aiming for 25Gbps
  - ~2 submissions of small test chips (VertexPix1, VertexPixHR)
- Current status
  - submitted a v0 test chip in IHP SG13G2 to address some readout aspects
    - 10 x 20 50µm x 50µm pixels; 1.5mm x 1.7mm chip size
    - expected back in Q1'25
  - produced a 8-to-1 serializer for 10Gbps





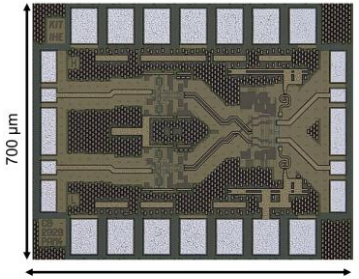
Test chip 500µm x 800µm

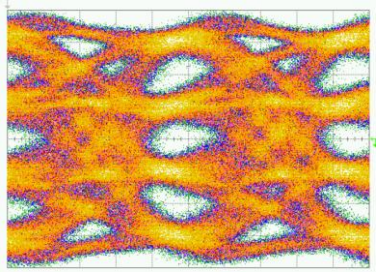


Fast Driver

- We will develop a multi-channel 4 × 25 Gbps driver for ring modulators
- Technology:
  IHP SG13G3 exploiting heterojunction bipolar transistors (HBT)
- Current status:
  - similar drivers already produced
    - Transimpedance Amplifier (TIA) for PAM-4 application
  - evaluating requirements for final driver chip
- Next:
  - x-ray irradiation of available drivers in IHP SG13G3

Example: TIA

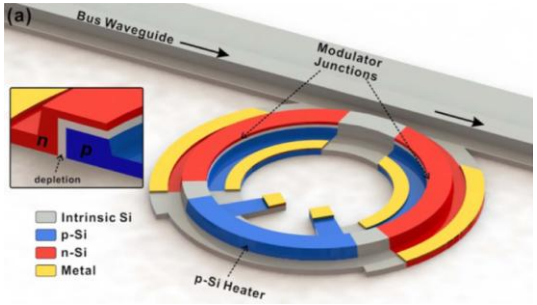


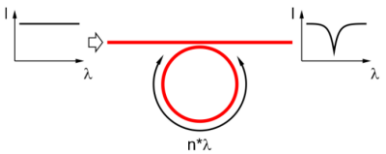


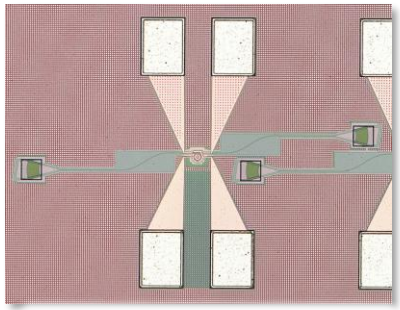
100Gbaud

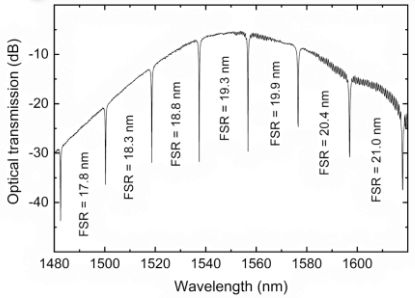
*PAM-4: four-level pulse-amplitude modulation

Ring Modulators









- Ring modulators are the most compact photonics modulators
- The bandwidth can be as large as 50Gbps using wavelength division multiplexing
- We aim for a custom design with temperature control

- Current status:
  - initial devices produced in IMEC ISIPP50G process (C-band (1550 nm ± 30 nm))
    - heater and coupling included
- Ongoing:
  - x-ray irradiation of available ring modulators from IMEC

Project Situation

- Reshaped proposed project after funding approval
- Project presented within DRD3 WP1
- Started some irradiation tests
- Next: investigate VertexPix_v0 and discuss system layout

	Q4'24	Q1'25	Q2'25	Q3'25	Q4'25	Q1'26	Q2'26	Q3'26	Q4'26	Q1'27	Q2'27
HBT irradiation											
Ring modulator irradiation											
VertexPix_0 production											
VertexPix_1 production											
Readout chain with existing driver and modulator											
VertexPixHR production											
Driver production											
PIC production											
Final chain assembled											

Spares

System Aspects

- Need to align requirements for VertexPix, driver and ring modulator to get demonstrator for up to 100 Gbps
- Assembly of chain and optical coupling
- Backend data acquisition (Serenity? developments at IPE)
- Also evaluated limits in view of radiation hardness