Quality Control of the Tileboards for the High Granularity Calorimeter upgrade of the CMS experiment

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DPG Göttingen (T 96.1 - Detector VII: Calorimeters)

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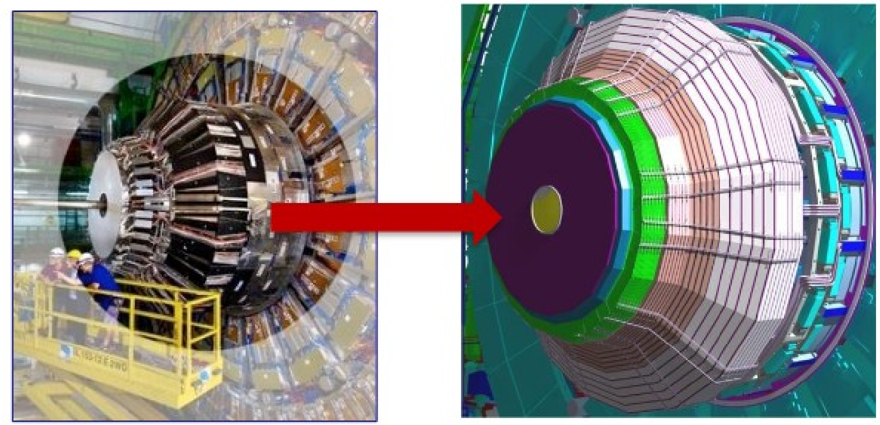
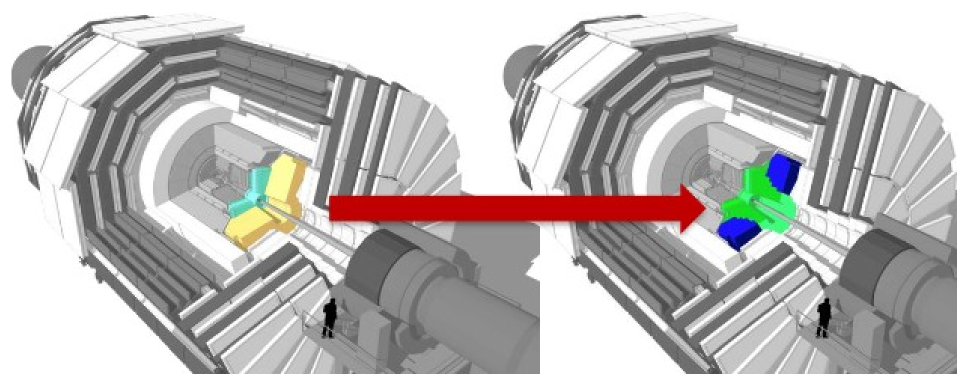
Introduction

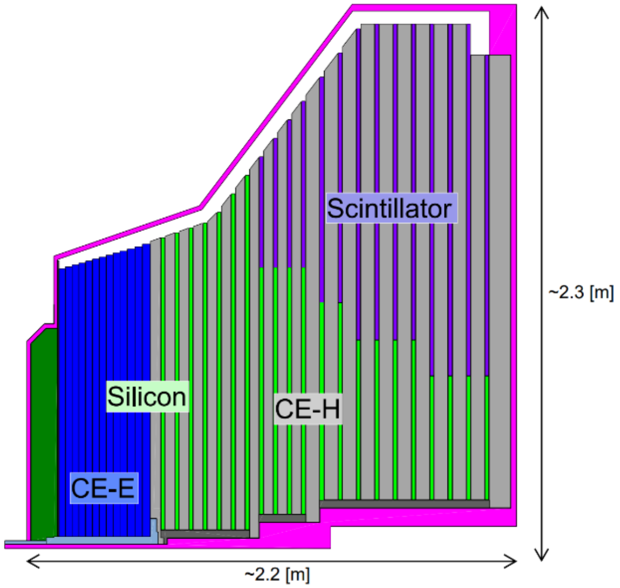
- The High-Luminosity Large Hadron Collider (HL-LHC) aims to increase the luminosity of the current LHC by a factor of ~10.
- Increased pileup and radiation. Calls for upgrade of current detectors
- CMS will be upgrading its endcap calorimeter (among other sub-systems) for HL-LHC with the new High Granularity Calorimeter (HGCAL)
- Worldwide collaboration between different universities and countries.
- HGCAL is a 5d imaging calorimeter (3d + Time + Energy)
- Consists of both an electromagnetic and hadronic calorimeter
- 2 different technologies are used in HGCAL
    - Silicon
    - Scintillator/SiPM-on-tile technology

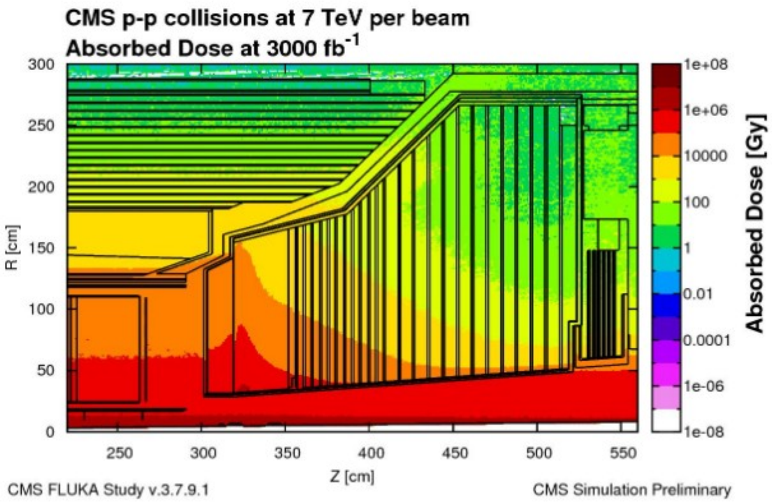




Why Scintillator technology

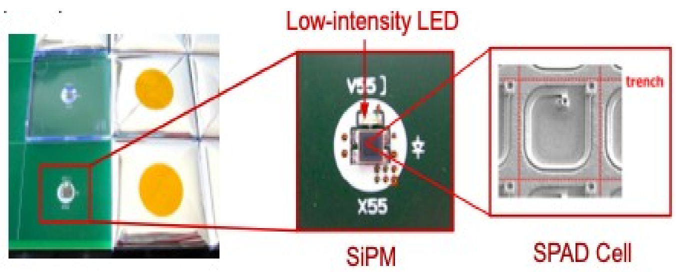
- Adapted and benefited from vast experience and R&D done for the Calice collaboration
- Different radiation rates throughout the endcap regions of the calorimeter
- Scintillator technology used towards the back where lower radiation doses are expected
- Allows reduction of overall costs
- 16 scintillator layers, ~4000 boards and ~280,000 channels



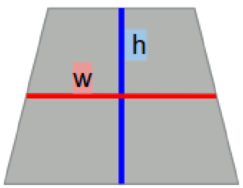


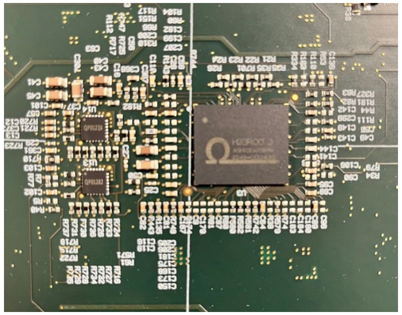
SiPM-on-Tile Technology

- The scintillator tiles are trapezoidal (considering the geometry of the end-cap region) shaped plastic wrapped in reflective foil.
- Optically linked to silicon photo multipliers (SiPM) making them SiPM-on-tile.

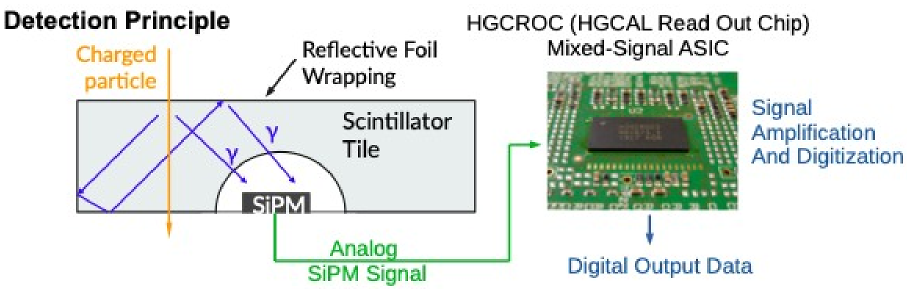


SiPMs consists of thousands of single photon avalanche diodes (SPAD) working in Geiger-Mode





- Signals are sent to the HGCROC (High granularity calorimeter read out chip) for signal amplification and digitization before being sent out to the backend.
- HGCROC has 72 channels and there are 1 or 2 chips per board.
- Output => ToA and (ADC or ToT)



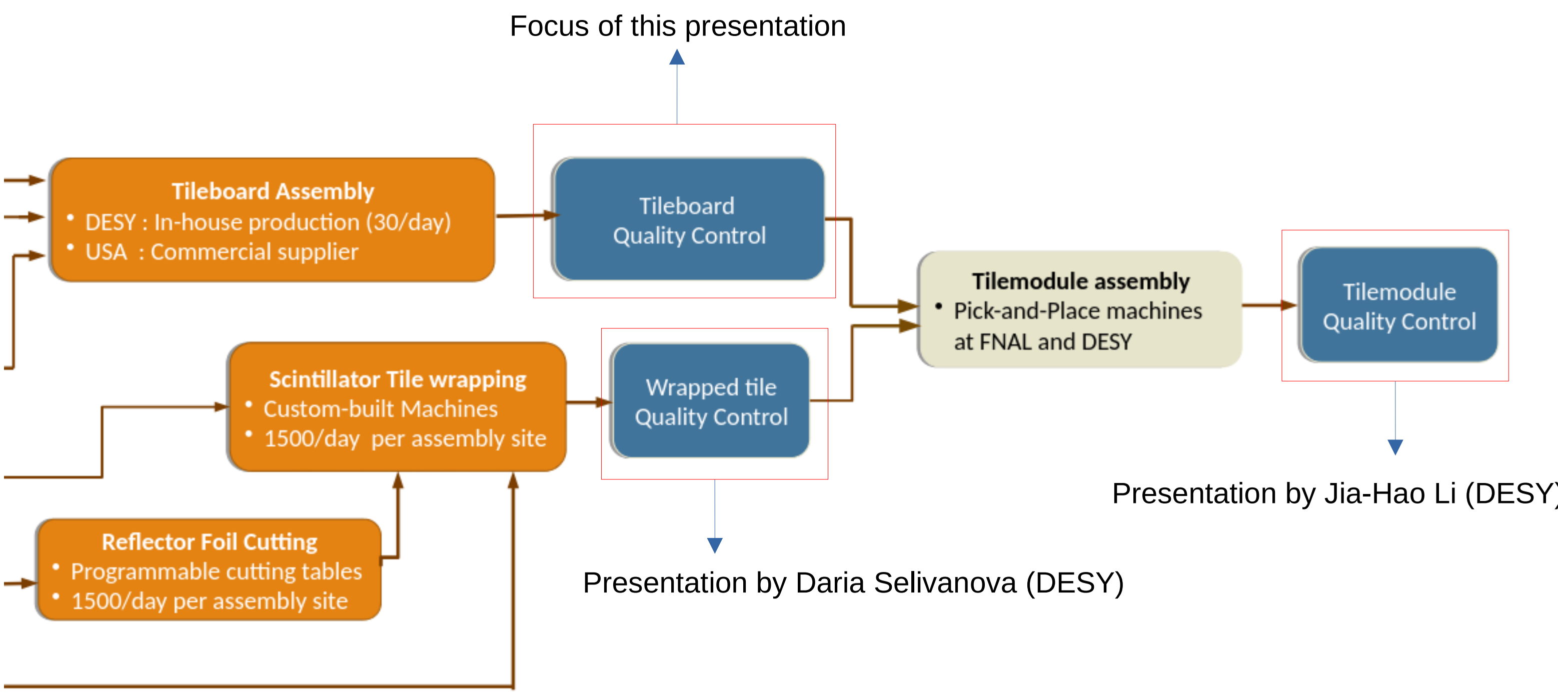
Small aside: Jargon

- Tileboard = PCB + electronics
- Tilemodule = Tileboard + tiles
- DESY is one of 2 assembly centers for the tileboards and tilemodules, hence a natural center for testing the assembly.
- The first step in Quality control will be to test the tileboards to make sure the electronics are working before placing the tiles.

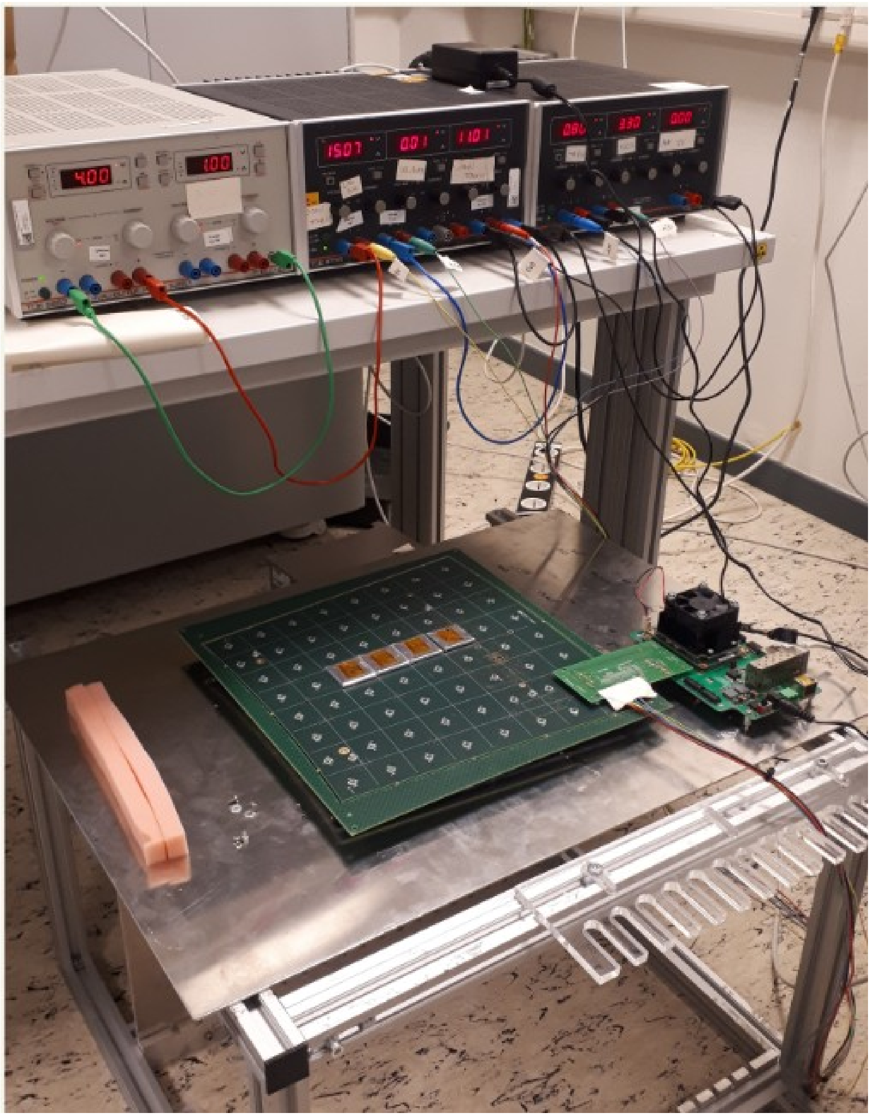
- Tileboard

- Tilemodule

Flow of QC procedures



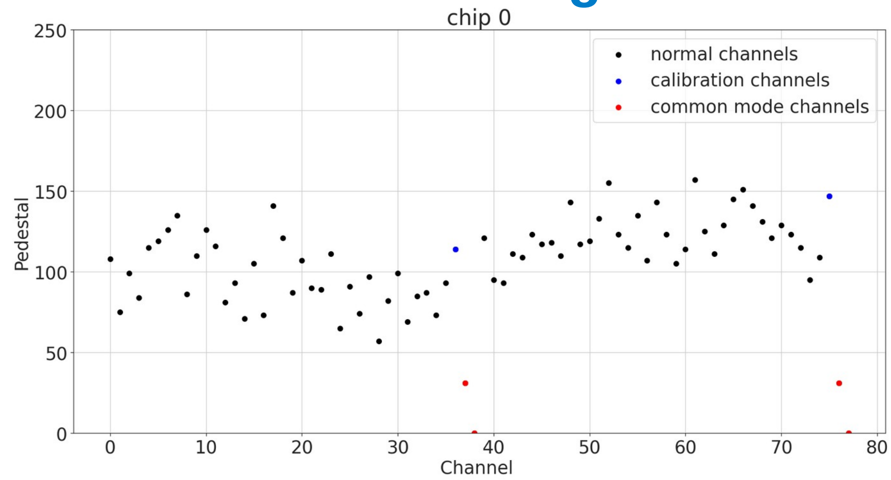
Goals of Tileboard Quality control (QC)



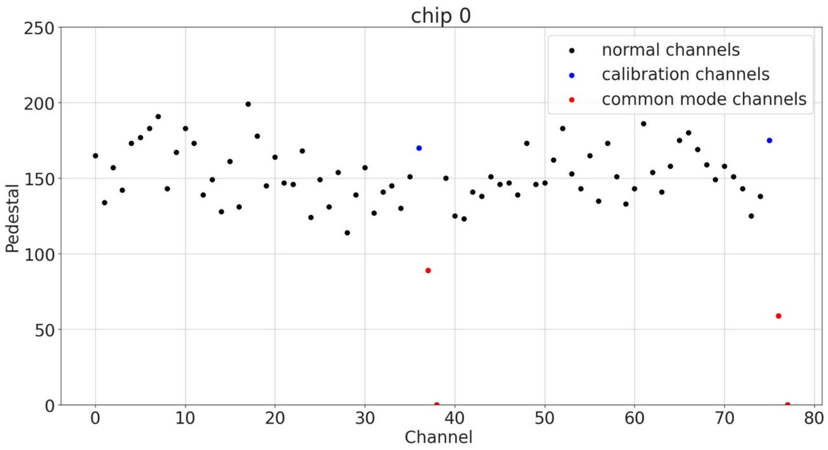
- Once the tileboard is assembled its functionality needs to be checked
  - Have to check if one can set parameters to the HGCROC and read out the data
- Large number of parameters to tune (~300 per chip)
- Additionally one has to check that the SiPMs can see light using the on board LED.
- With all the data taken one can also perform an initial tuning of the board.
- So the **QC test stand** also acts as **the initial tuning stand**.

Example: Pedestal tuning

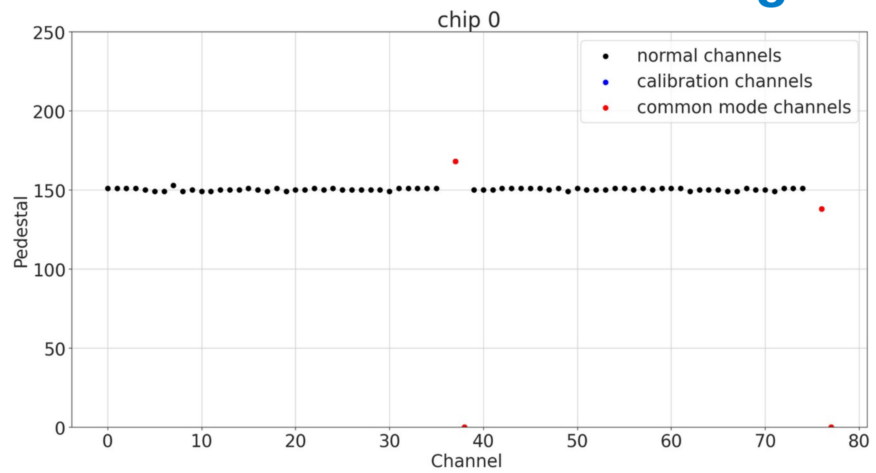
No tuning



Global chip alignment

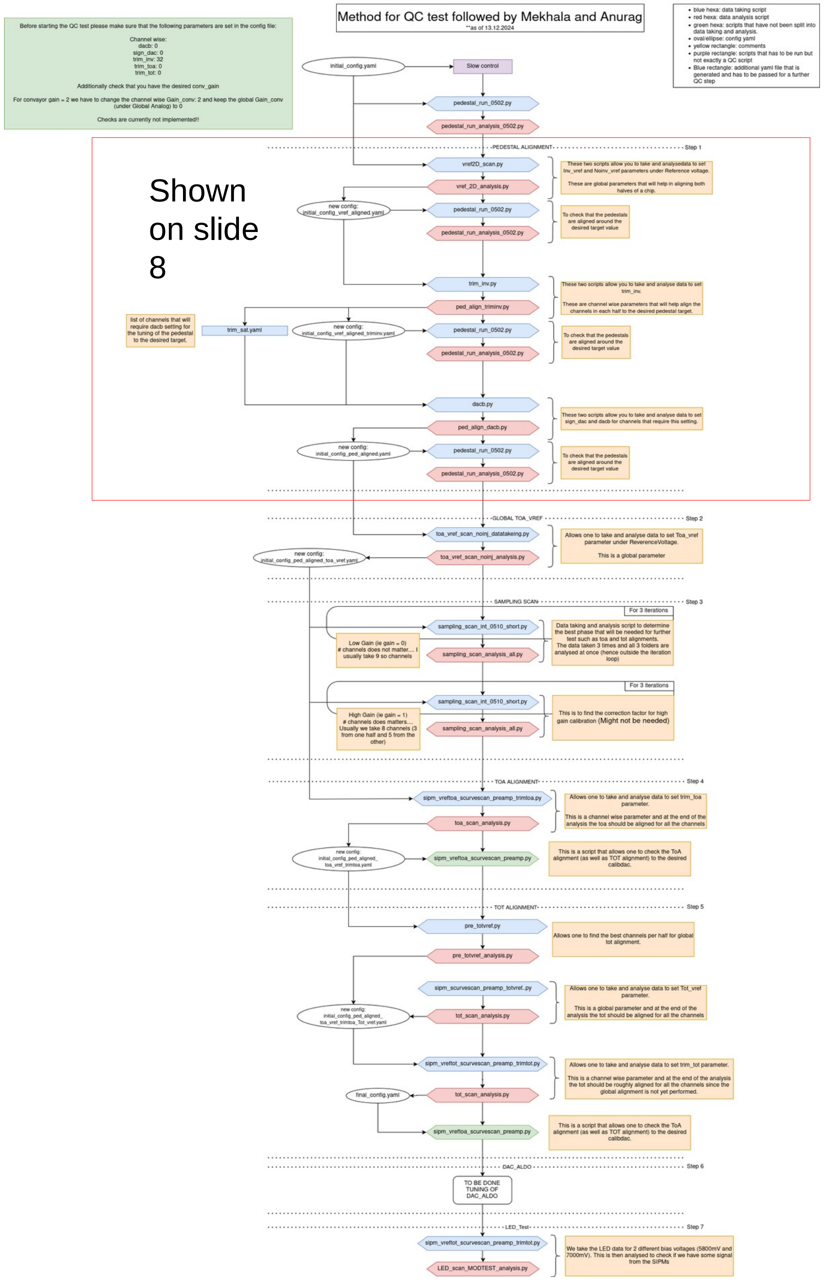


Final channel-wise tuning



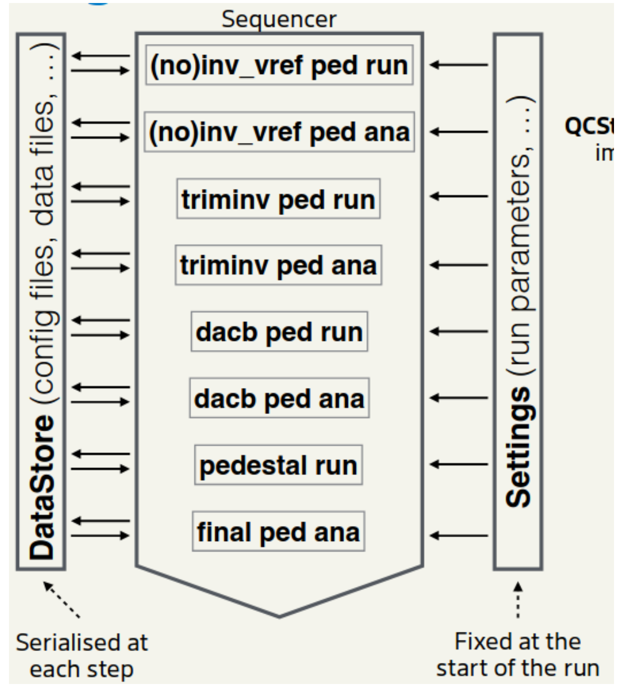
Towards Automation

- **~4000 boards** have to be tested worldwide.
- **Designed to be modular,** allows extra analysis without having to retake data everytime. Also easy to check analysis by re-running only the steps needed and not the full procedure.
- Should account for most of the expected failures and allow for simple instructions to recover tests so that **non-experts can also operate the test stand.**
- Should provide reports
  - Detailed to be stored internally:
    - Which channels are bad or sub-standard quality
    - What parameters cannot be tuned properly for said channel
  - Higer level reports for cms database
    - Dead channels
    - If the board passes the QC or not
    - Initial tuning parameters



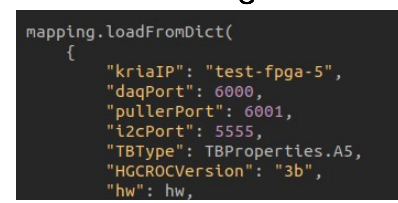
Building the Code

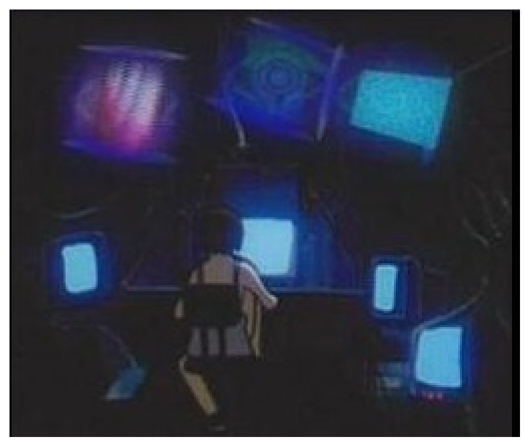
- Aim: create a comprehensive qc procedure
  - can be used by non-experts.
  - Provides debugging tools for experts
- Requires an efficient and easy to understand set of scripts for developers since this is a worldwide collaboration.
- Ensure modularity of the design and standard coding conventions.



Sequencer

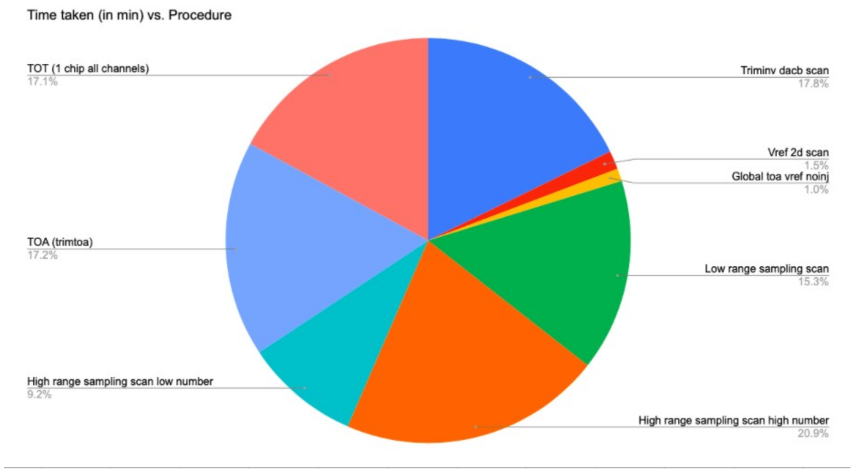
Settings





Optimization of Runtime

- Need to test **150 boards** per month. (~ 8 boards per day)
- **Target: ~ 30 mins - 1 hours per board**
- Current benchmark: ~ 1 – 1.5 hours per board
- Optimization stratagies:
  - Reduce number of events taken
  - Optimizes scans to regions of interest/signal
  - Reduce grid scan size. For example:
    - ToT scan: 8 points to do a linear fit…
    - Can reduce this to 4 points



Summary and the Future

- Basic framework of the QC procedure is now in place
- Further optimization is necessary to meet timing requirements
- Development of GUI in progress:
  - Much more intuitive to understand withouth knowing the code details
  - Much easier to teach new colleagues about the procedure
  - Reduces potential mistakes that may come from using a computer terminal

Thank you

Contact

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