BCM1F TDCs STATUS

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DESY

Cms/Fcal Meeting, 07.09.2011

Readout

Read Output Buffer error – new board!

- On 15 August after TDCs were restarted due to exchange of power supply an error started to appear very frequently

  [ERR:TDC_V767_CAEN-BLTRead_Output_Buffer] Read Error!

- After various tests and checks the conclusion was that the board needed to be replaced!

- Thanks to Elena, the TDC board was changed last week, a new spare was taken from the pool and installed in the so-called gated crate.

- Tests with both boards were performed from Hamburg with the help of Elena in S1…

Readout

Tests with the new boards

- Both boards running much more stable than the previous one.

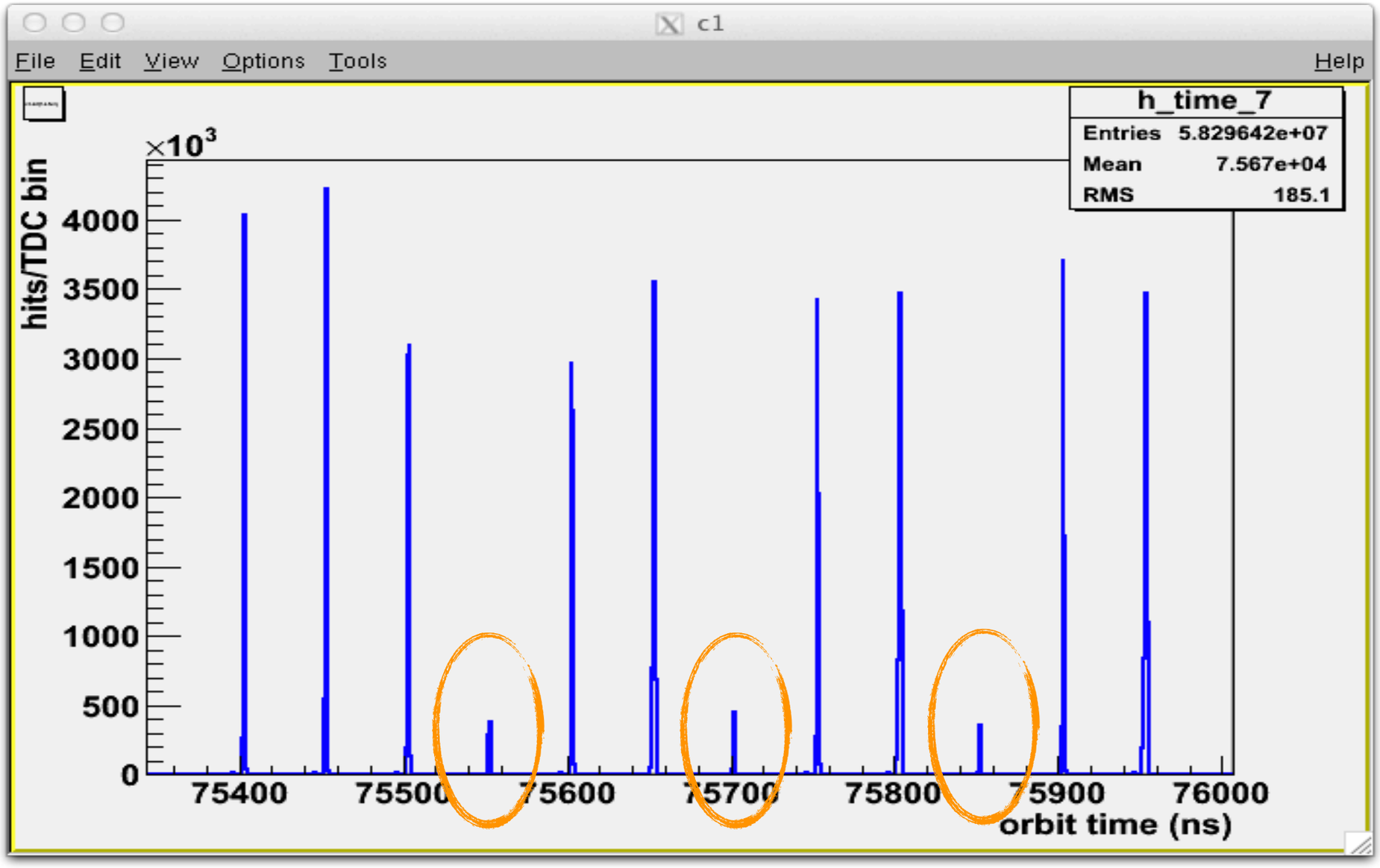
- **[ERR:TDC_V767_CAEN-BLTRead_Output_Buffer] Read Error!** still appears and exactly twice, few minutes after the readout starts(???)
  - Seen also in the gated crate!!!

- A test was ran over the weekend: only the two errors after the readout was restarted appeared since Friday, 02.09, afternoon :) until Thursday, 08.09, when high lumi beams came.

Data

Pulse generator (I)

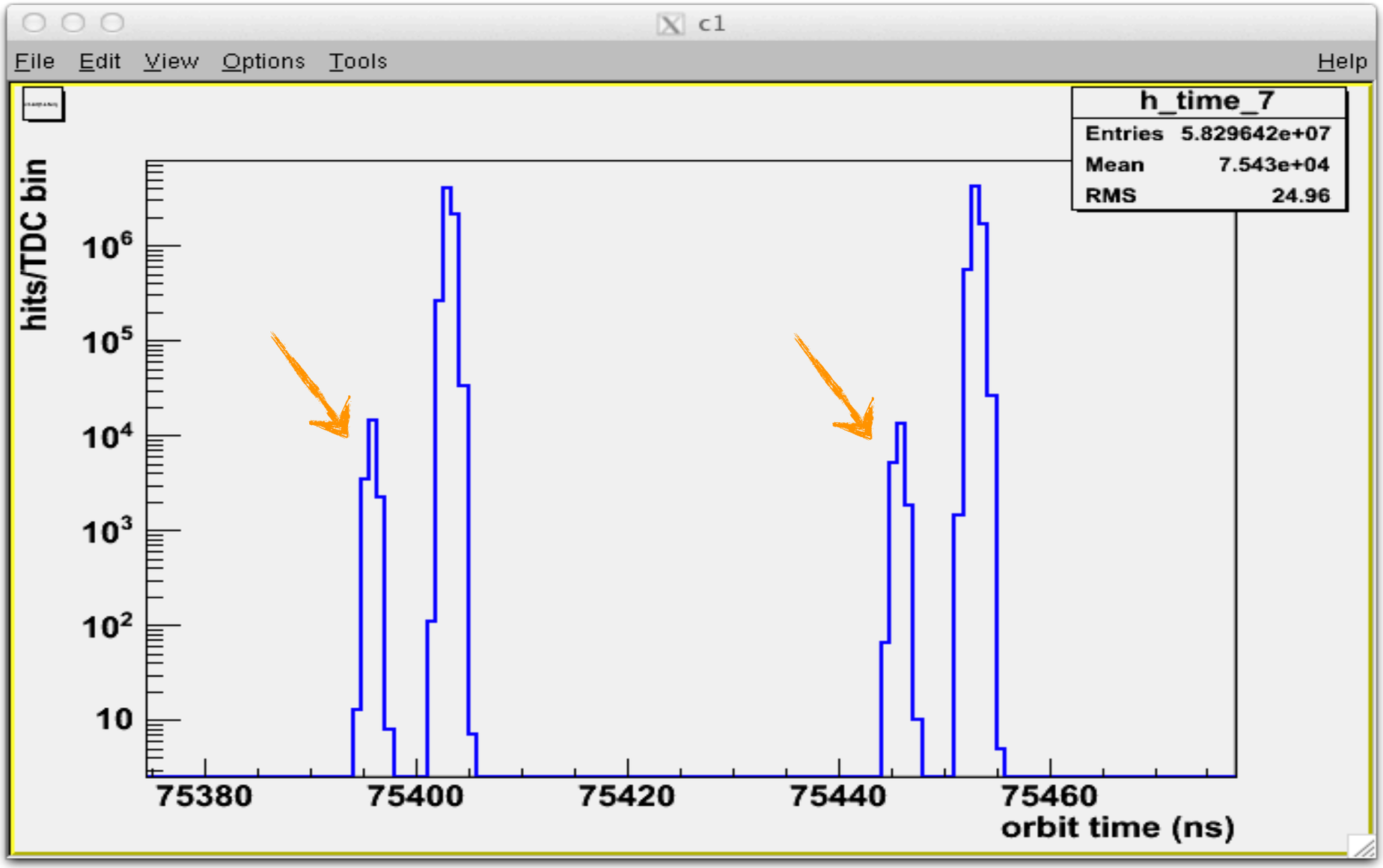
- One of the tests were done with pulse generator with pulses spaced by 50 ns.



Data

Pulse generator (II)

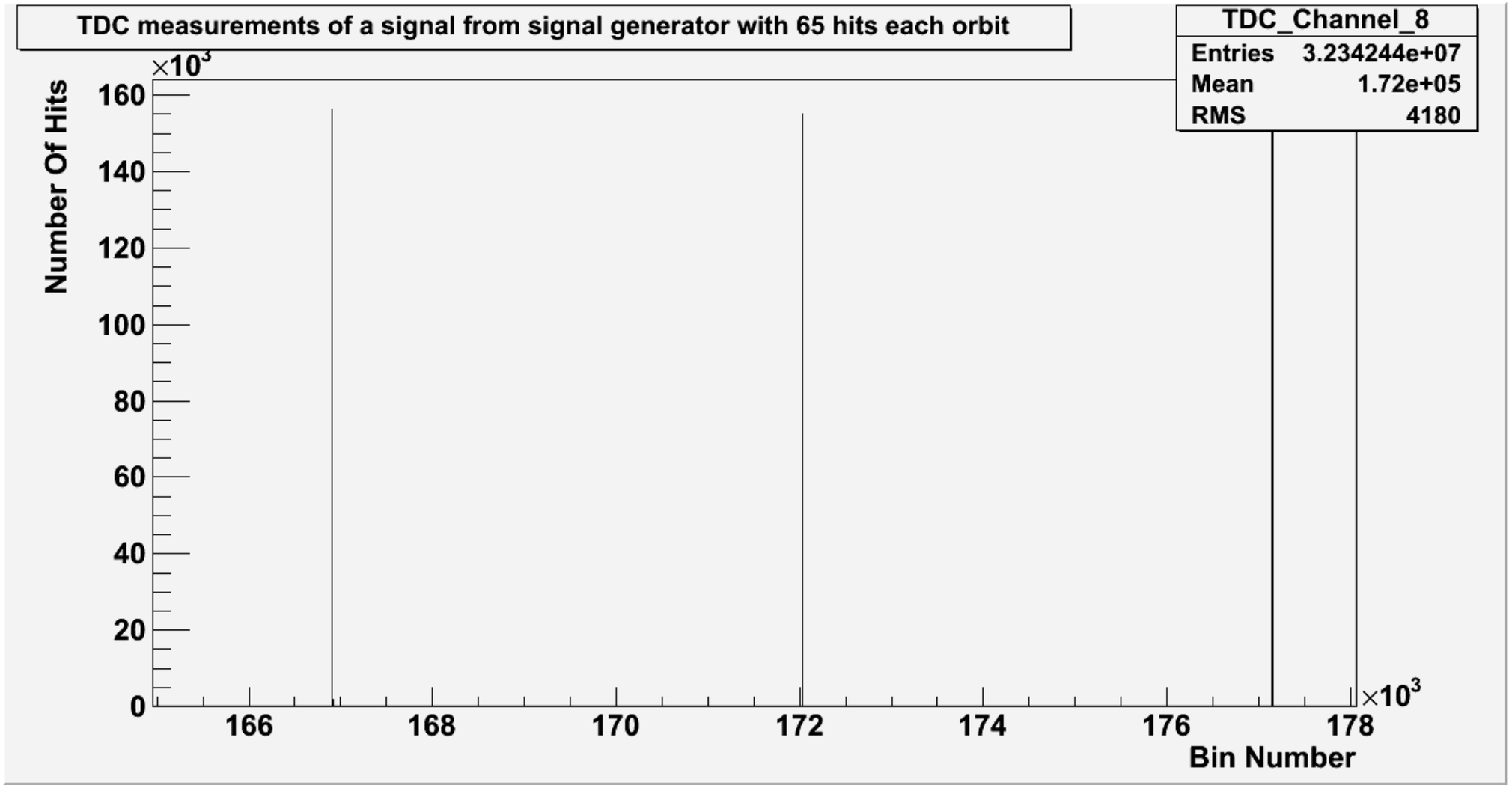
- Strange small peaks 10 ns earlier then the main peaks ??? with BOTH TDC boards tested!



Data

Pulse generator (III)

- *Strange small peaks 10 ns earlier then the main peaks NOT seen in the gated crate with a TDC 1290 – by Anne et al.*



Data

Beams (I)

Sat 03.09.11: 12h-14h
NO collisions

- Beams from LHC over the weekend after TS.
- Scheme:
  Single_2_1_1_1_wp

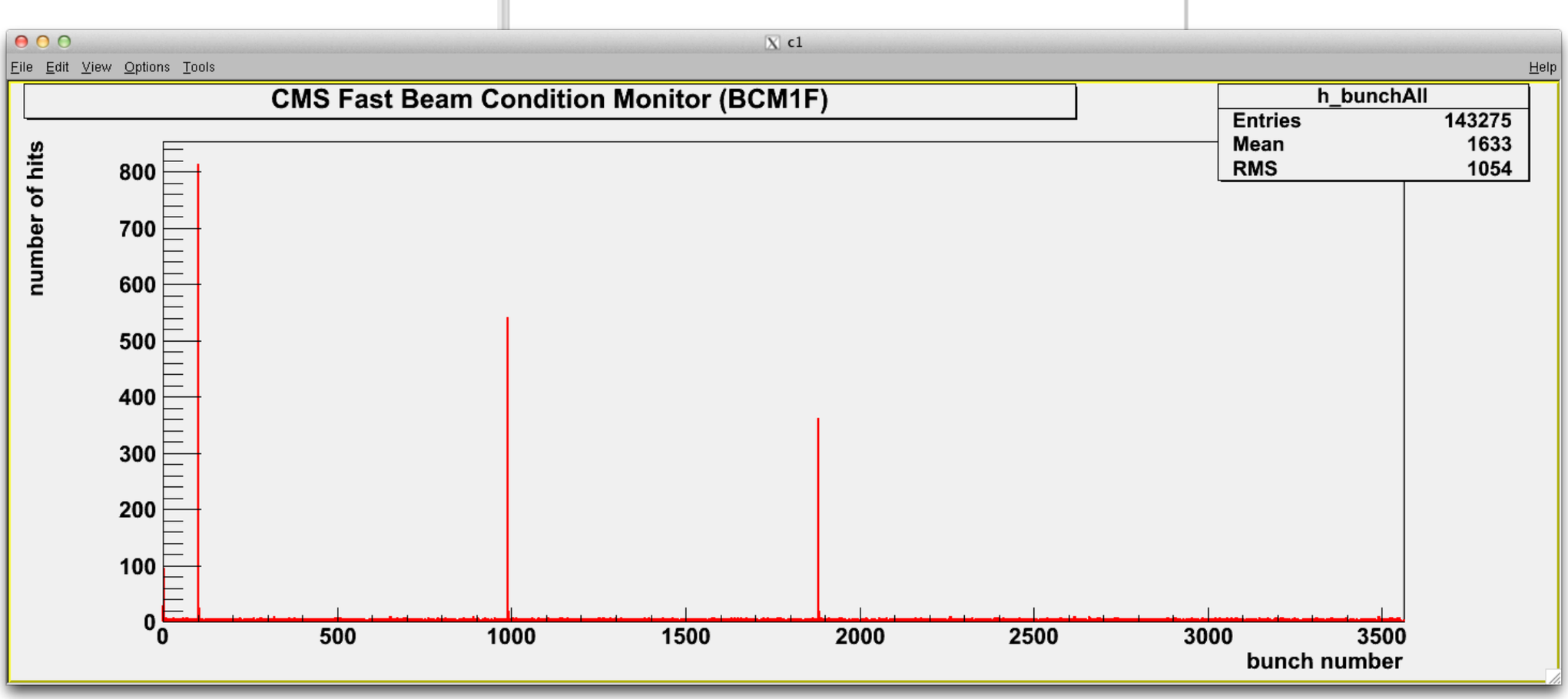
General Info | Bunch Configuration | InjectionSequence | HEAD-ON COLLISIO

Bunch config B1

Bunch...	Bucket...	dist from previous (ns)	dist from next (...
1	1		2500.0
2	1001	2500.0	44625.0
3	18851	44625.0	

Bunch config B2

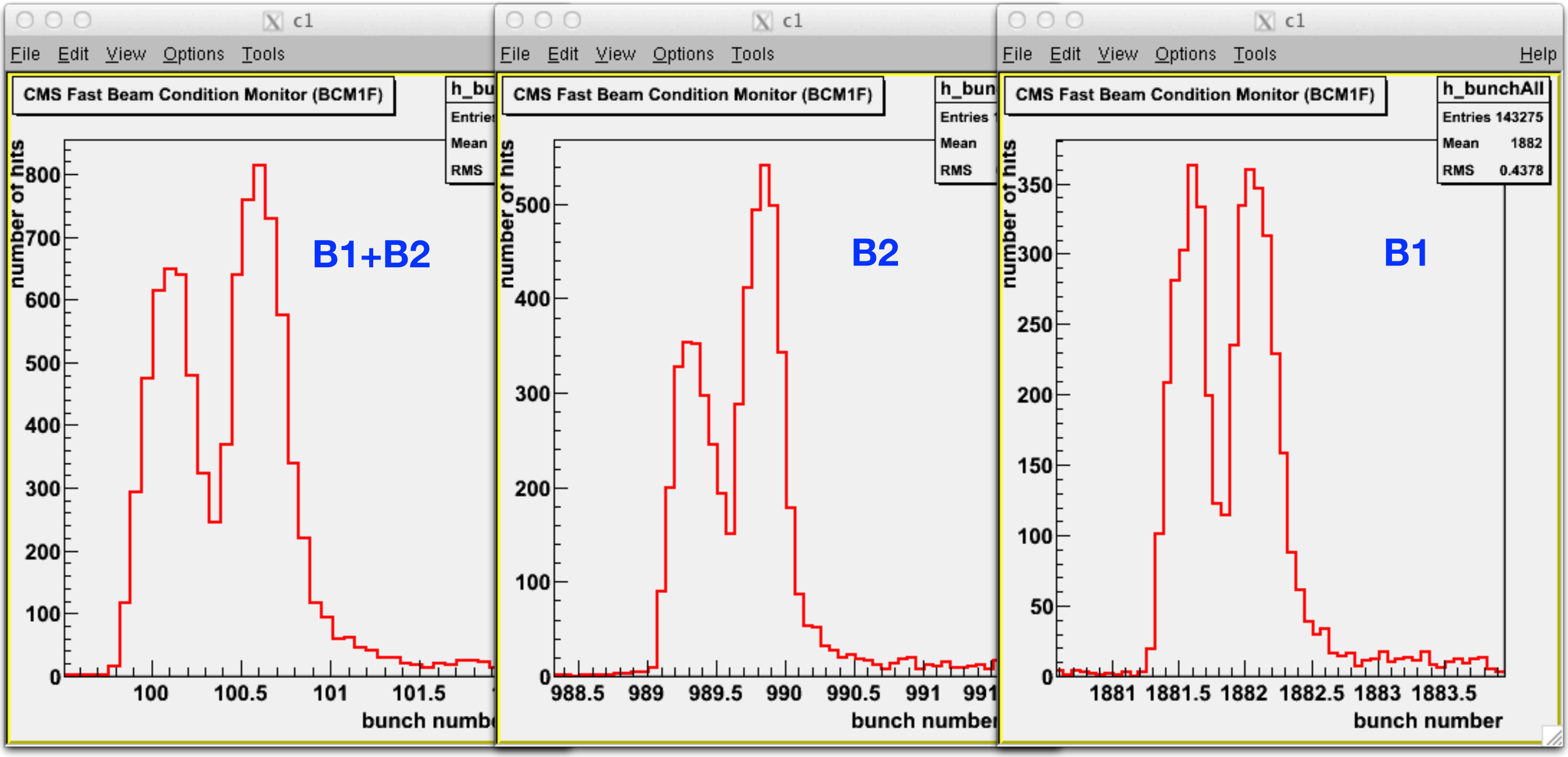
Bunch...	Bucket...	dist from previous (ns)	dist f
1	1		2500
2	1001	2500.0	2227
3	9911	22275.0	



Data
Beams (II)

Sat 03.09.11: 12h-14h
NO collisions

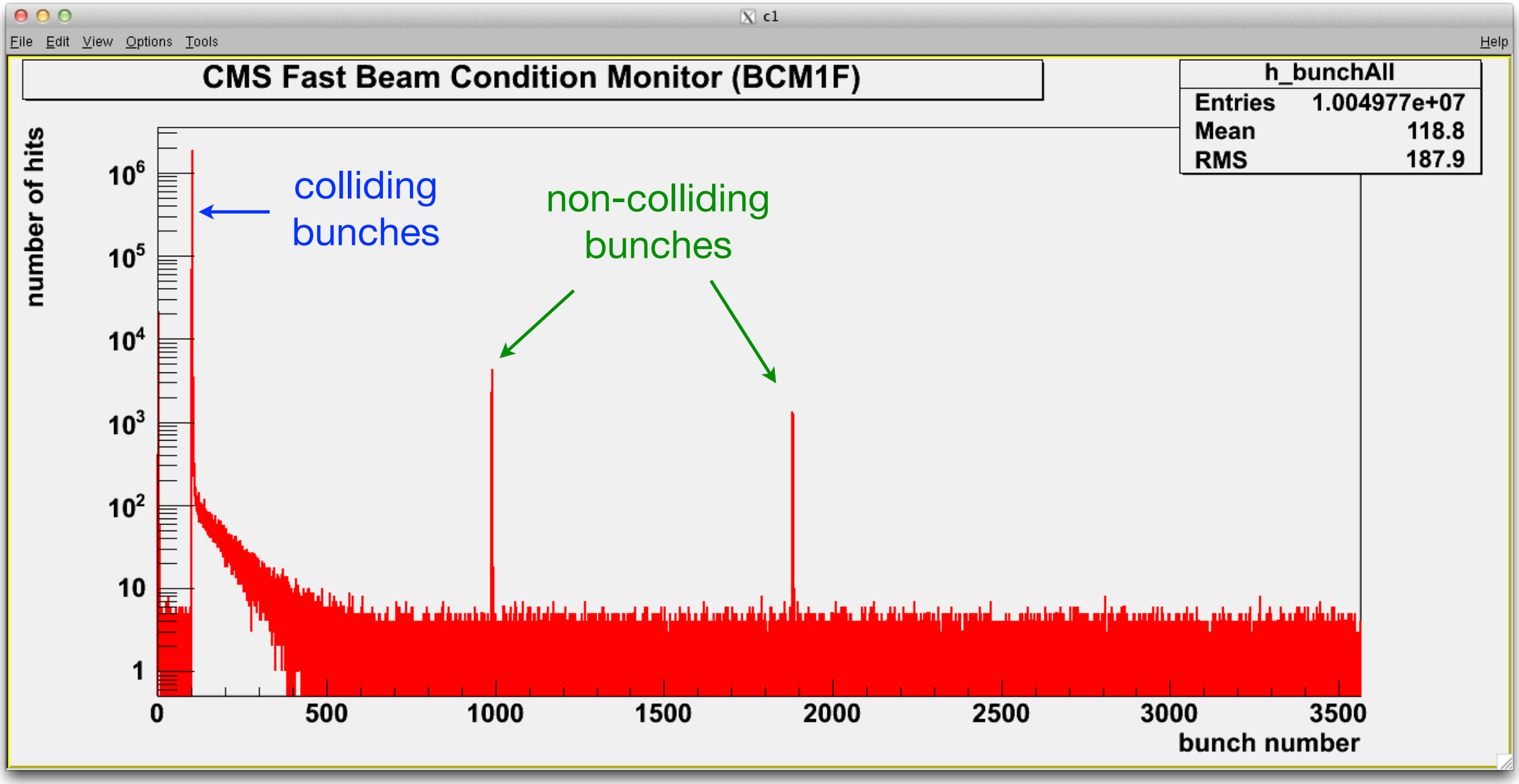
- Zoom… Resolution seems to have improved ~3ns!



peak position slightly off! need calibrate reference

Data
BEAMS (III)

Sat 03.09.11: ~18h-19h
Collisions+collimator setup



Data

Beams (IV)

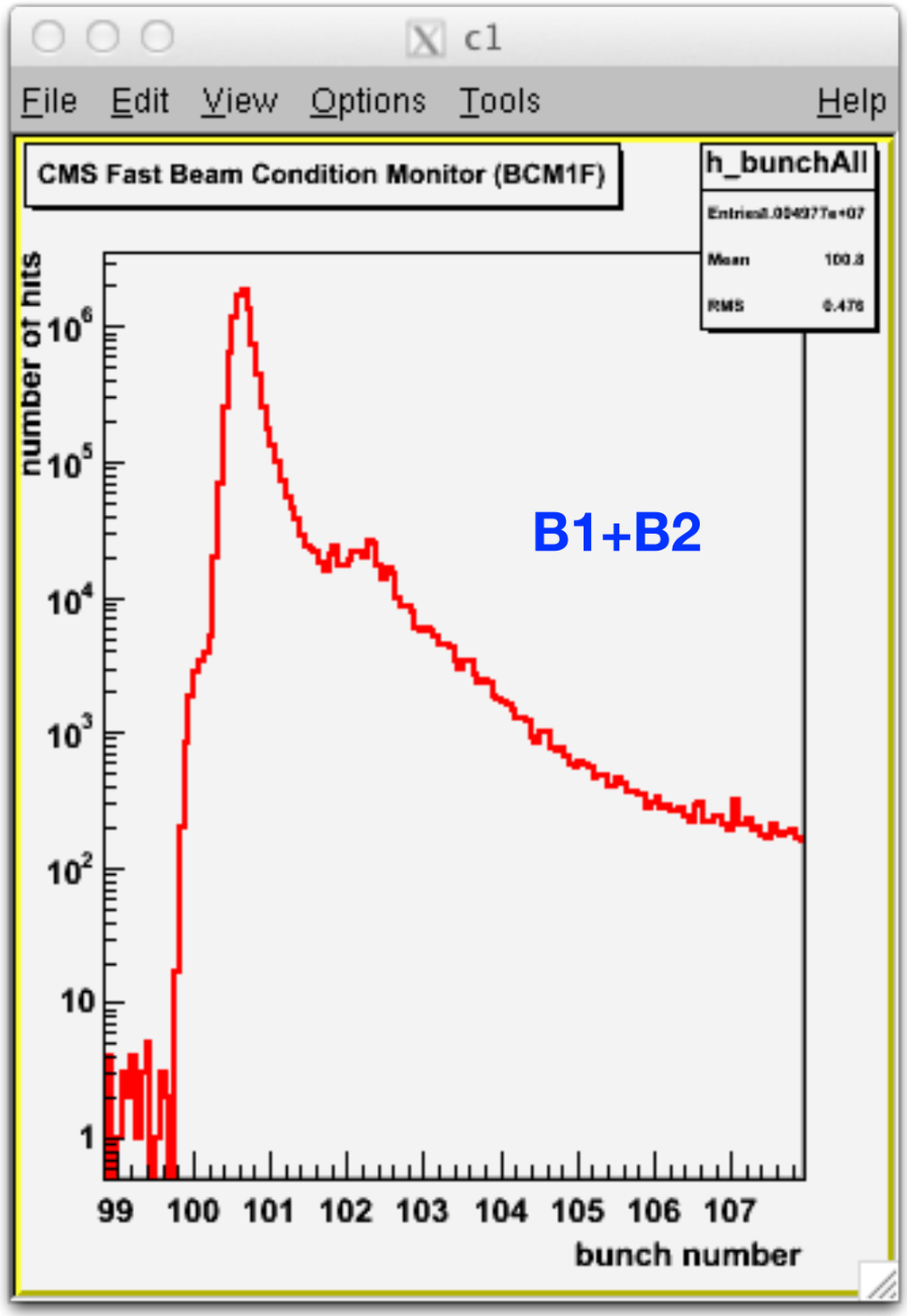
Sat 03.09.11: ~18h-19h
Collisions+collimator setup

- Strange bumps bumps before and after collision peak.

- Not able to say whether instrumental or from machine studies.

- Not enough raw data (prescaled) to do a scan.

- Seems to affect non colliding bunches too…

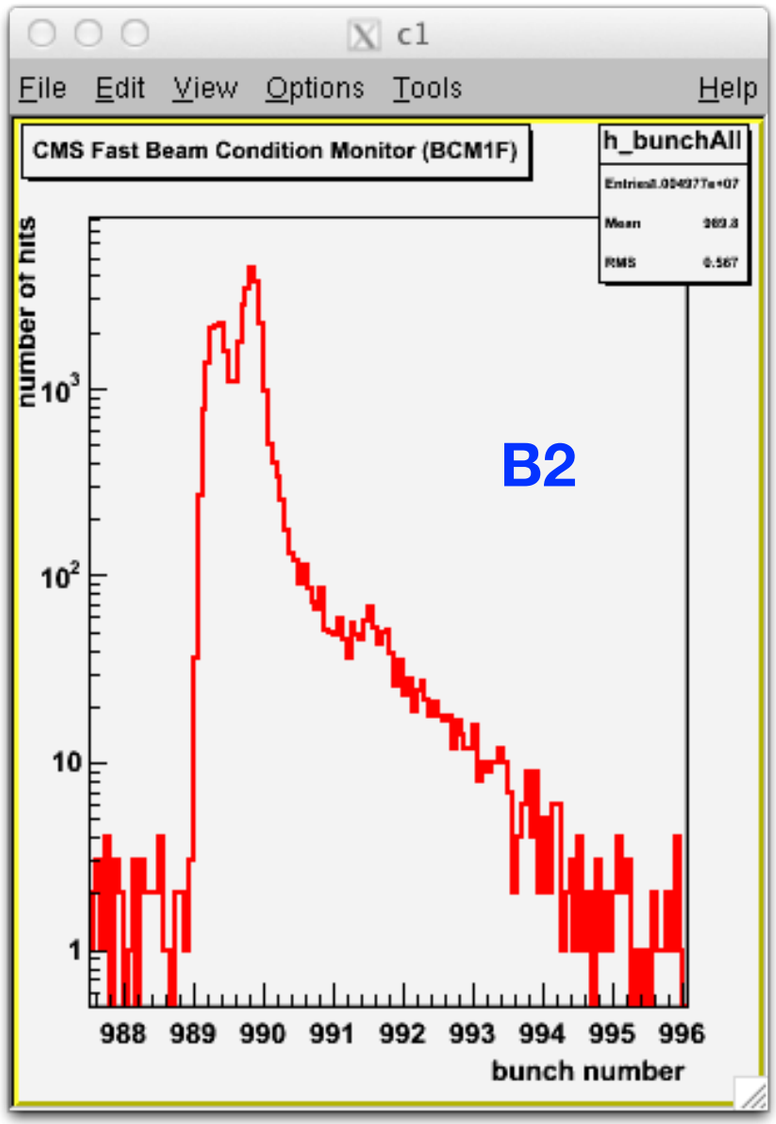


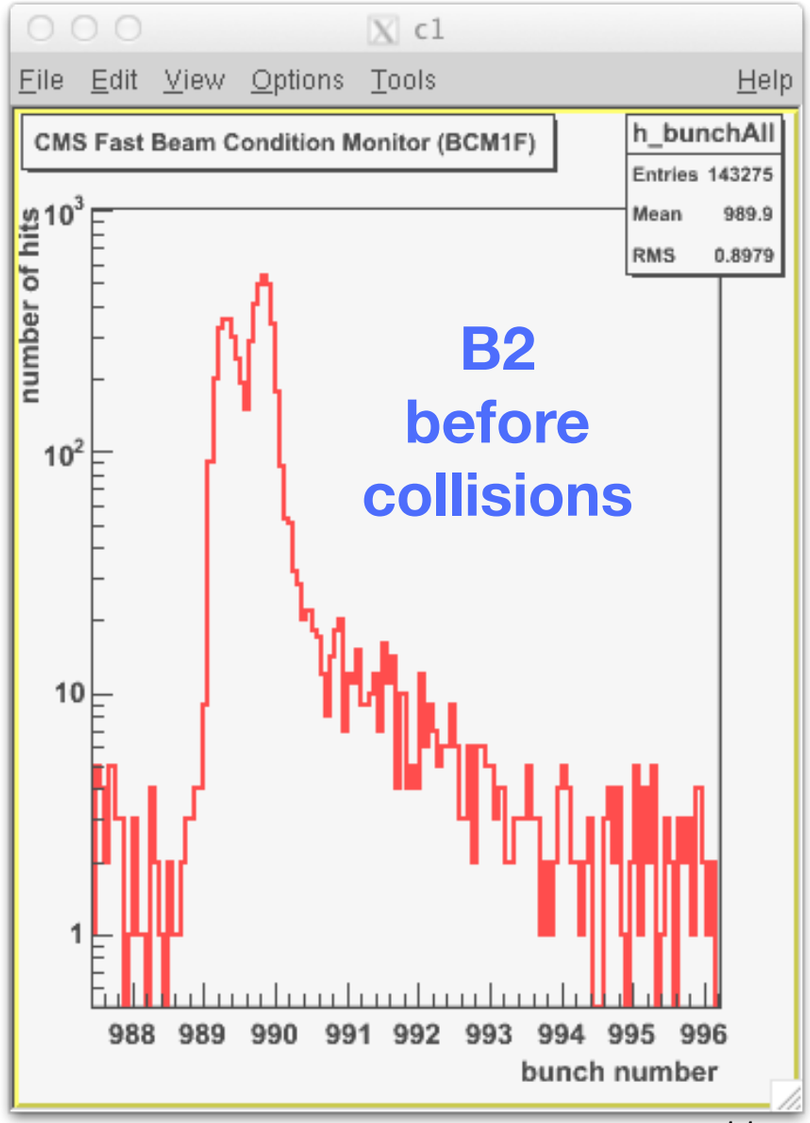
Data

Beams (V)

Sat 03.09.11: ~18h-19h
Collisions+collimator setup

- It is difficult to tell if the bump was there before collisions due to low statistics. But notice that the rates were higher during collisions:
  1 hour of data during collisions versus 2 hours of data before collisions.



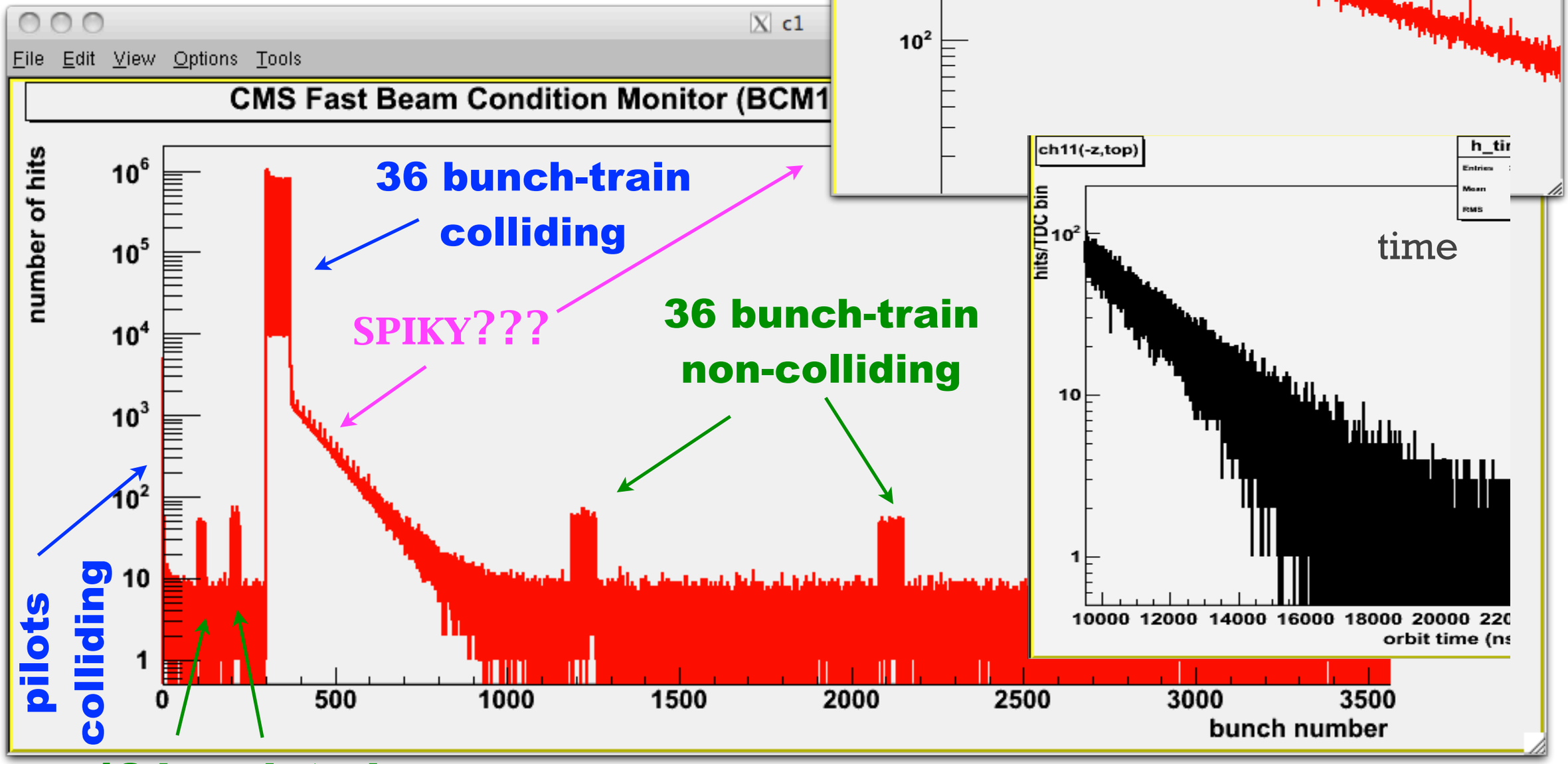


Data

Beams (VI)

- Scheme???

Tue 06.09.11



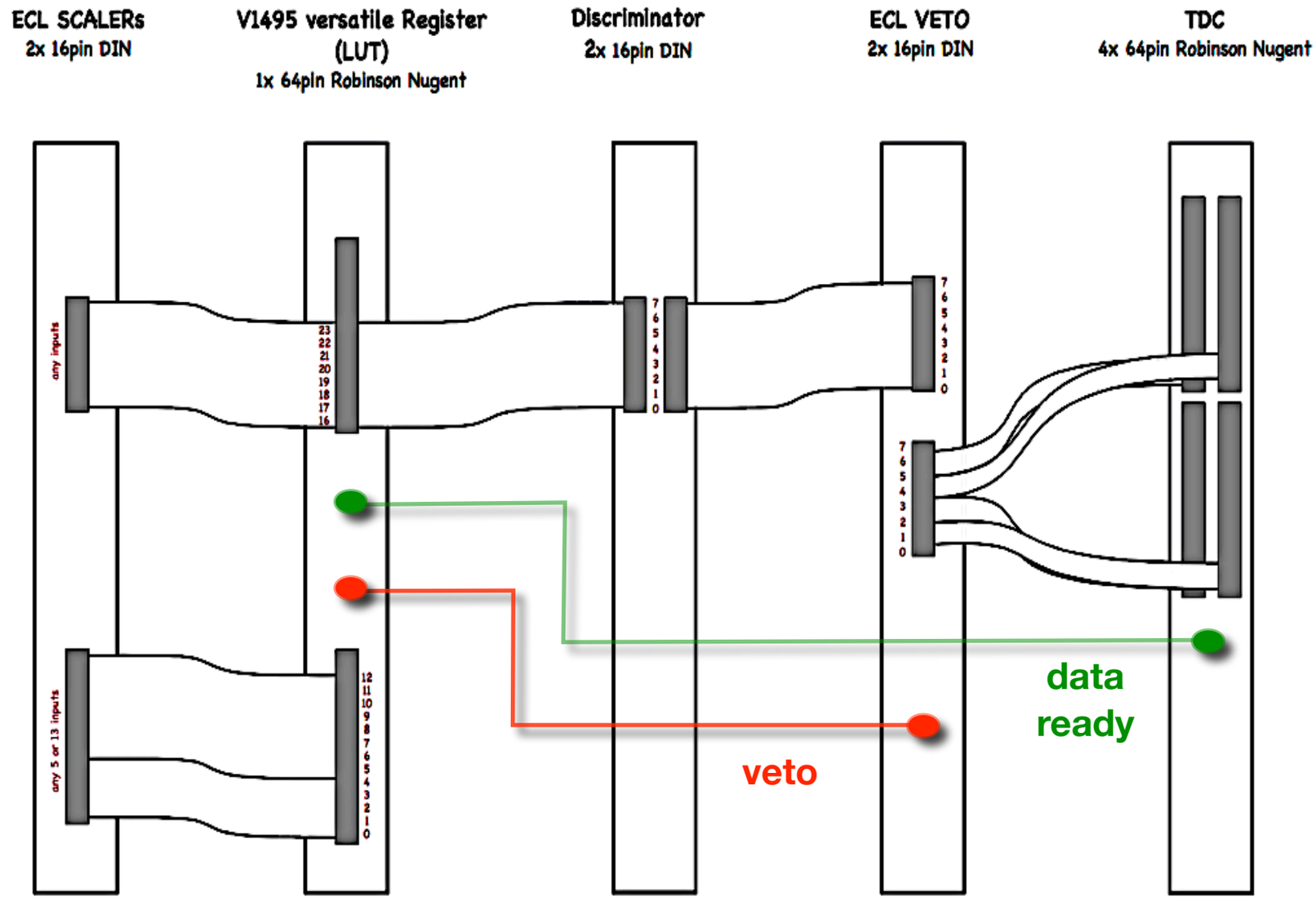
High rates

DAQ

- Almost everything that could be done in the DAQ to avoid problems at high rates is implemented.

- Signals, but NOT the start signals (orbit trigger), are vetoed during readout.

- **Vetoing is done via a fast hardware signal.**

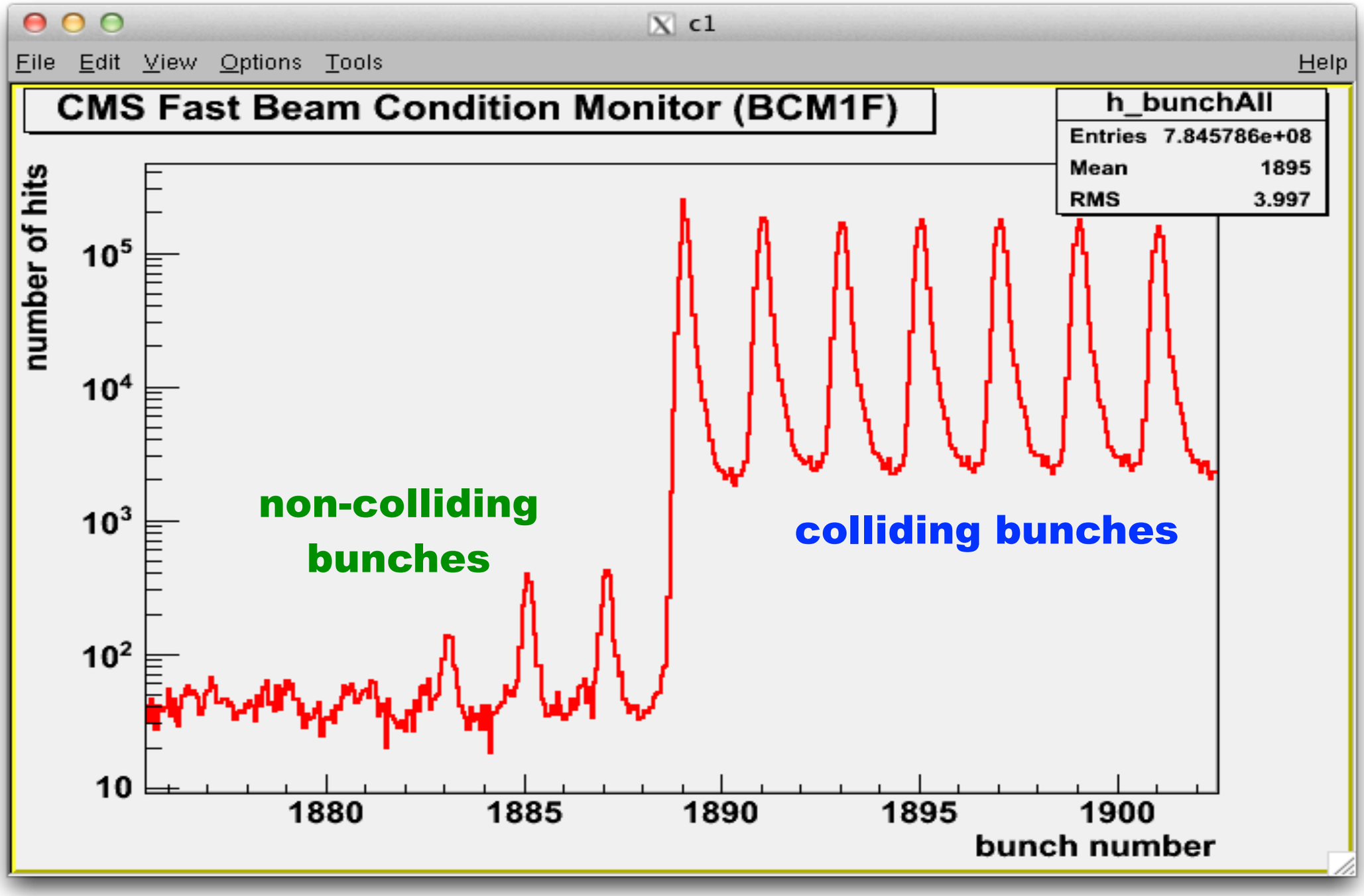


Thanks to Vladimir, Elena and Hans!

Scalers Wiring with LUT
Henschel/Lange
17Feb10

High rates

Well resolved bunches



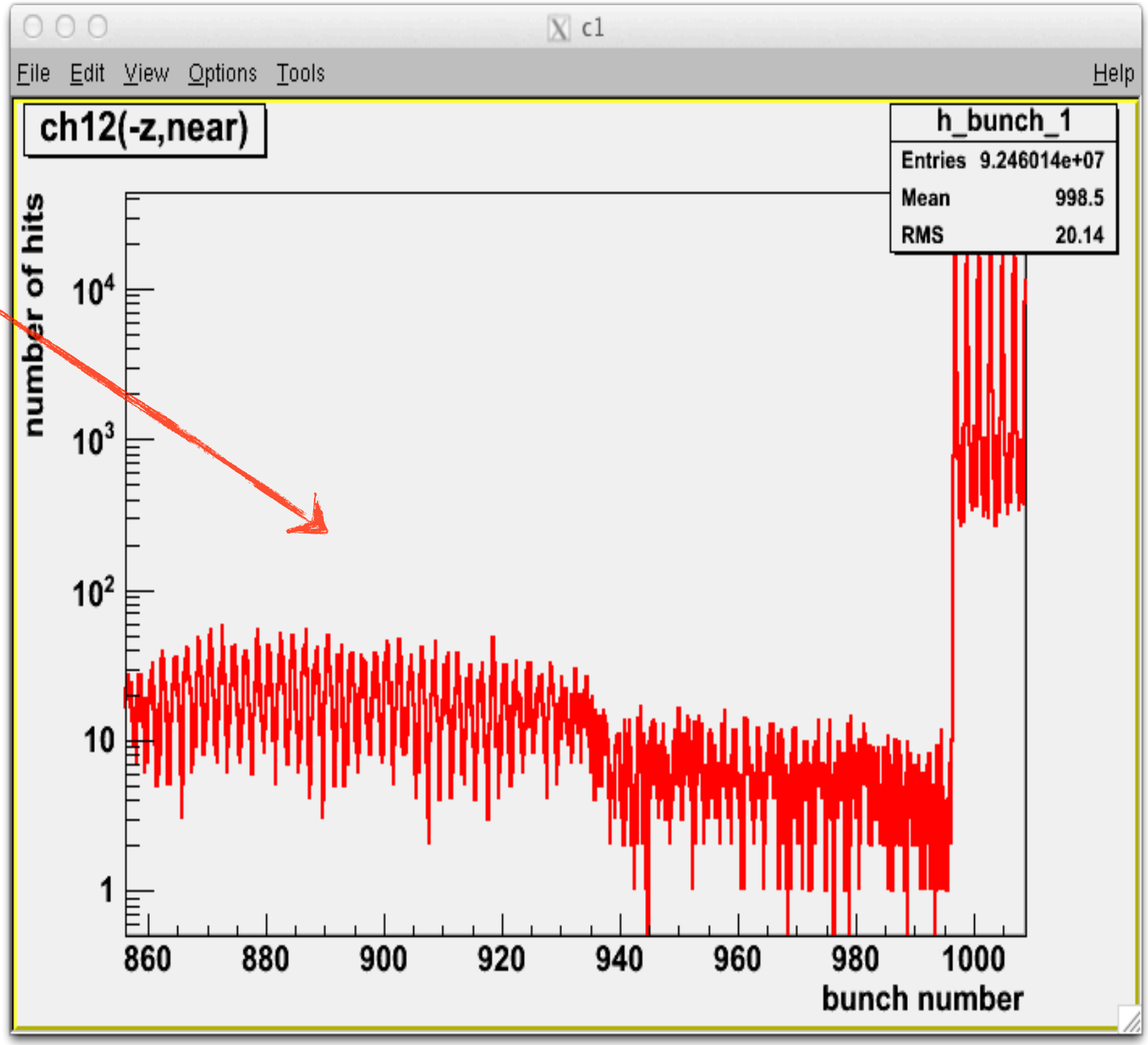
High rates

Spurious bunches

- Spurious bunches re-appearing (08.09.11)

- CH12, CH13, CH22, CH23

- **NEW BOARD!!!**



High rates

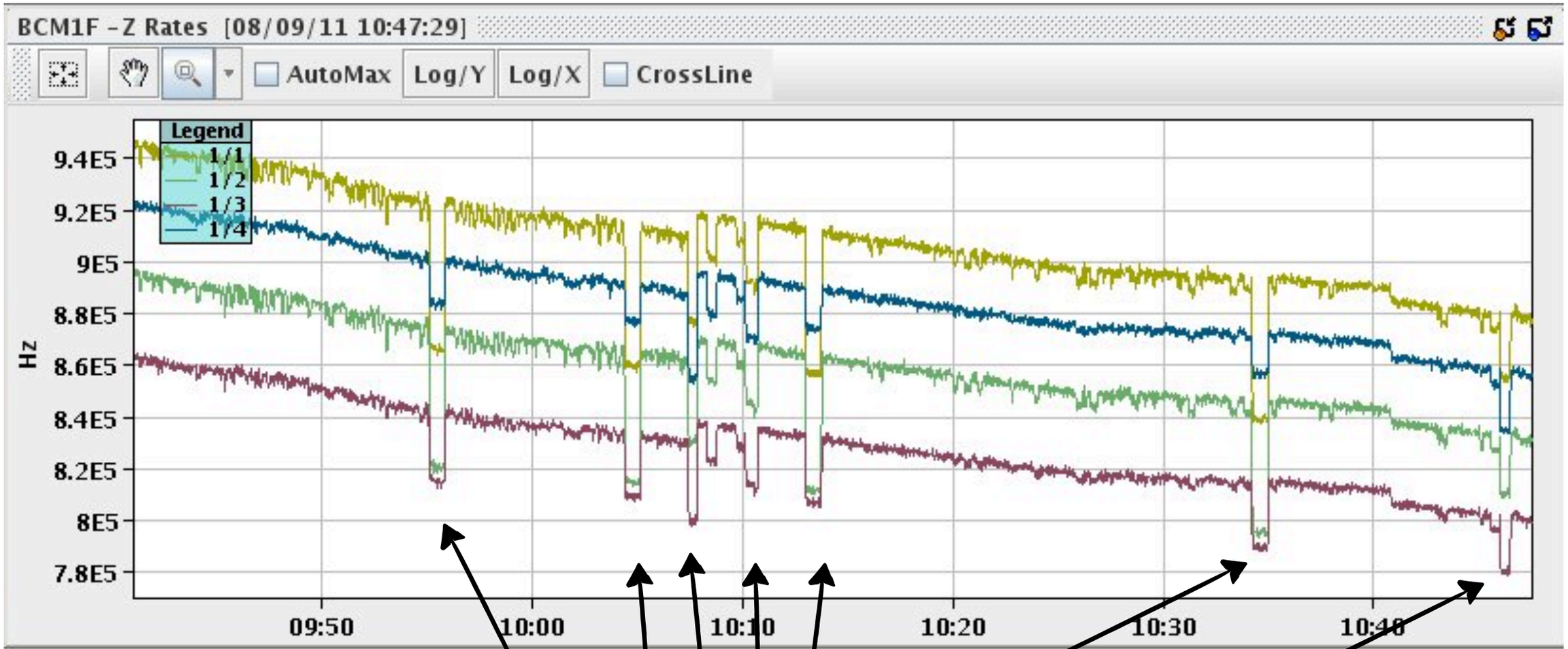
Readout errors

- In addition, errors are back!

```
ERROR in TDC_No = 1 Hit Error
ERROR in TDC_No = 1 Hit Error
ERROR in TDC_No = 2 Hit Error
ERROR in TDC_No = 1 Hit Error
ERROR in TDC_No = 1 Event Buffer Overflow
ERROR in TDC_No = 1 Hit Error
ERROR in TDC_No = 1 Hit Error
ERROR in TDC_No = 1 Event Buffer Overflow
ERROR in TDC_No = 2 Hit Error
ERROR in TDC_No = 1 Event Buffer Overflow
```

- ***"The timing data from the hit registers are checked for correctness when written into the event buffer. If an error is detected in the data the Hit_error status is set… The setting of this error condition normally implies that the DLL has lost lock caused by loss of clock for an extended period."***

High rates
TDC-Scaler correlations



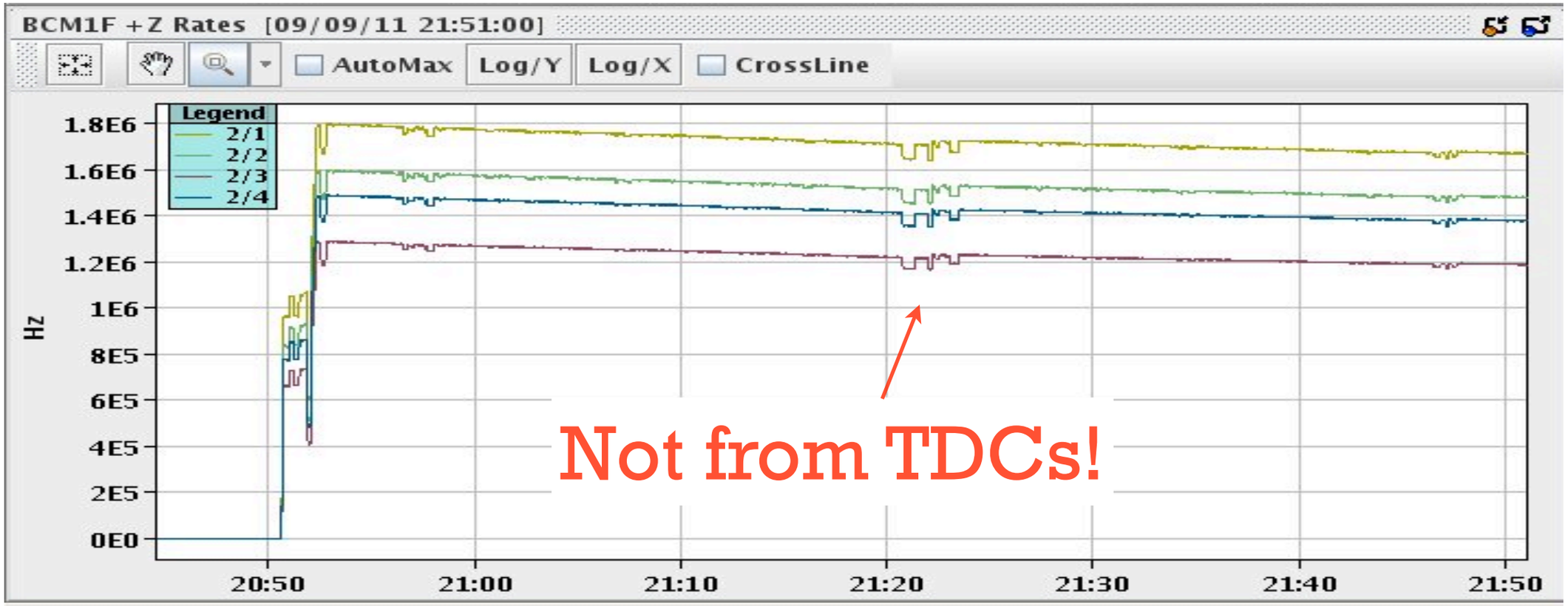
TDCs resets!

High rates

Tests

- **Channels (CH12, CH22, CH13, CH23) connected to TDC chips 1 & 2, disabled (Fri 09.09)**

- TDCs ran smoothly during fill 2092 with CH11, CH21, CH14, CH24 in chips 0 & 3. Rates up to 3 MHz per chip!



Software
Status

- Better handling of readout errors, with more logged information.

- Reduced the size of the almost full buffer to account the start signals that are not vetoed during the readout avoiding buffer overflows. Tests performed in the beginning of August with excellent results: two weeks of data taking without a single buffer overflow error.

- Minor changes/cleaning/fixes in other codes.

- Modification in codes committed to repository.

Software

Ring Buffer

- New libraries for the ring buffer provided by Konstantin Boyanov.
- Main feature: location of the ring buffer in memory is static.
- In principle, if the readout job crashes other ring buffer client jobs don’t need to be restarted. They keep idle and resume when there is a new entry in the ring buffer.
- In very preliminary tests the location in memory does not change once the ring buffer is created. But the client jobs don’t resume after new entries are provided to the ring buffer.
- Tests ongoing…

To do

- More tests with the TDCs in the gated crate.
- Part of the tests should be without gated signals, but all signals. I would like to compare the performance between the two crates and calibrate the reference time and differences due to cable length in the gated crate.
- Investigating different readout mode to use a time window to sample part of the orbit.
- ...

Summary and conclusions (I)

- **NEW TDC BOARD MORE STABLE WITH RESPECT TO THE BUFFER READOUT ERROR.**

- **~3ns resolution with non-colliding beams!**

- Strange bumps seen during collisions.

- Strange pattern from pulse generator signals observed in both TDC 767 boards in the main crate but not seen in the gated crate by TDC 1290.

- **TDCs running fine since Fri 09.09 with 4 channels only, chips 0 & 3.**

Summary and conclusions (II)

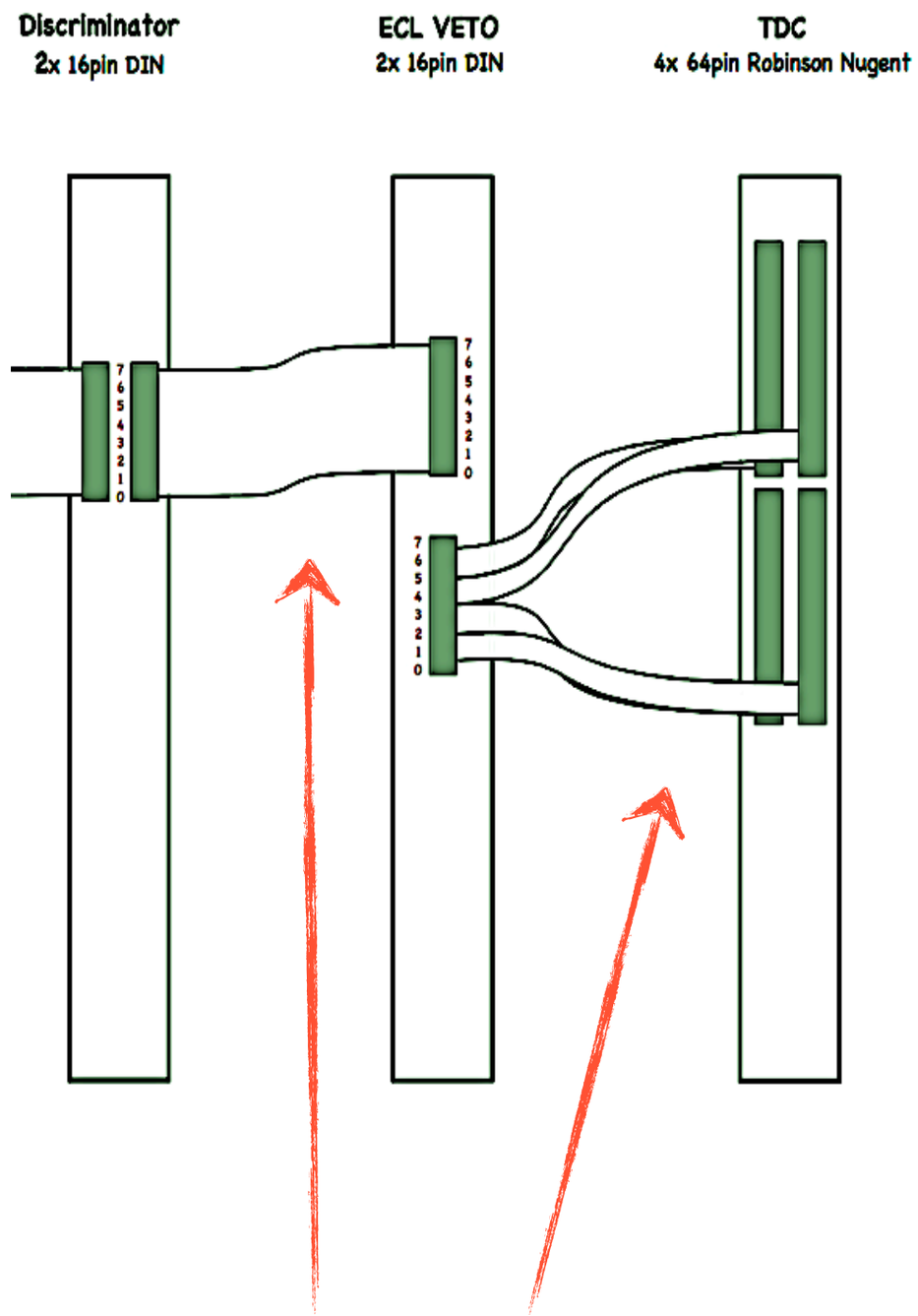
- **Improvements in the software were done for better error handling and to deal with high rates.**

- In case modifications are not enough to tackle high rates, try to mask one channel per TDC chip and/or lower the almost full level.

- Preliminary tests performed with new version of the ring buffer libraries.

Summary and conclusions (III)

- Errors from chips 1 & 2 at high rates.
  Channels disabled -> no errors.
- Spurious bunches in channels connected to chips 1 & 2 as with previous board.
- Are both problems correlated?
- Hit errors in chips 1 & 2 seen in previous board before being replaced!
- **To be investigated:**
  - Damaged cables
  - Problems with VETO
  - Could chips 0 & 3 handle the 8 channels?

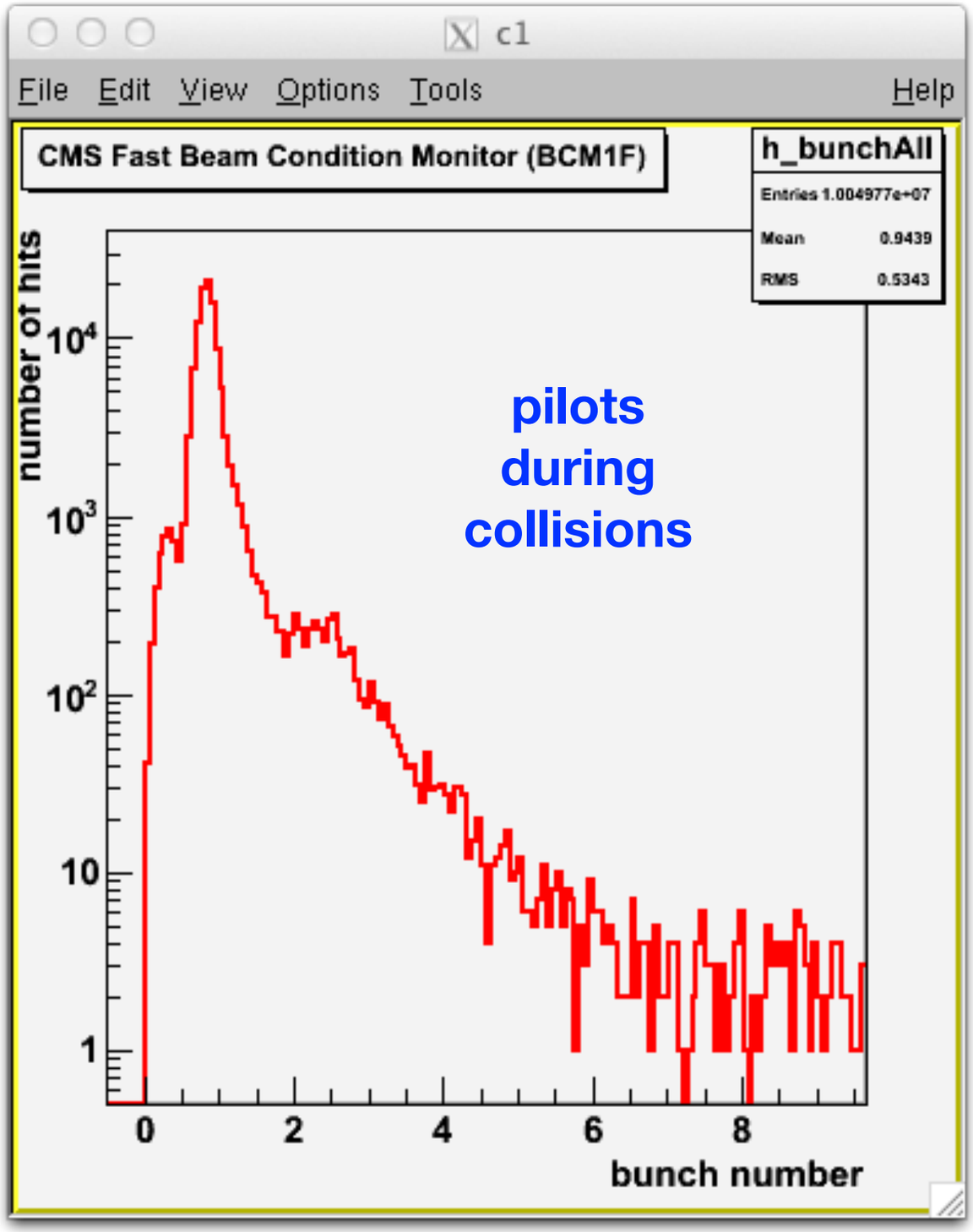


Many thanks to Elena!

Extra slides

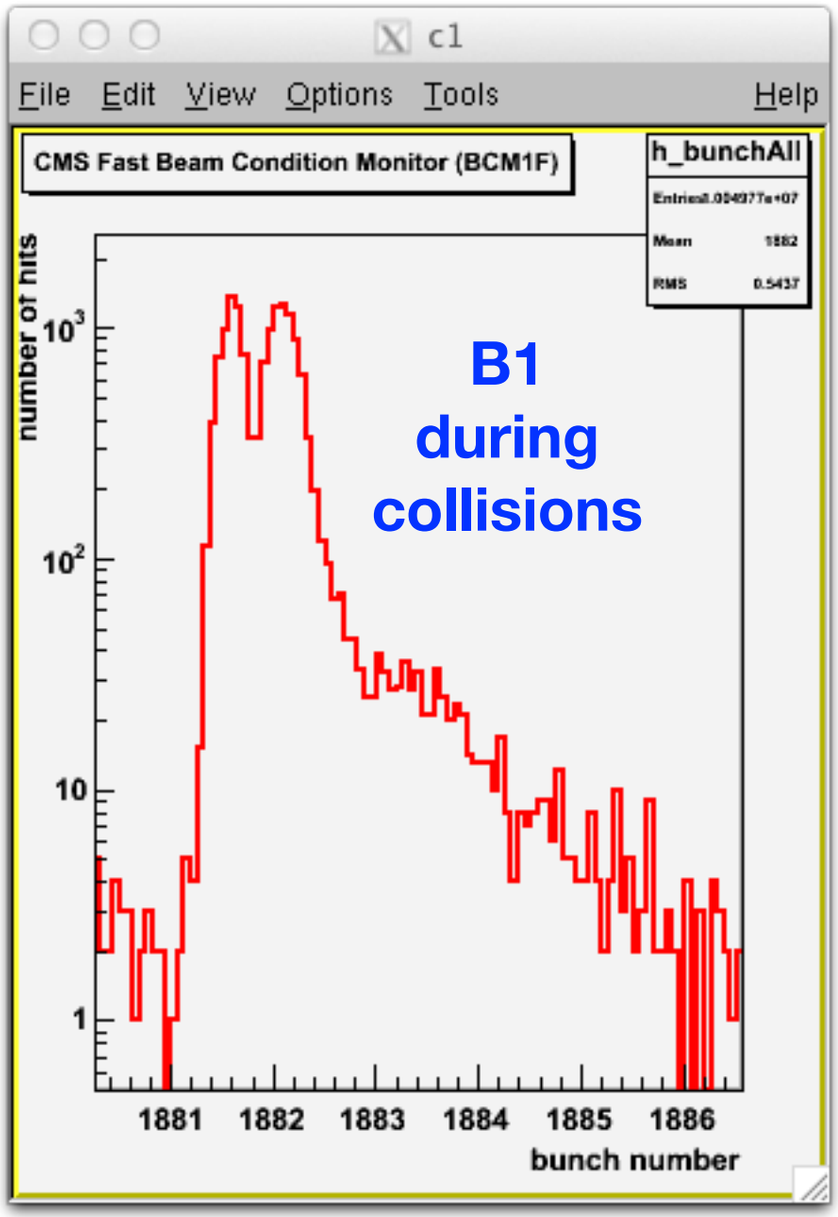
Data

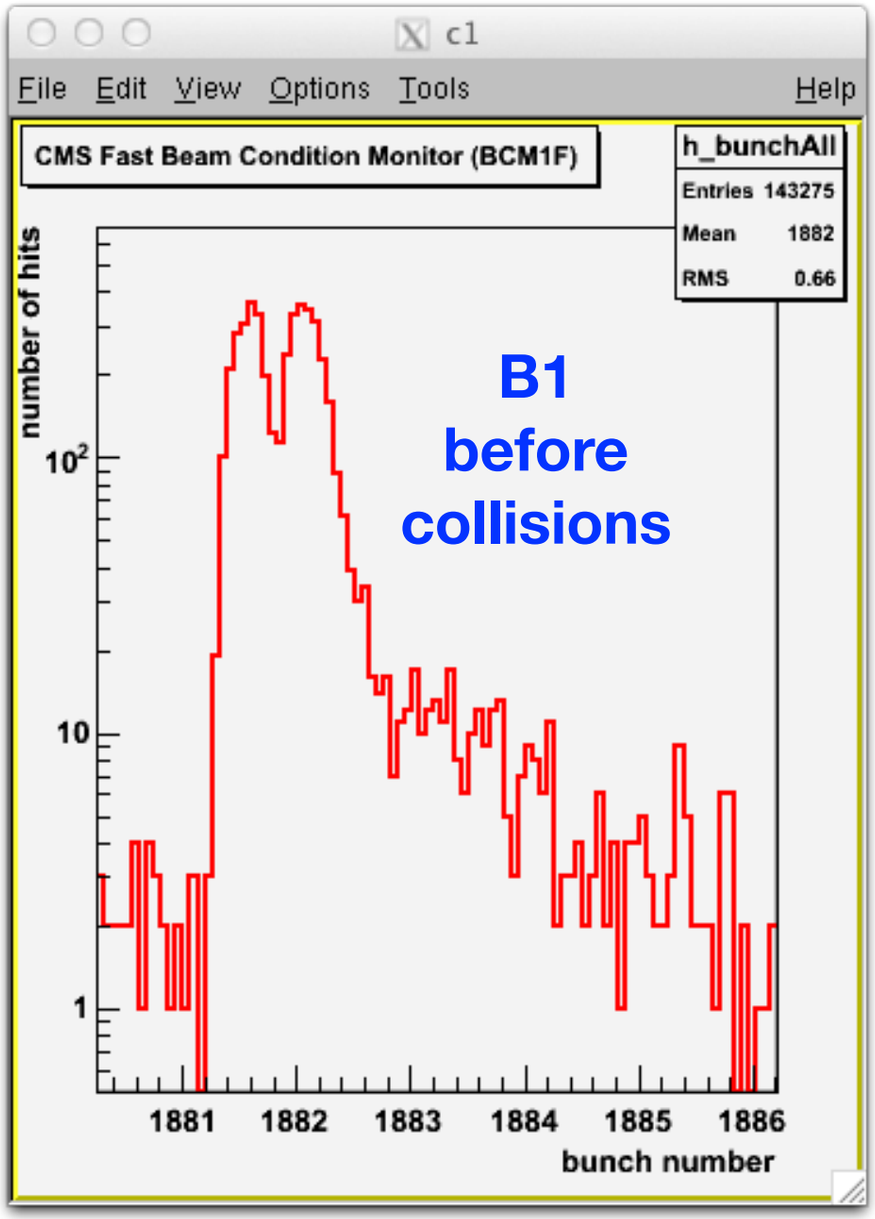
Beams


c1
File Edit View Options Tools Help
CMS Fast Beam Condition Monitor (BCM1F)
h_bunchAll
Entries 1.004977e+07
Mean 0.9439
RMS 0.5343
number of hits
10^4
10^3
10^2
10
1
0
2
4
6
8
bunch number
pilots
during
collisions

Data

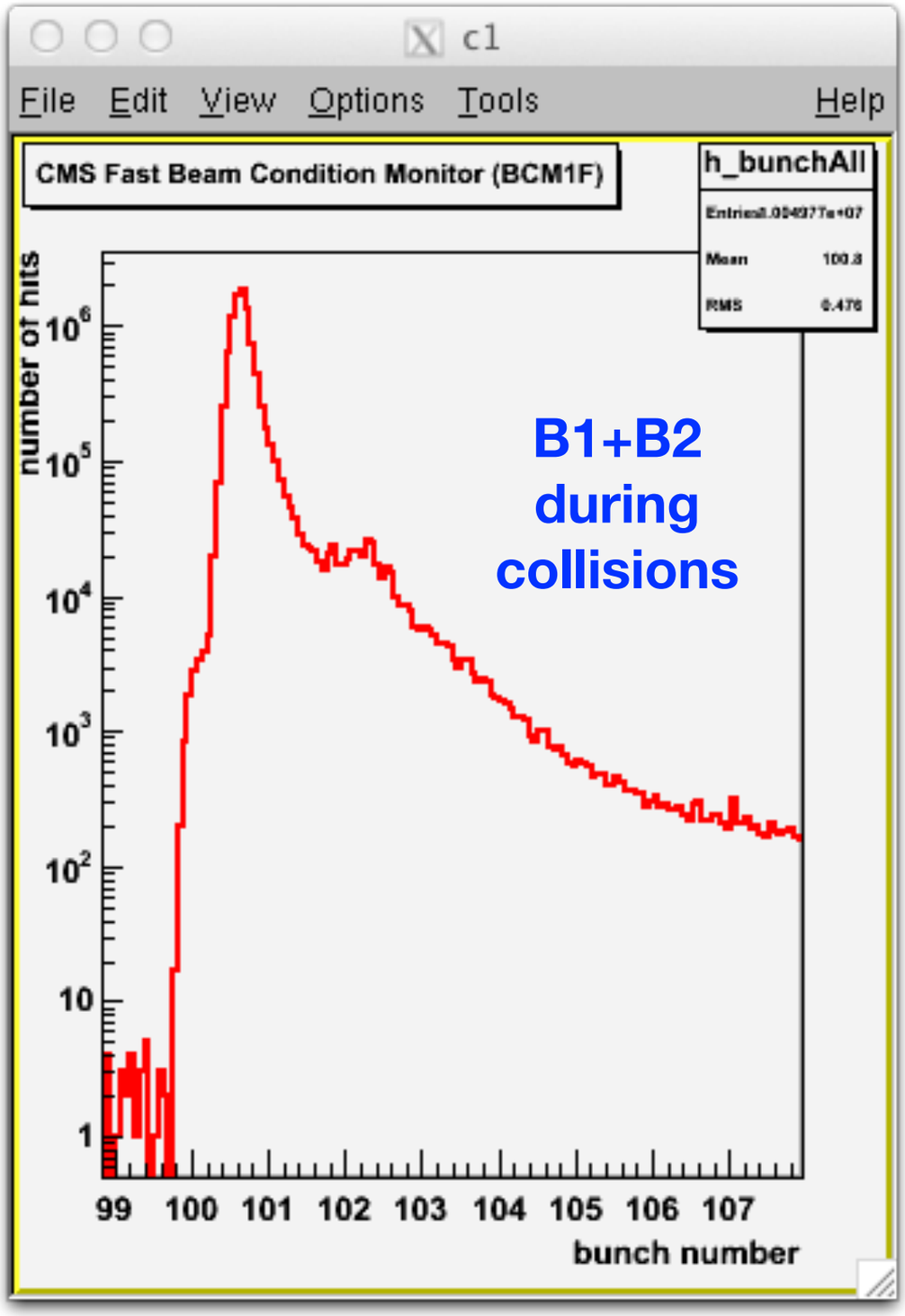
Beams

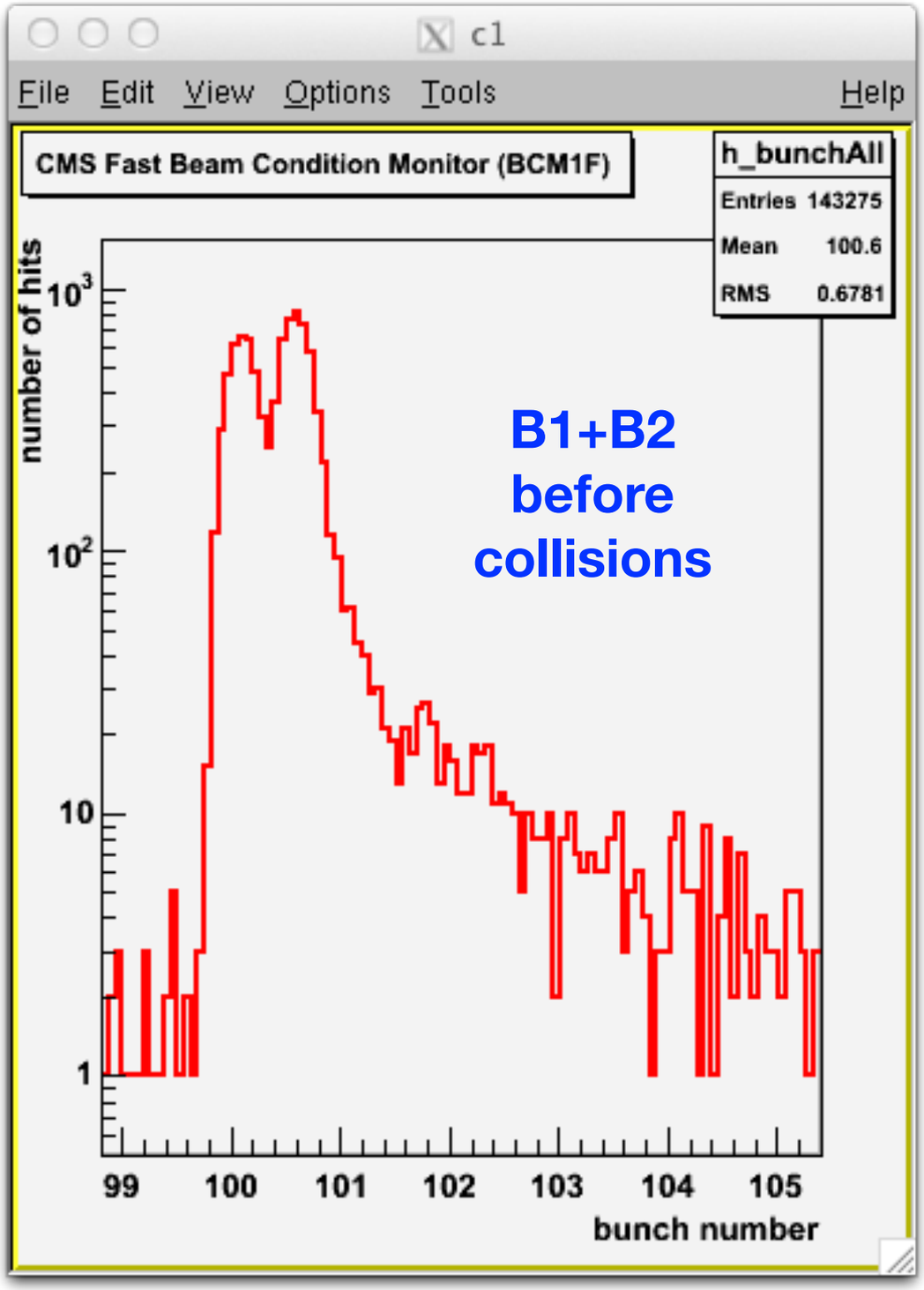

c1
File Edit View Options Tools Help
CMS Fast Beam Condition Monitor (BCM1F)
h_bunchAll
Mean 1882
RMS 0.5437
number of hits
10^3
10^2
10
1
B1
during
collisions
1881 1882 1883 1884 1885 1886
bunch number


c1
File Edit View Options Tools Help
CMS Fast Beam Condition Monitor (BCM1F)
h_bunchAll
Entries 143275
Mean 1882
RMS 0.66
number of hits
10^2
10
1
B1
before
collisions
1881 1882 1883 1884 1885 1886
bunch number

Data

Beams


c1
File Edit View Options Tools Help
CMS Fast Beam Condition Monitor (BCM1F)
h_bunchAll
Mean 100.8
RMS 0.476
number of hits
bunch number
B1+B2
during
collisions


c1
File Edit View Options Tools Help
CMS Fast Beam Condition Monitor (BCM1F)
h_bunchAll
Entries 143275
Mean 100.6
RMS 0.6781
number of hits
bunch number
B1+B2
before
collisions