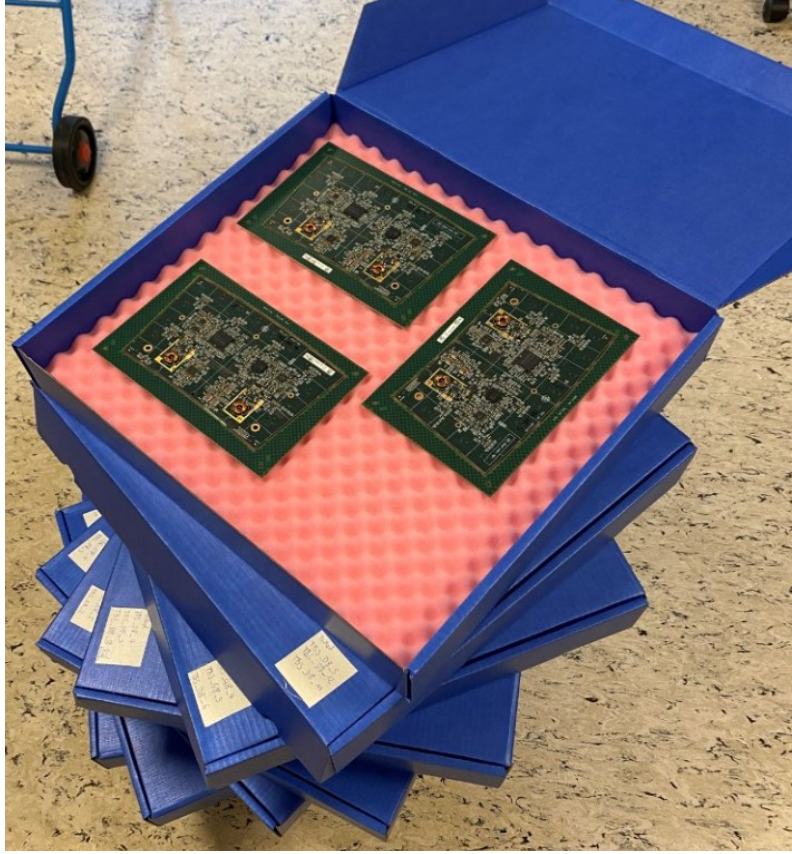
Automated Quality Control
for SiPM-on-Tile Modules in the CMS HGCAL Upgrade



FH SciComp Workshop'25

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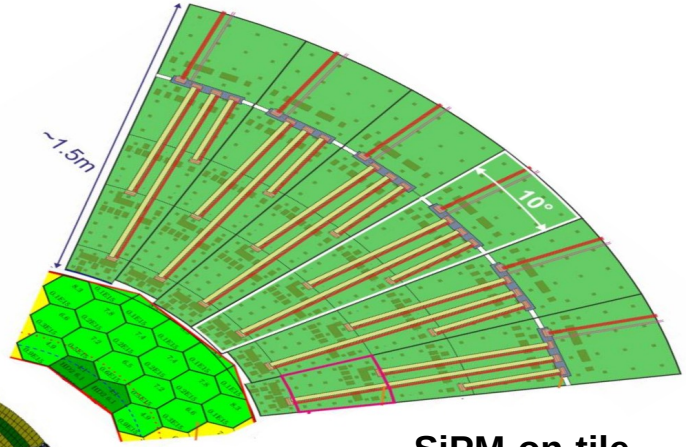
(DESY CMS & FTX groups)

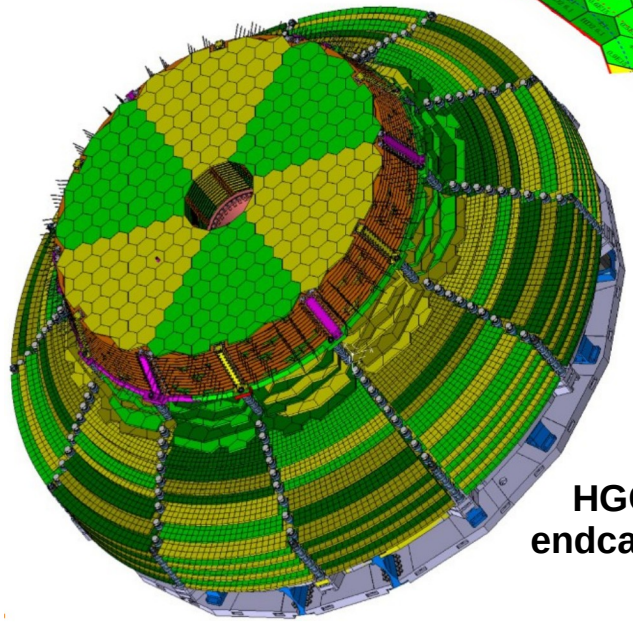
Outline

- The CMS high granular calorimeter upgrade (HGCAL) for HL-LHC
- SiPM-on-tile module production at DESY
- Software for automatic quality control
- Outlook:
  Tileboard/module tracking tool
- Summary



Silicon modules

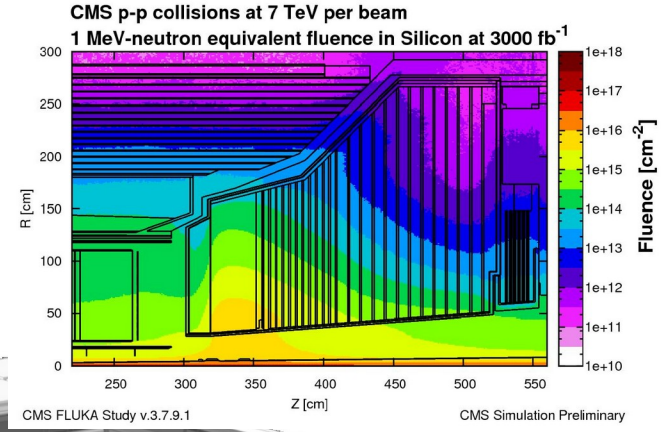
SiPM-on-tile modules



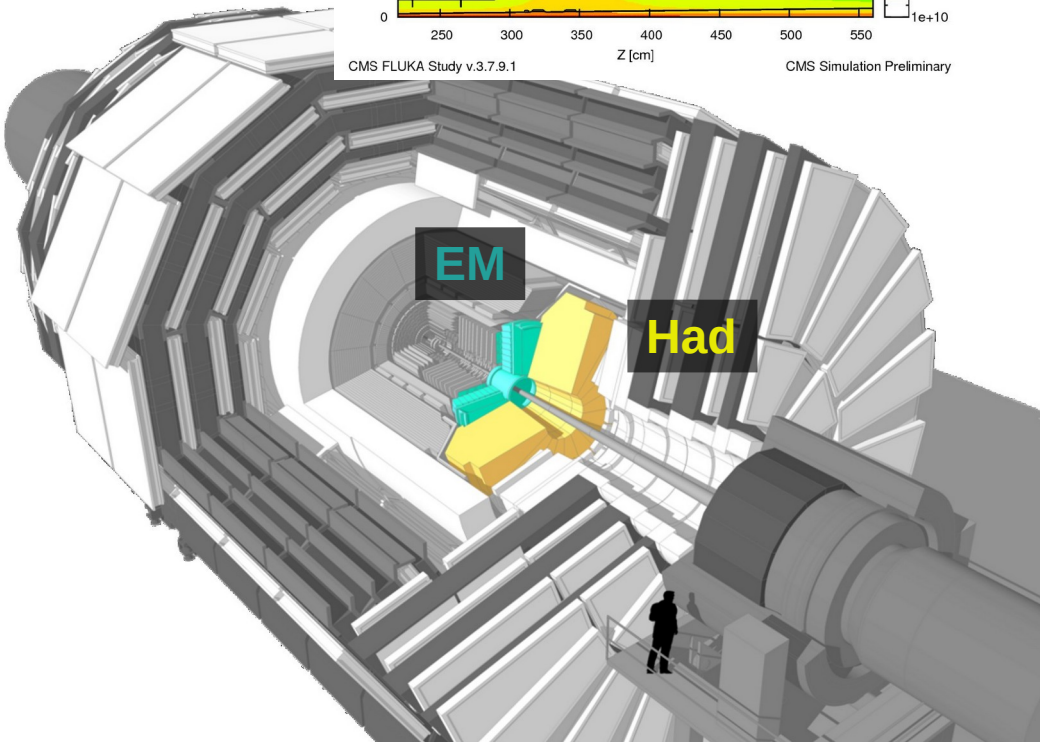
HGCAL endcap

Introduction

- HL LHC luminosity will reach $5\text{–}7.5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
  = 4x higher than currently!
- Up to **200 pileup** events expected
- LHC detectors have to be upgraded!



- CMS high granularity calorimeter (HGCAL)
  = **entirely new calorimeter** in both endcaps
  - Covers $1.5 < |\eta| < 3$
  - Electromagnetic & hadron calorimeter parts
  - Finely-segmented & radiation-hard
  - Contributes to event trigger decision

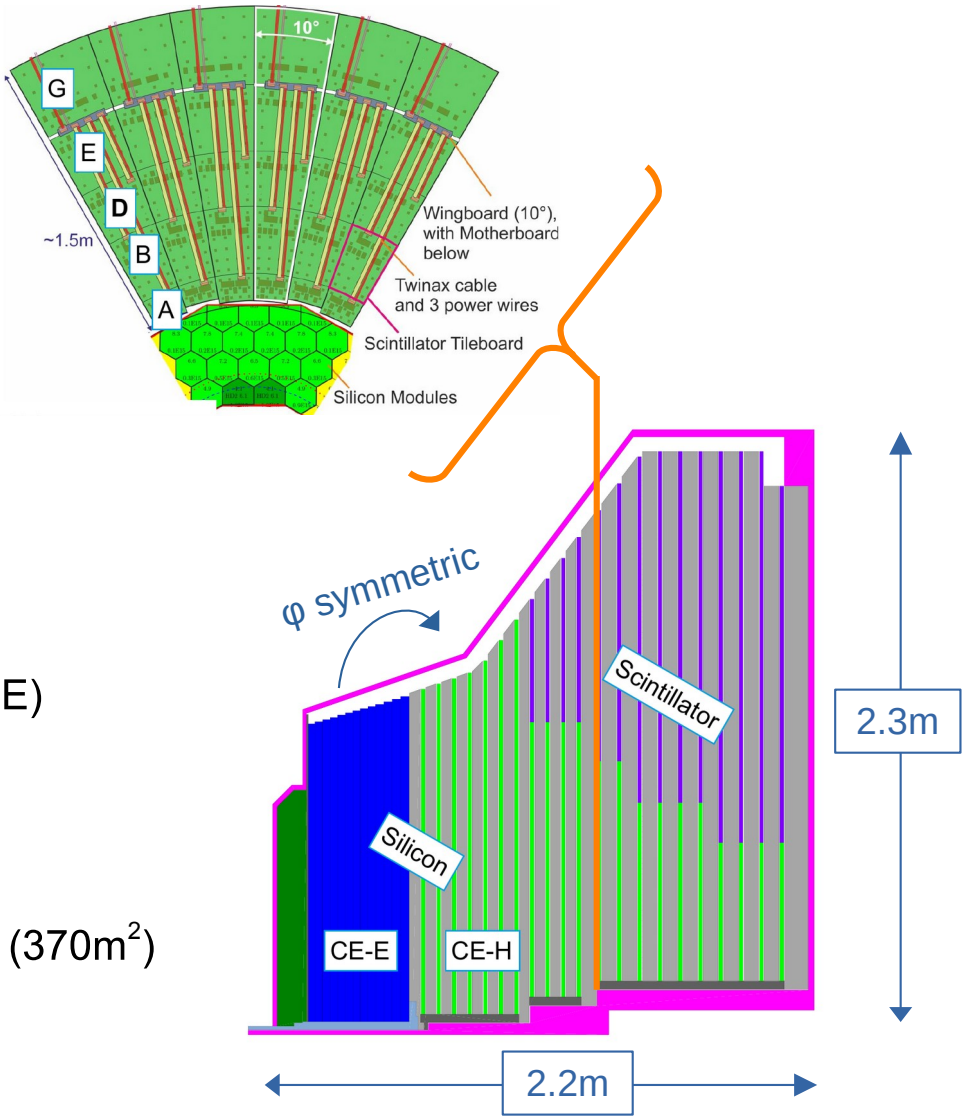


Composition

- CE-E: Electromagnetic calorimeter
  - **Hexagonal silicon modules**
  - Cu, CuW, Pb absorbers, 26 layers ($\approx 28 X_0$)

- CE-H: Hadronic calorimeter
  - Hexagonal silicon modules (similar as CE-E)
  - **Scintillator tiles** in regions with lower radiation (< $5 \cdot 10^{13} \mathrm{n/cm}^2$) w/ silicon photomultipliers (SiPMs) for readout
  - Cu/Steel absorbers, 21 layers ($\approx 10\lambda$ including CE-E)

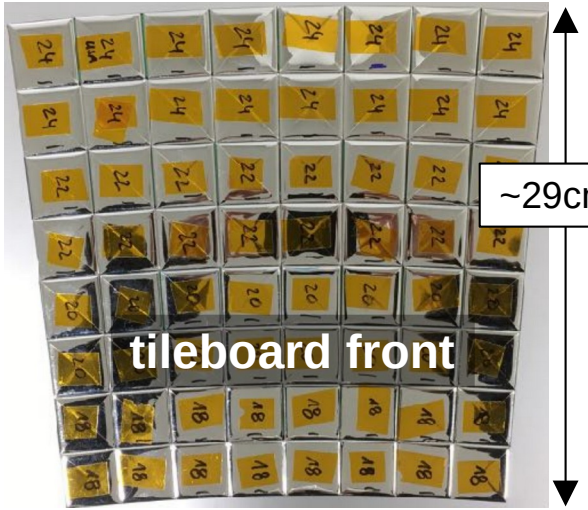
- Key parameters
  - 6M silicon channels from 26k modules (620m^2)
  - 240k SiPM-scintillator channels from 3.7k tileboards (370m^2)
  - Cooled to -30°C using two phase CO_2 cooling
  - 220t per endcap



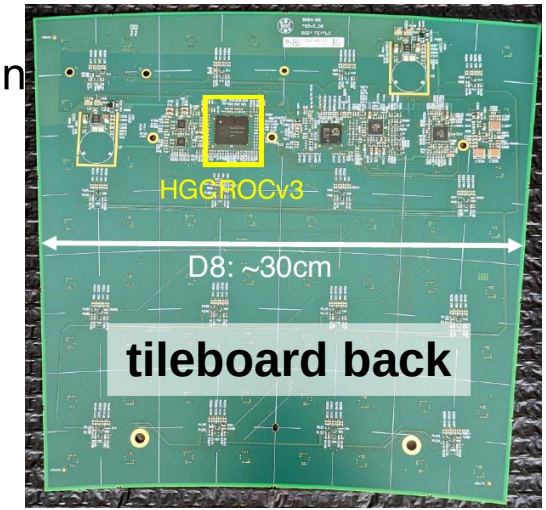
SiPM, Tiles & Boards

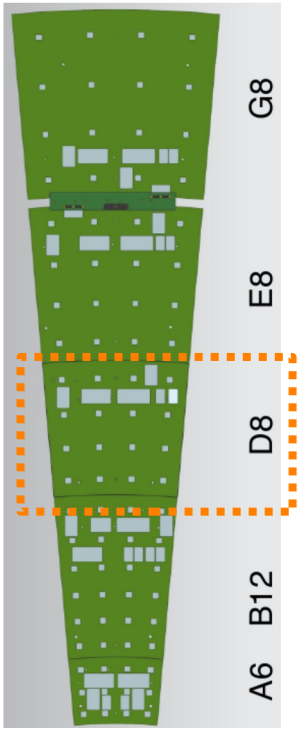
SiPM-on-tile originally developed by CALICE for e^+e^-

- Trapezoidal scintillator tiles (1.25°)
  - Wrapped in reflecting foil
  - 3mm thickness
  - Size increases radially from 2 to 5.5cm
  - Cast/machined or injection-molded
- SiPMs
  - Radiation-tolerant & low dark-rate after irradiation
  - High photon detection efficiency
  - Includes UV-LED system for initial calibration
- Tile boards
  - 8 main geometrical form factors
  - Typically 8 x 8 = 64 tiles/SiPMs per board (requires only 1 HGCROC readout chip)



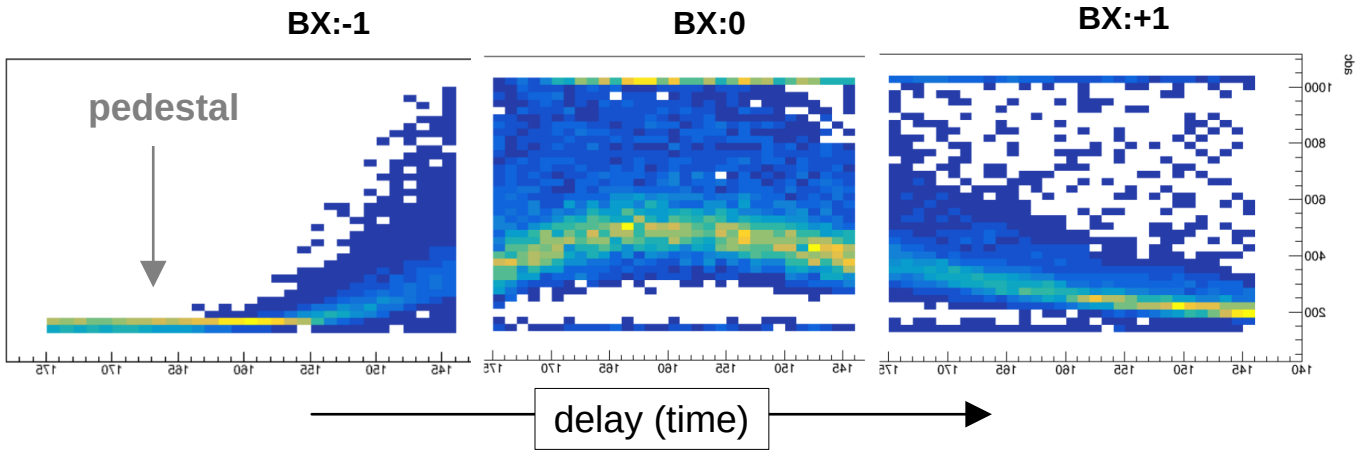
MPPCs



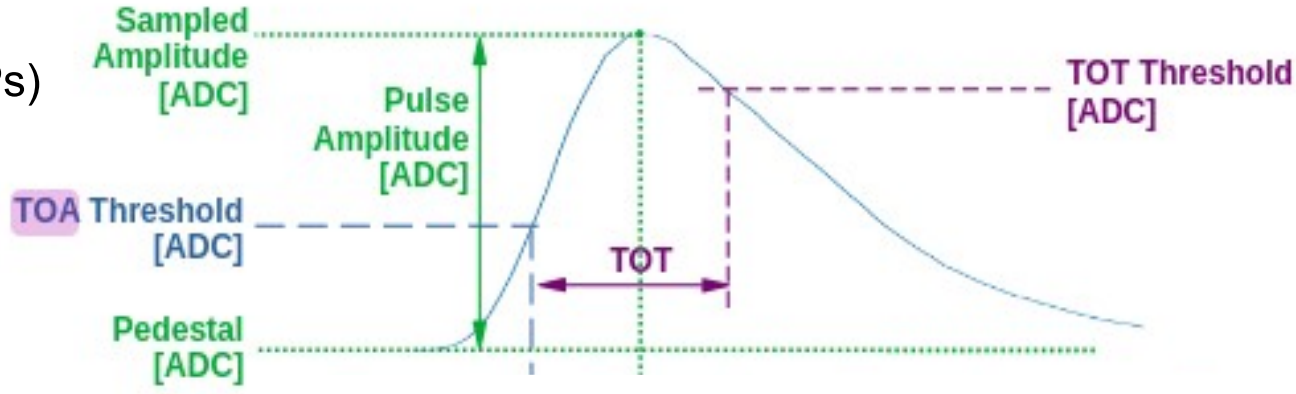


SiPM-on-tile module signals

- MIP pulse shape in DESY II testbeams
  - Read out time stamp from beam trigger system
  - MIP signal visible across 3 bunch crossings



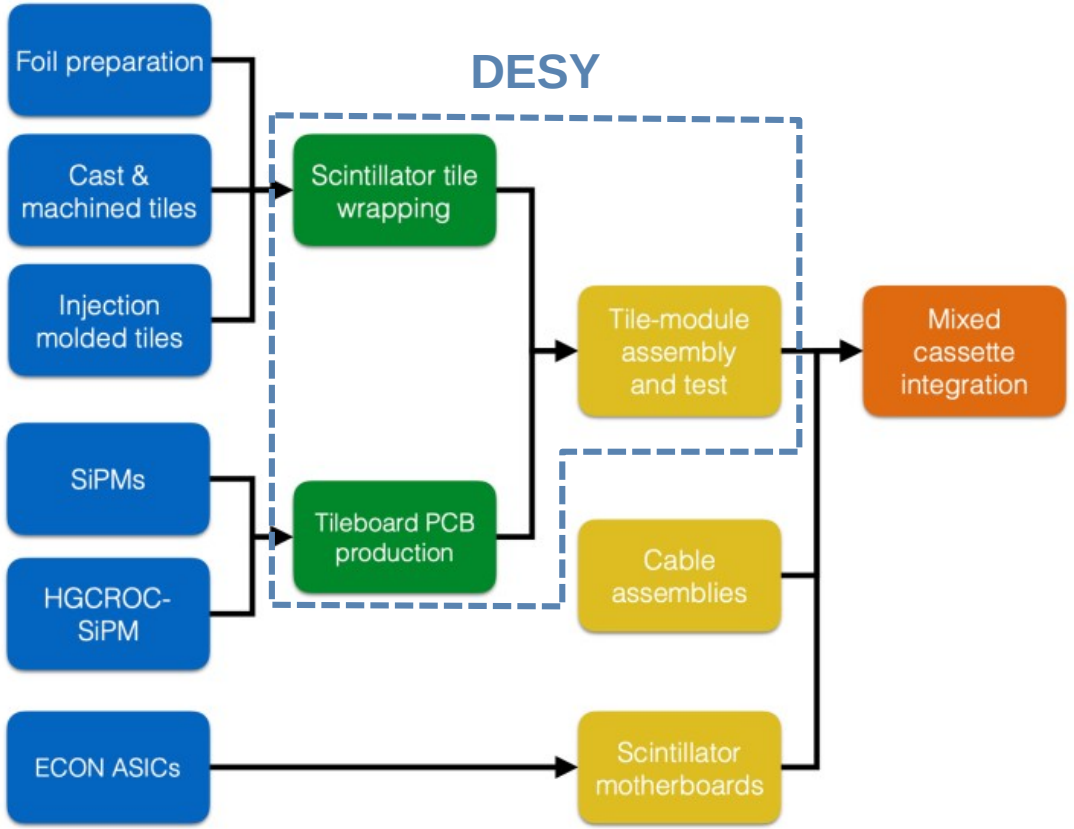
- Dynamic range
  - Read **ADC** at max. pulse when signal is **small** (~10 MIPs)
  - **Higher** signals covered by time-over-threshold (**TOT**)
  - ADC at previous bunch crossing read out for **pedestal subtraction**



Assembly overview

- Scintillator tiles
  - Moulding tiles at FNAL
  - Cast tiles from NIU
- Tileboard/module assembly & tests
  - Production target per site
    - 2'000 boards/modules in total
    - 150 modules/month
  - DESY: ZE assembly; FTX/CMS tests
  - US: board test (UMD), module assembly + tests (FNAL)
- Cassette assembly at FNAL

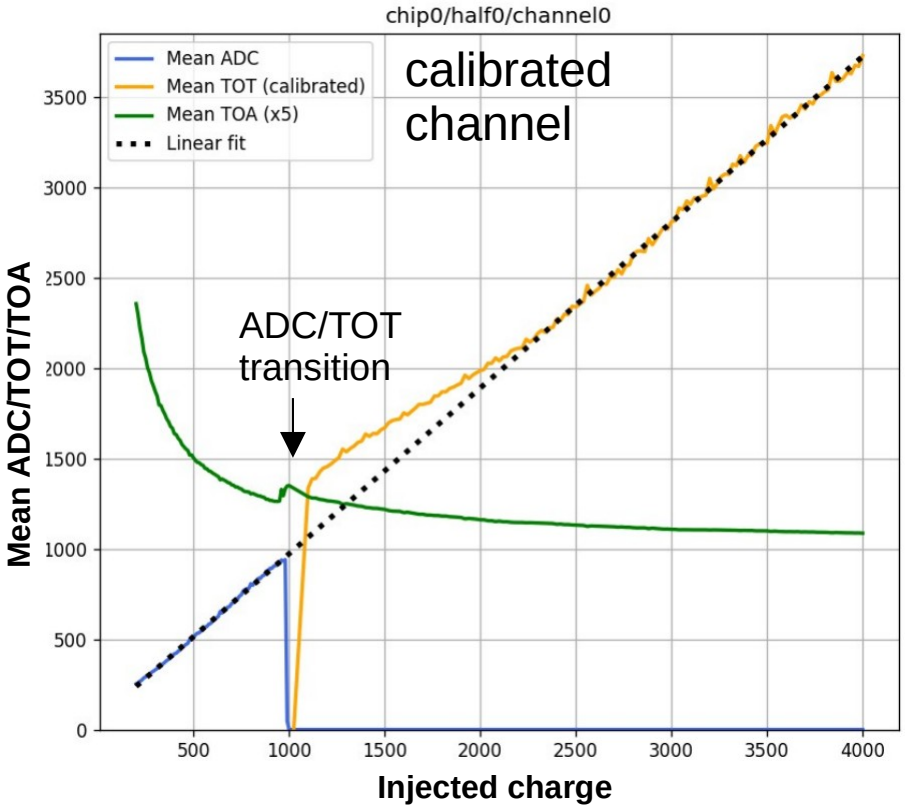
→ Coordination & regular exchange required between sites



Quality Control: Goals

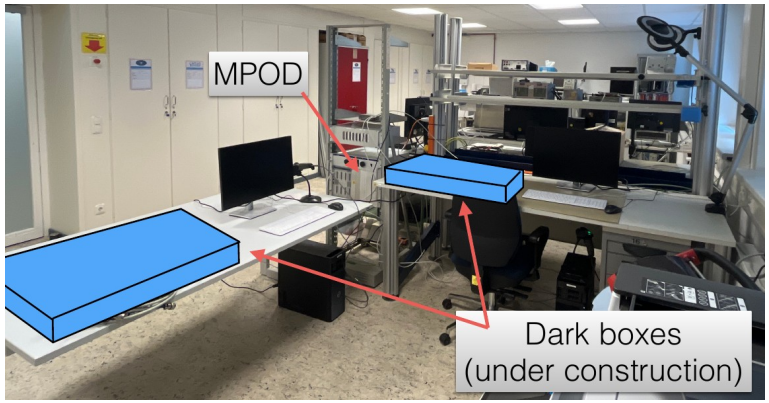
- Verify functionality of board
  - Smoke test: boards can be powered (Vcc: 11V; SiPM bias: 48V; LED: 5-8V)
  - Communication with readout chip

- Verify calibration of chip/board
  - Derive initial calibration per board/chip (provides also good starting point for operation in cosmic test stand/cassette test)
  - Calibrate sensors (temperature, voltage, current)
  - Adjust pedestals to common ADC level
  - Adjust timing (TOA & TOT)
  - Define transition ADC → TOT



QC tests at DESY

Tileboard QC (PCB+SiPMs)



Cold QC (electrical test)

Tilemodule assembly

Cold QC
(mechanical)

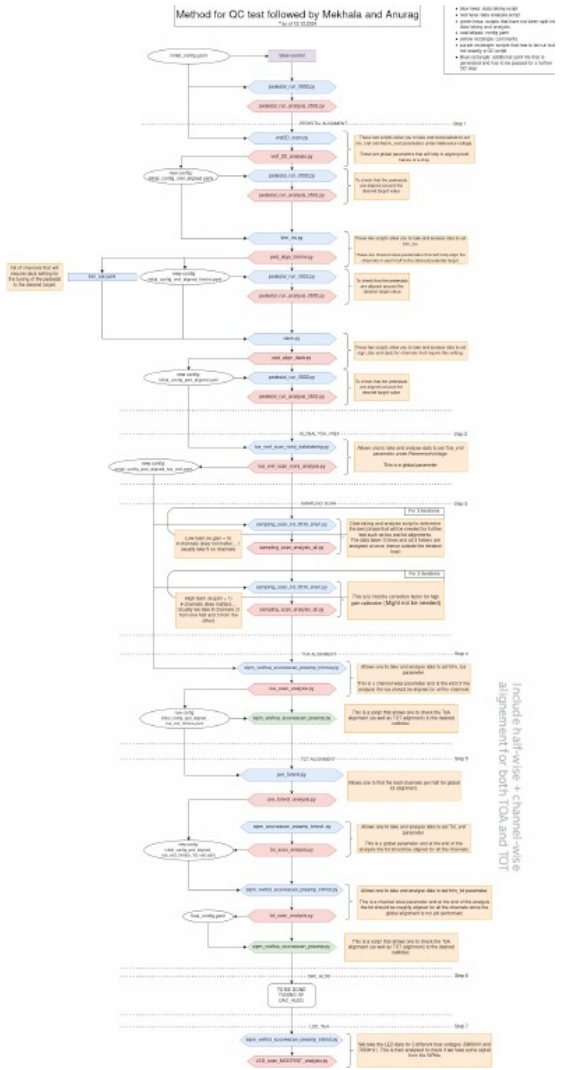
Tilemodule QC (cosmics)

send to
FNAL

Quality control SW requirements

- Multi-step procedure
  - Data-taking; parameter scans; analysis; deriving/loading new chip configuration files
- Many parameters
  - Per chip half or per channel
- Many outputs
  - Raw/ROOT files; analysis results (HDF5); plots & tables

- All of this needs to be ...
  - Reproducible
  - Operated by non-experts
  - Work “fast”; 30min/board for standard tests
  - Automated to minimize expert intervention
  - Stop early in case of hardware failures



TBQC framework

- New framework build on top of FPGA-based DAQ (purely written in python)
- Goal: streamline QC steps into **big chains**
- **Modular** approach
  - Easy to add/remove data-taking & analysis steps
  - Clear **configuration** and QC **flow**
  - Each step interacts with **data store** to add/retrieve results
  - Hardware operation through interfaces
- Organizes QC results into **reports** containing data for plots & tables + descriptions/comments
- Extensive gitlab CI tests to ensure code quality (pytest, flake8, mypy, coverage)
- Browser-based GUI foreseen as well

Central QC config

```
defaultConfig = {
    "firmware": "tileboard-triple-v3p0",
    "kriaIP": "test-fpga-5",
    "HGCROCVersion": "3a",
    "convGain": 4,
    "baseOutputDir": "/home/hgcal/testdata/",
    "pedestalTarget": 150,
    "pedestalLowerLimit": 145,
    "pedestalUpperLimit": 155,
}

[...]
```

Prepare hardware

```
kriaService = KriaServices()
kriaService.connect()
kriaService.loadFirmware()
kriaService.startDAQServer()
kriaService.startSlowControlServer()
kriaService.startDAQClient()

[...]
```

QC flow

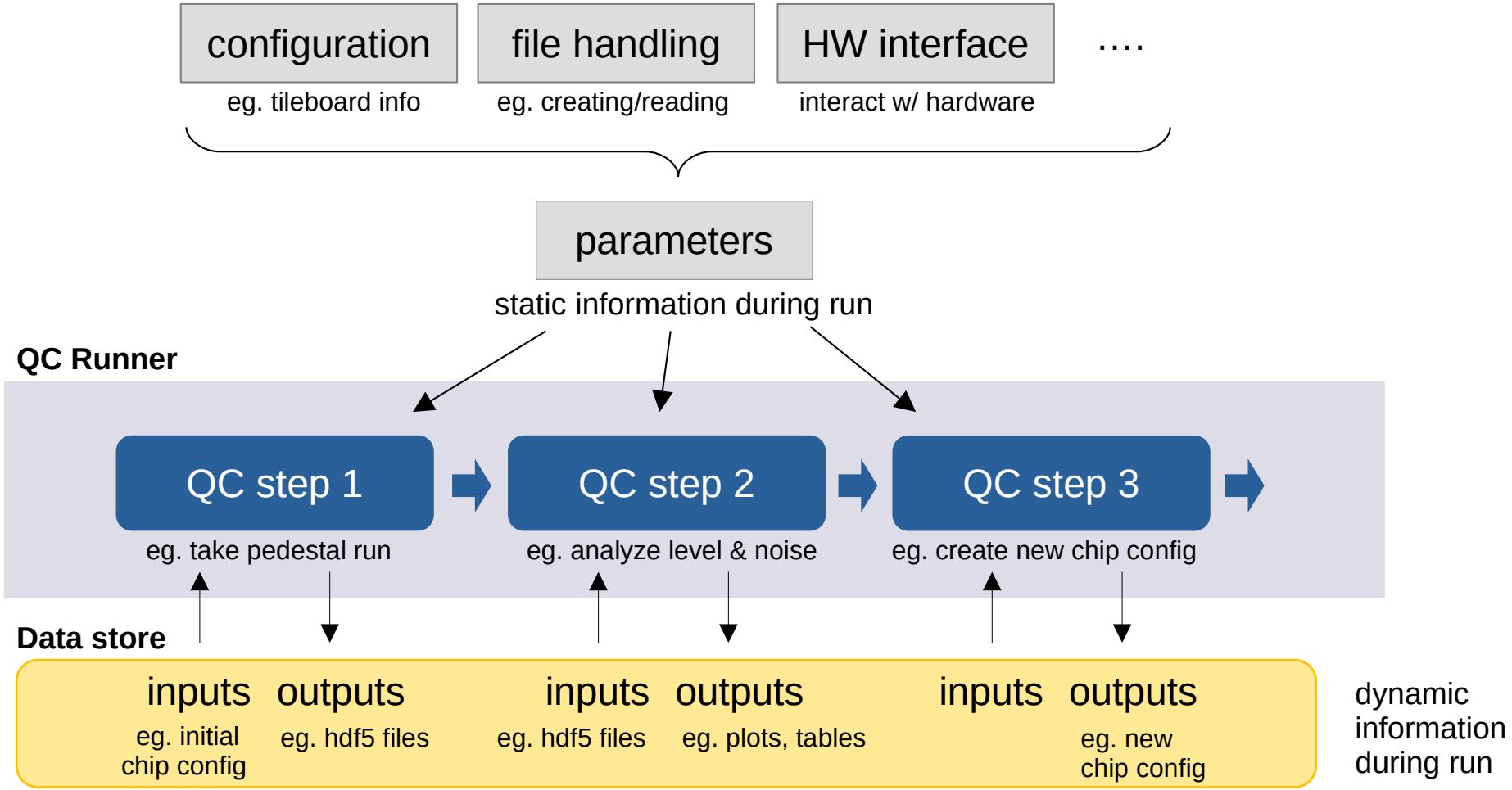
```
runner = Runner(
    runnables=[
        configGenerator,
        GlobalPedestalDAQ, globalPedestalAna,
        TriminvDAQ, triminvAna,
        dacbDAQ,dacbAna,
        pedestalDAQ,pedestalAna,
    ]
)

[...]
```

Execute steps

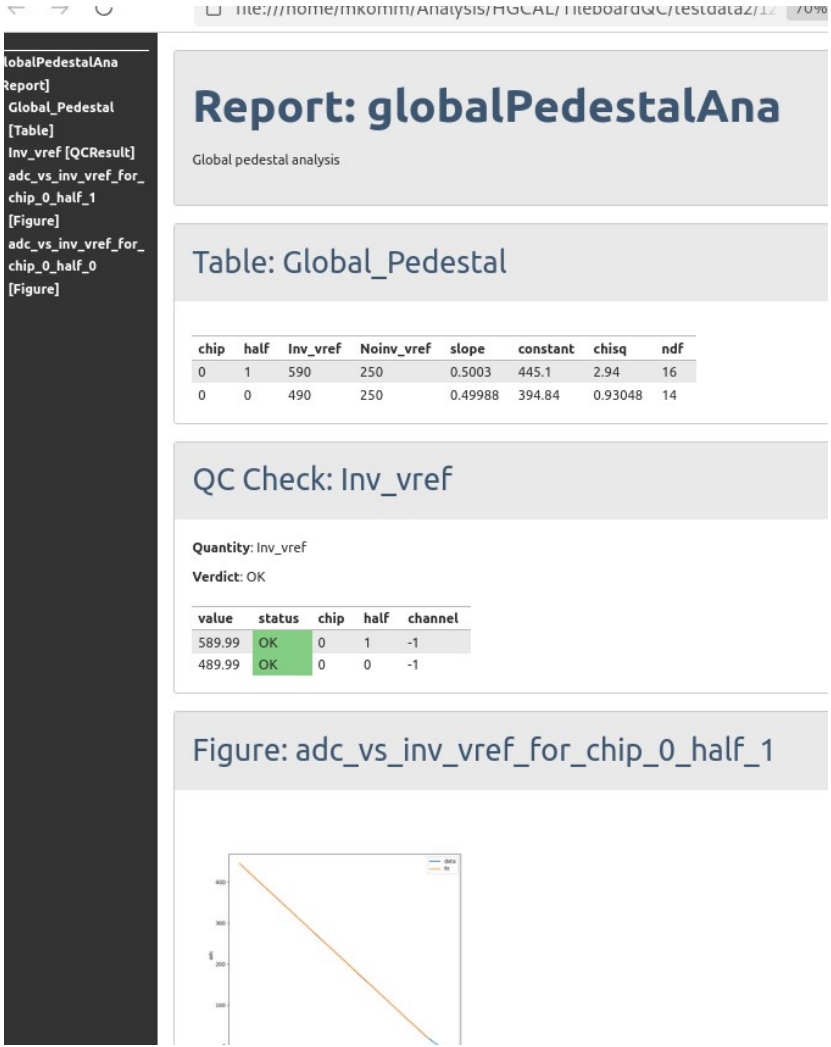
```
dataStore = DataStore(metaInfo = ...)
runner.runAll(dataStore)
```

Software structure

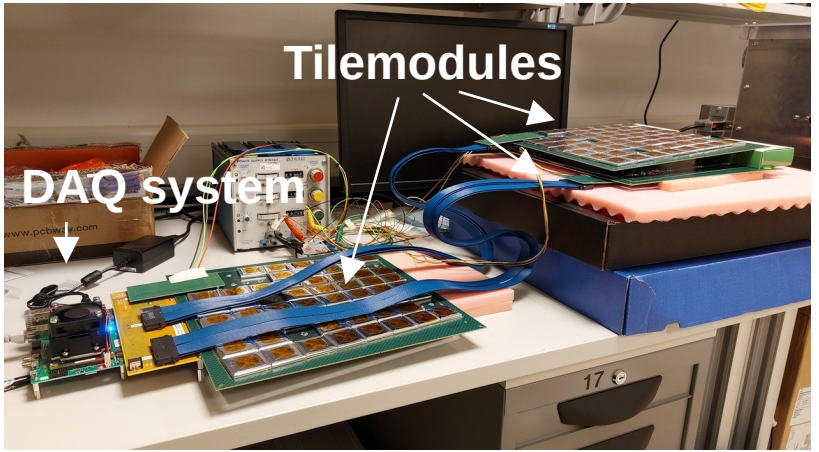


QC results

- Data store per run to pass & serialize information between steps
  - Input/output file paths
  - Run parameters & resulting chip configs
  - Detailed QC reports
  - Script to generate quick visualization as HTML page from saved reports
- Storage (~30TB required for all boards/modules)
  - Common EOS space at CERN foreseen
  - Can be queried to fill a subset of QC results into official CMS DBs
  - Enables meta analyses (eg. variations between boards)
  - Share chip configuration with cassette assembly



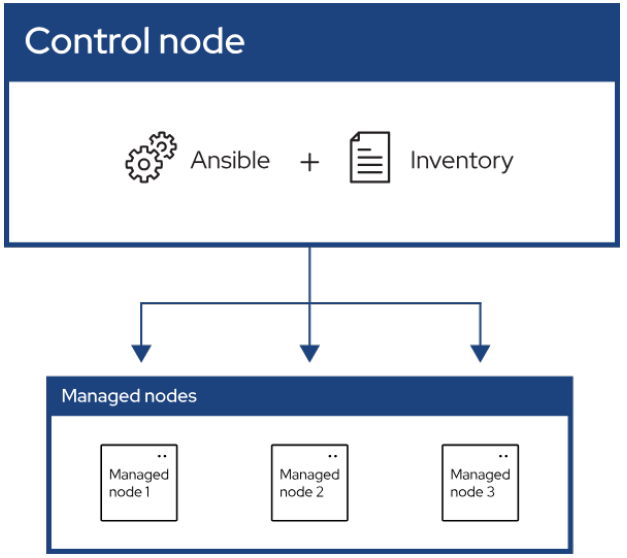
System administration



- Need easy way to configure QC PCs & FPGA-based DAQ systems
  - Distribute SW updates to all devices
  - Ensure consistent setup at QC stations; no debugging/SW developments
  - 2 dedicated stations for developments foreseen

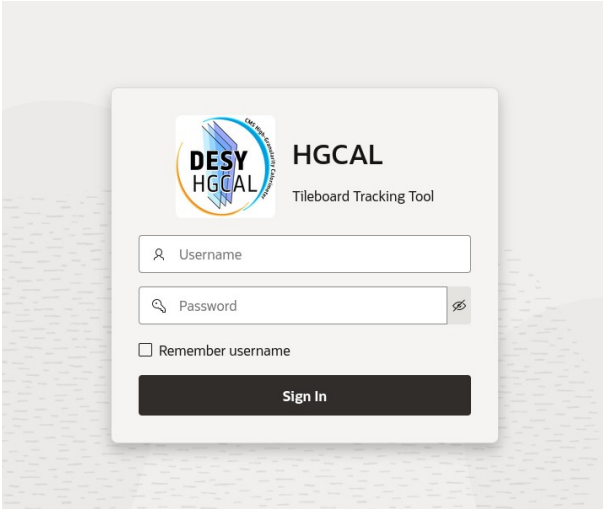
- Bottleneck
  - At DESY DAQ systems are in special network
    → No access to internet; local service needed!

- Solution: Ansible
  - Open-source automation tool for configuration management, application deployment, and orchestration
  - Only needs to be installed on a control node
  - All managed nodes will be controlled via SSH



Tileboard/module tracking system

- Motivation
  - Need a system to **keep track of tileboard/modules** internally at DESY
  - Easy to connect various information sources (eg. assembly)
  - Can be used to figure out what boards have been processed at which QC station, when & by whom
  - QC operators need easy access from all stations
  - Useful if a board is lost+found → **figure out its history** (eg. who has handled it in the past and when/why)

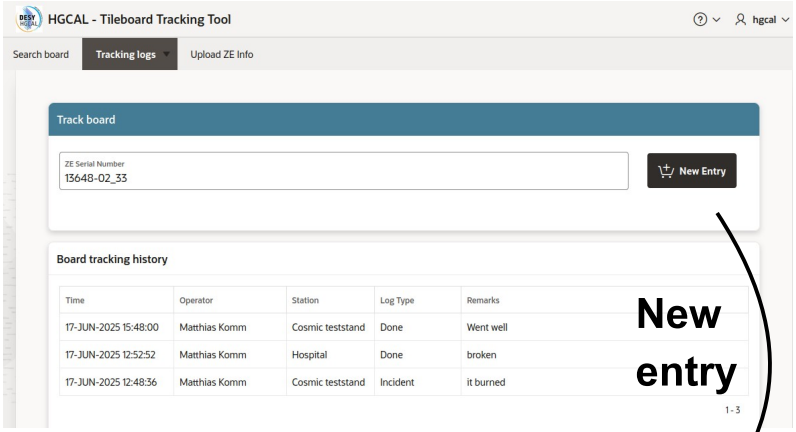


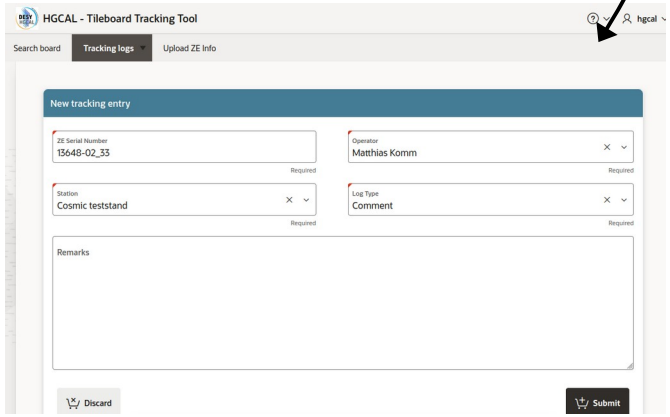
- Solution suggested by DESY IT
  - **Oracle APEX** application
  - Web frontend + Oracle DB as backend
  - Hosted at DESY directly; backup every day
  - Automatically query/add entries through REST API
  - Also useful to **collect inputs** to be uploaded to CMS assembly DB
  - Prototype → next slides

Tracking system prototype

Search board history by serial number

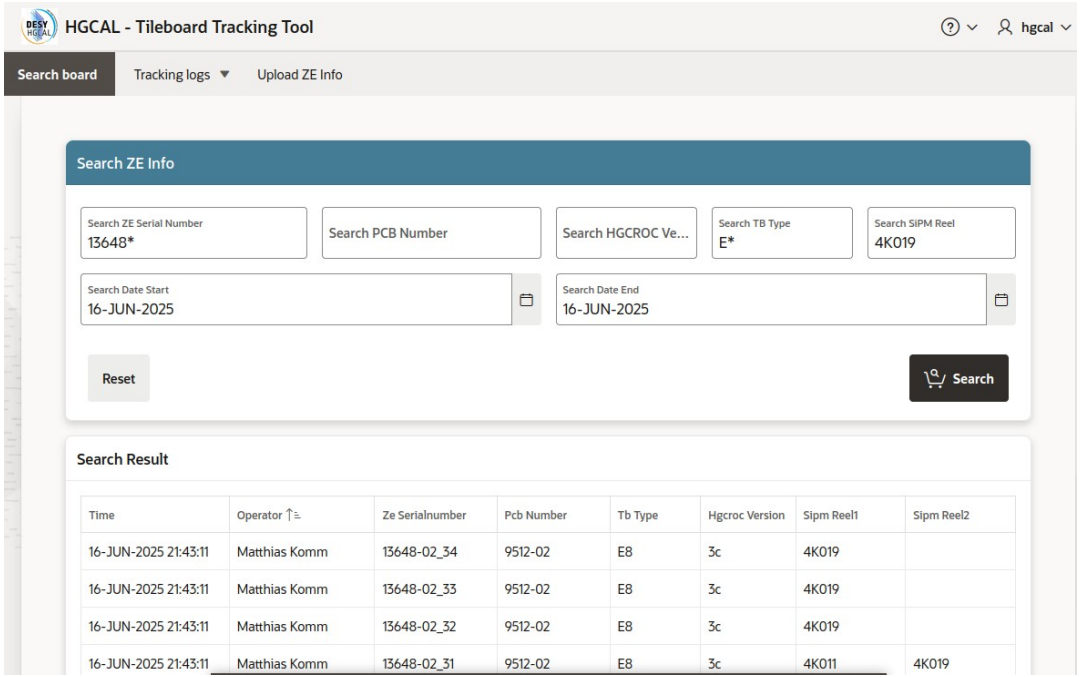
easy to use barcode scanner at QC stations





Search for boards

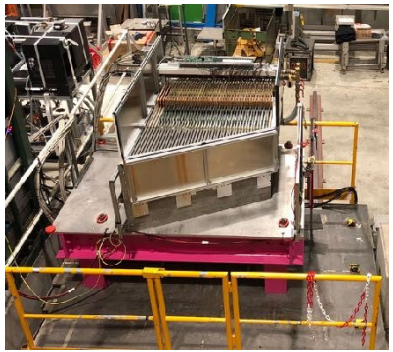
connect to information from assembly by uploading CSV files on website



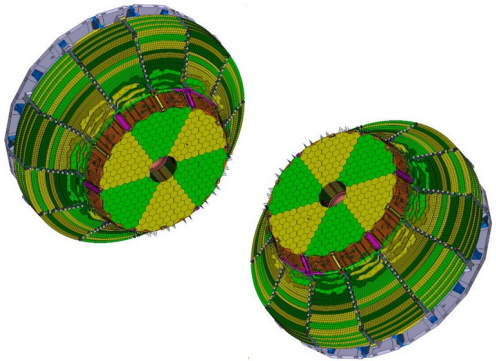
A bigger context …

- High channel count = a challenge on all levels
  - Production, test, calibration, software, management
  - 2’000 boards to be produced at DESY
  - Each step requires high degree of automation

future detectors
will only be possible
through a new level
of automation!



x10



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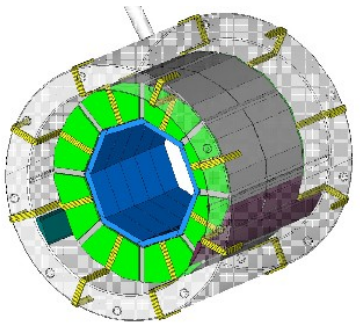


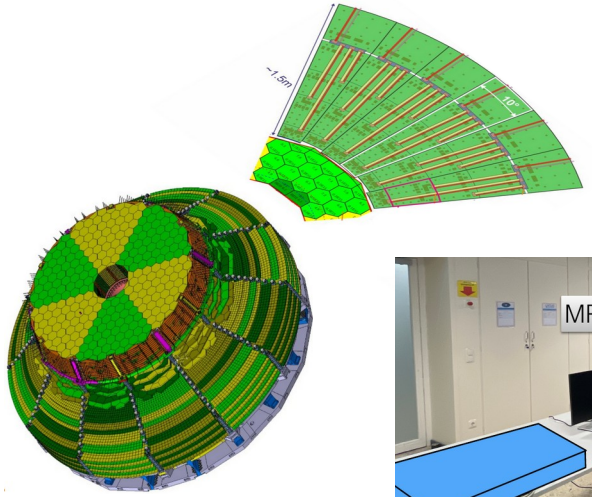
CALICE AHCAL
prototype
22’000 SiPMs

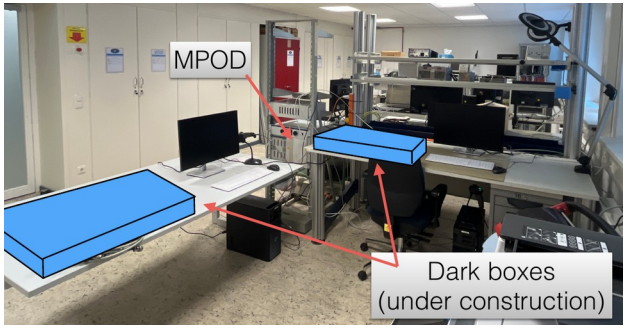
CMS HGCAL
2 endcaps
240’000 SiPMs

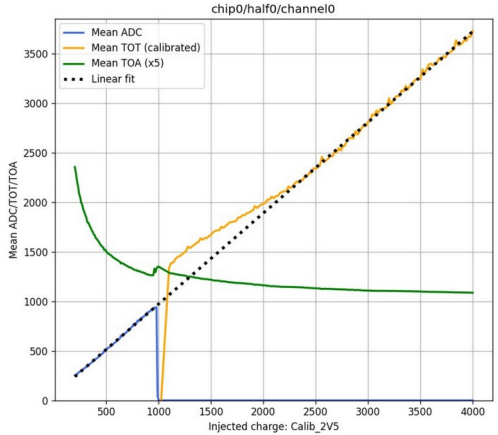
CLD/ILD HCAL
barrel only
4’000’000 SiPMs

Summary

- The CMS high granularity calorimeter (HGCAL) for HL LHC
  - Silicon & SiPM-on-tile modules
  - 2'000 SiPM-on-tile modules (150/month) to be produced at DESY
- Automatic quality control
  - Developed framework to cope with complex QC workflow (smoke test, data-handling, analysis, calibration)
  - Can be operated by non experts
  - First 36 boards QC'ed by today!!!
- Tileboard/module tracking
  - Based on Oracle APEX



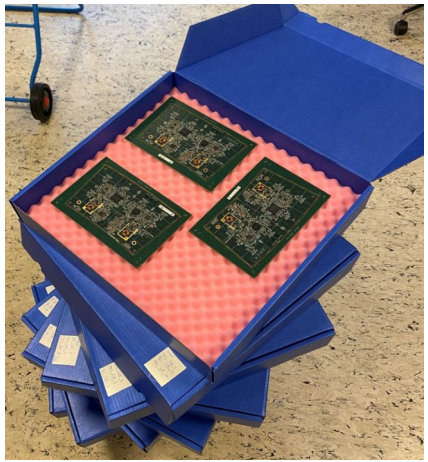


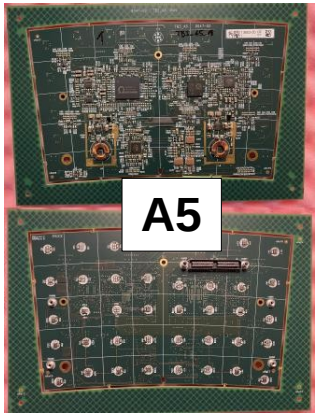


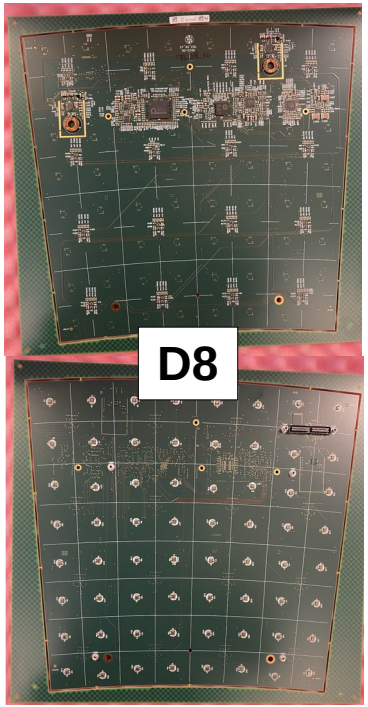
Backup

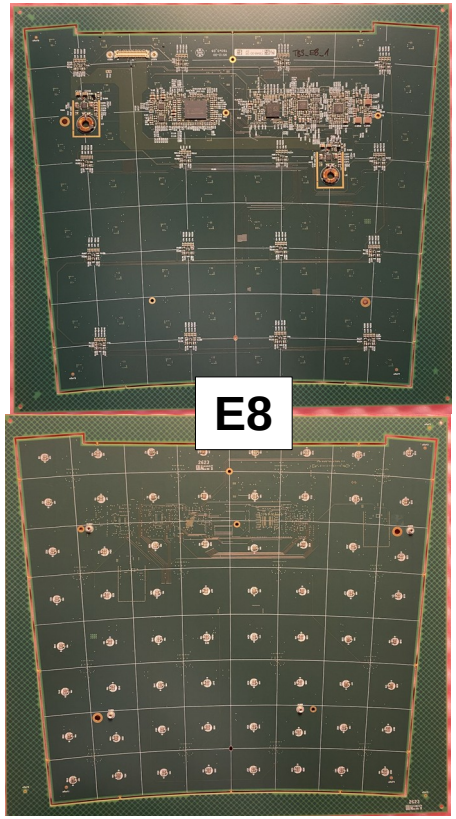
Tileboard form factors

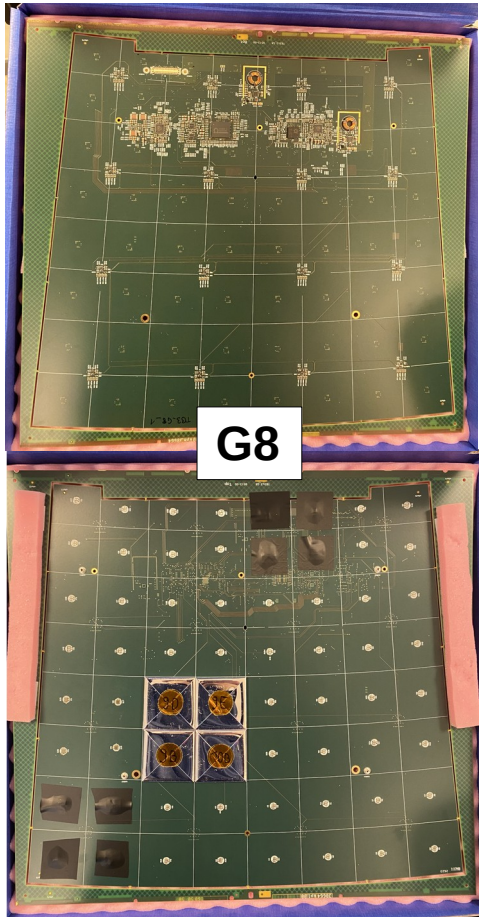
here without tiles; naked SiPMs visible



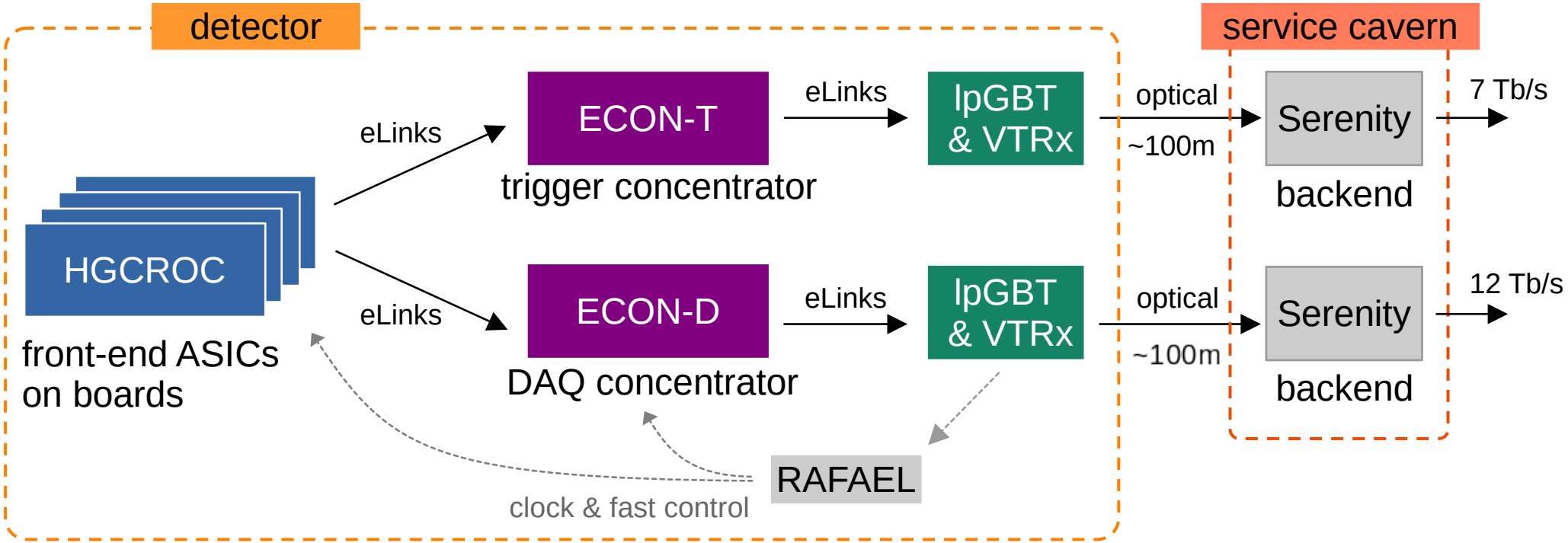








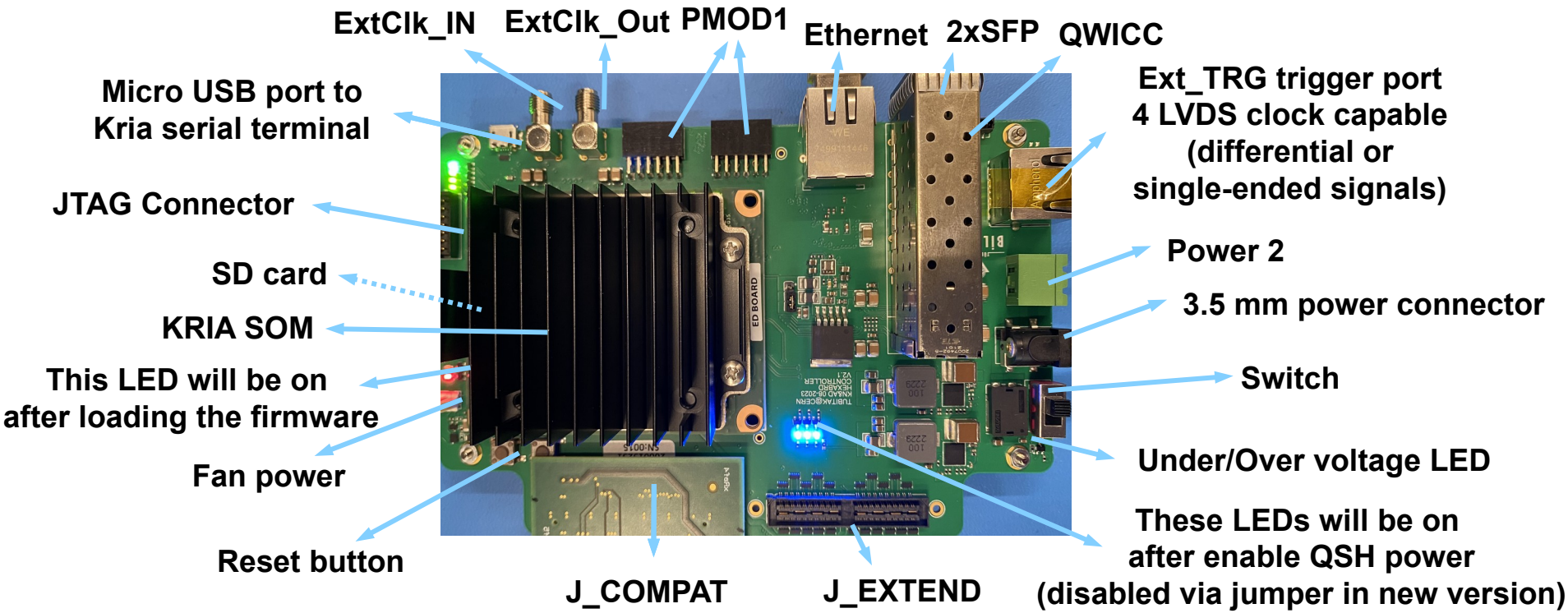
Overview: DAQ & trigger data flow



- Shared readout chain between silicon and SiPM-on-tile modules
- Trigger links continuously readout at 40MHz
- DAQ links read only on positive trigger decision (~750kHz)
- eLinks operate at 1.28 Gb/s; optical links at 10.24 Gb/s; 100 Gb/s data-to-surface links (120x)

FPGA-based DAQ

- AMD KRIA SOM (4 core Cortex-A53; Zynq UltraScale+ FPGA)
- Custom carrier board developed for HGCAL



Silicon modules

- Hexagonal shape to maximize wafer usage
- Two major layouts to equalize occupancy
  - High-density (HD): 432 channels
    $0.5\,\mathrm{cm}^2/\mathrm{pad}$; 6 HGCROC readout chips
  - Low-density (LD): 192 channels
    $1.2\,\mathrm{cm}^2/\mathrm{pad}$; 3 HGCROC readout chips
  - 9 partial layouts for edges
- Complex 6-fold rotational geometry