The OCTOPUS Project: Towards a Vertex Detector for Higgs Factories

Optimized CMOS Technology fOr Precision in Ultra-thin Silicon

Gianpiero Vignola, on behalf of the OCTOPUS project

11th Annual MT Meeting
GSI in Darmstadt, 03 November 2025

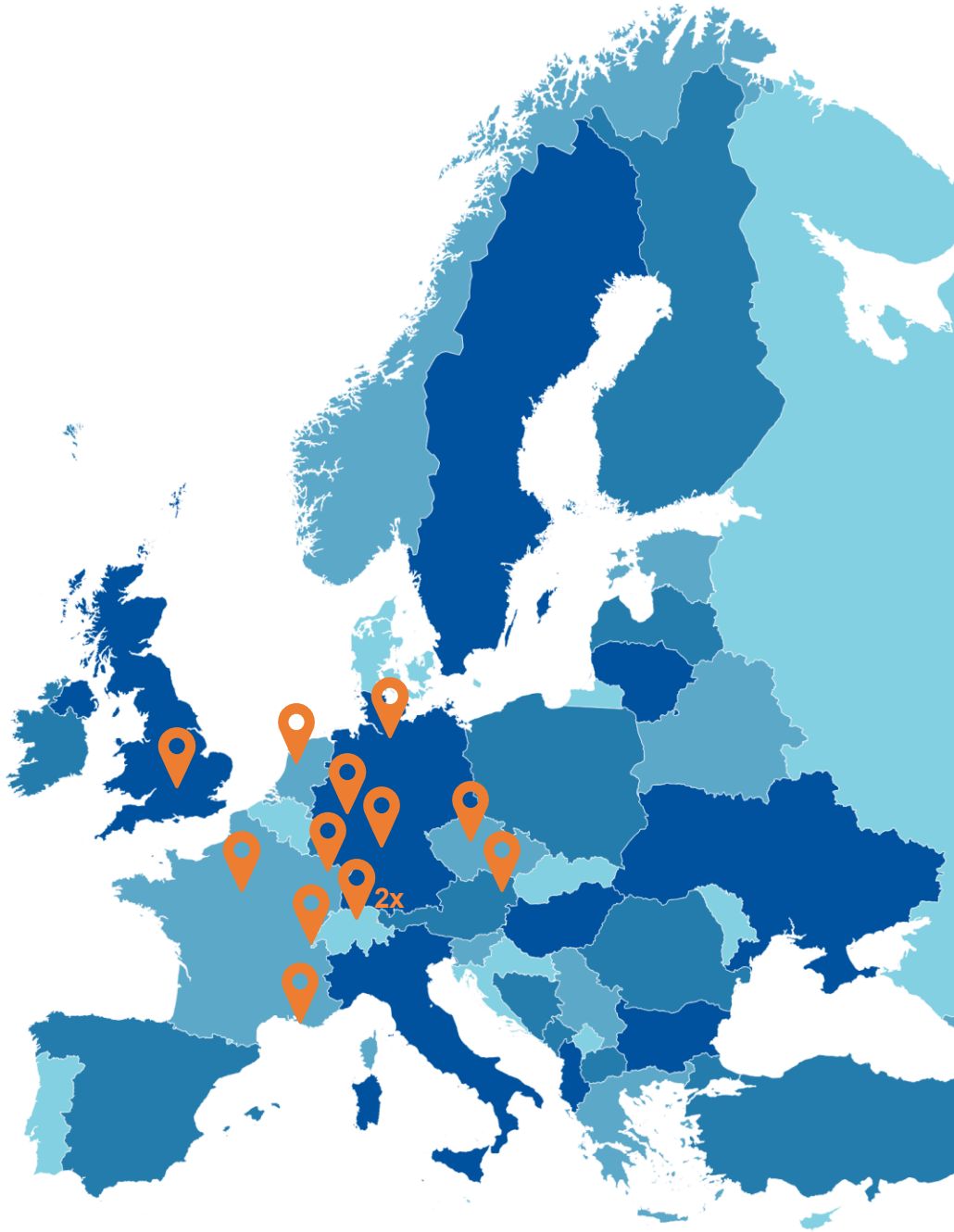
HELMHOLTZ

DESY.

OCTOPUS Institutes

International Project within DRD3 Collaboration

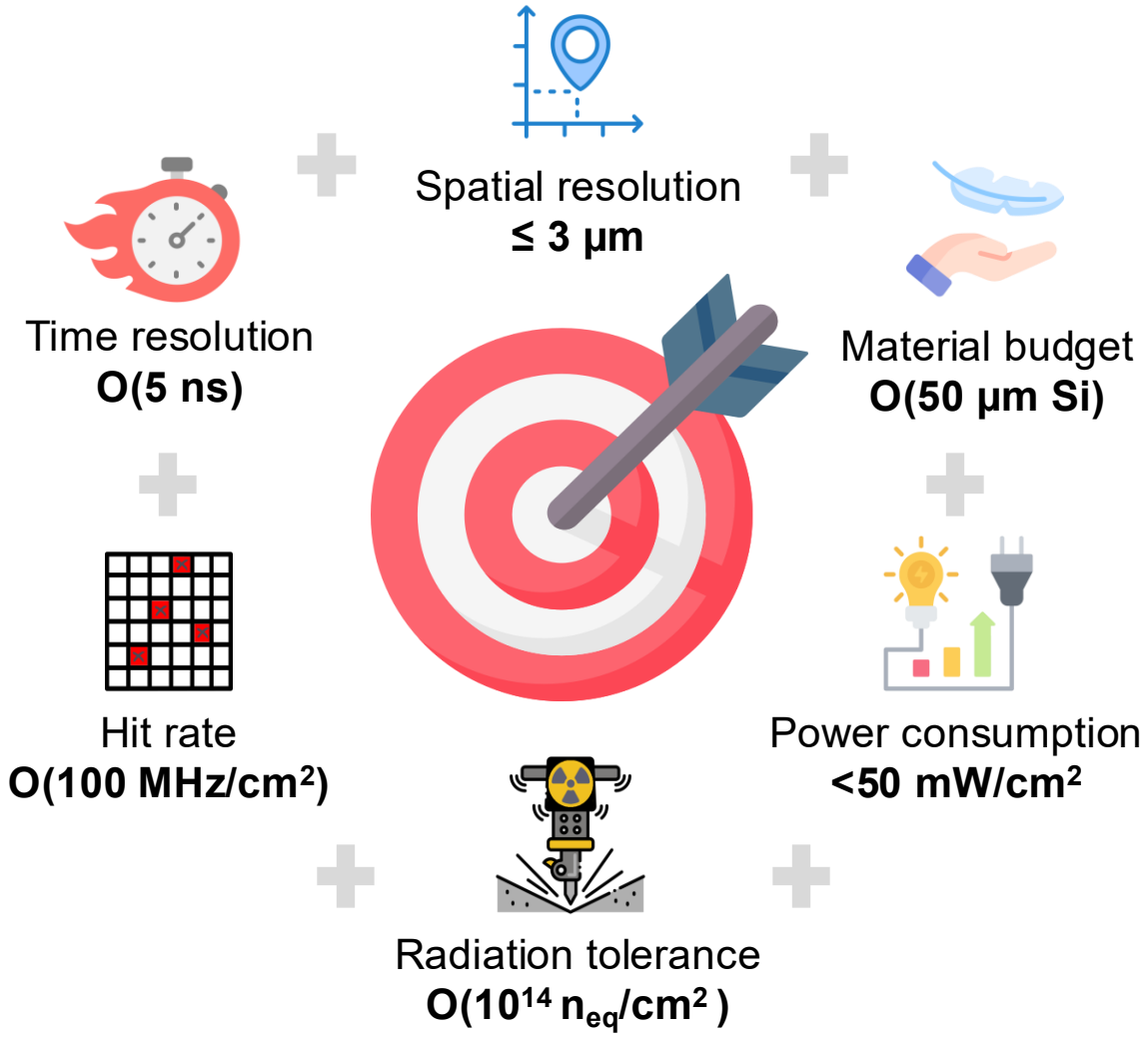
Member institutes	
APC Paris	GSI Darmstadt MT
Universität Bonn	IPHC Strasbourg
CPPM Marseille	MBI Vienna
CERN Geneva	NIKHEF Amsterdam
DESY Hamburg MT	University of Oxford
ETH Zürich	Universität Zürich
FNSPE CTU Prague	



OCTOPUS Project: Final Target

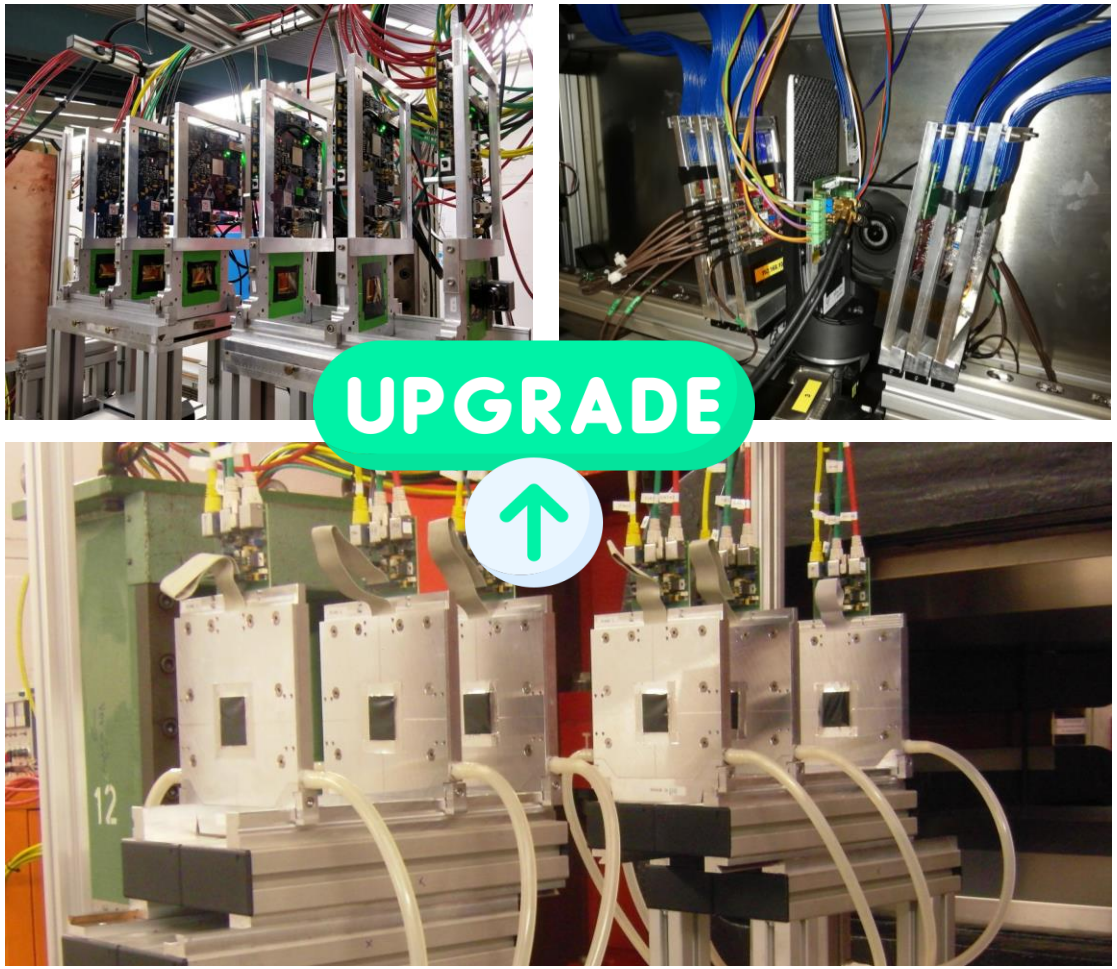
Vertex Sensor Demonstrator

- Development of a full-size sensor demonstrator for future lepton collider vertex detectors
- Target vertex-detector requirements outlined in the ECFA detector roadmap (in 2021)
- Simulate, develop, and test fine-pitch pixel sensors prototypes
- Exploiting synergies with related R&D activities and other DRD groups (DRD7, DRD8)
- Staged approach: adapting to the upcoming strategy update recommendations



OCTOPUS Project: Intermediate Target

Development of High Resolution Sensor for Beam Telescopes



Spatial resolution
≤ 3 µm

Time resolution
~~O(5 ns)~~
O(100 ns)

Material budget
O(50 µm Si)

Hit rate
O(100 MHz/cm²)

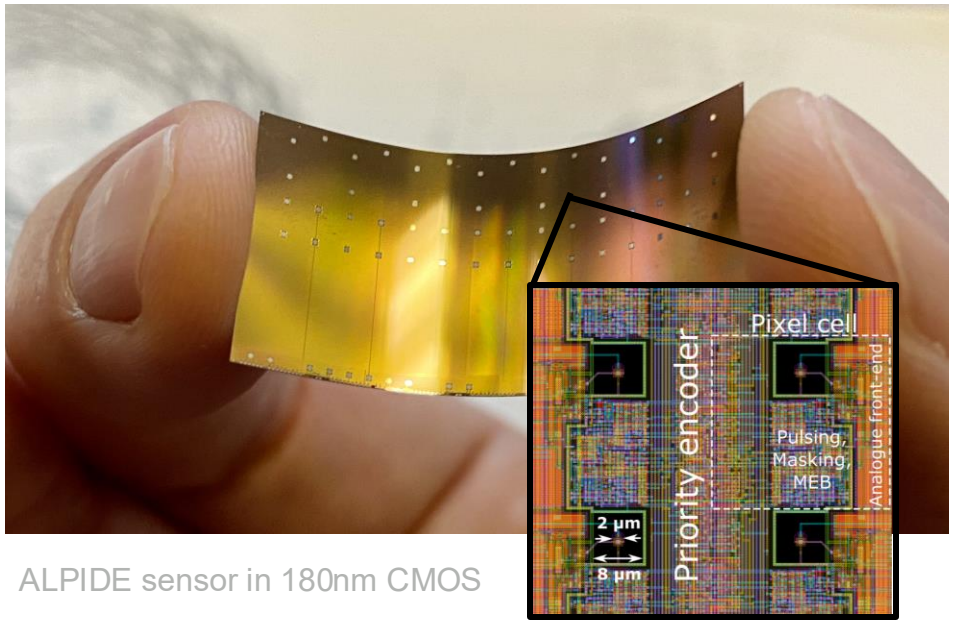
Power consumption
~~<50 mW/cm²~~
<500 mW/cm²

Radiation tolerance
~~O(10^{14} n_{eq}/cm²)~~
Not explicitly required

The Technology

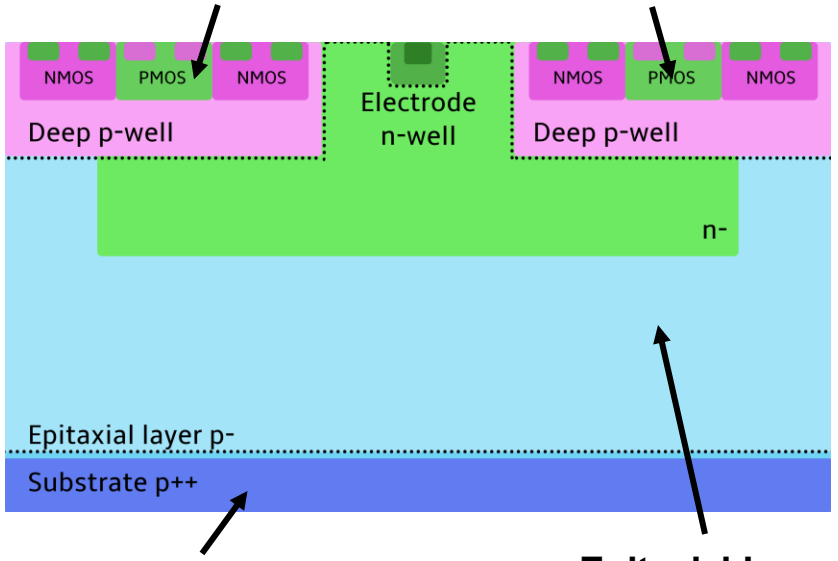
Monolithic Active Pixel Sensors (MAPS)

- Small collection electrode MAPS developed using commercial CMOS processes
- Already in use as detectors in HEP experiments
- Several R&D ongoing for the next-gen. MAPS produced using a CMOS 65 nm process



ALPIDE sensor in 180nm CMOS

Monolithic Electronics
CMOS circuits on the same silicon. No additional electronics required. Can be at pixel level (masking, amplification, discriminator, digitization, etc.) or in the sensor periphery (memory, TDCs, data serializers, etc.)



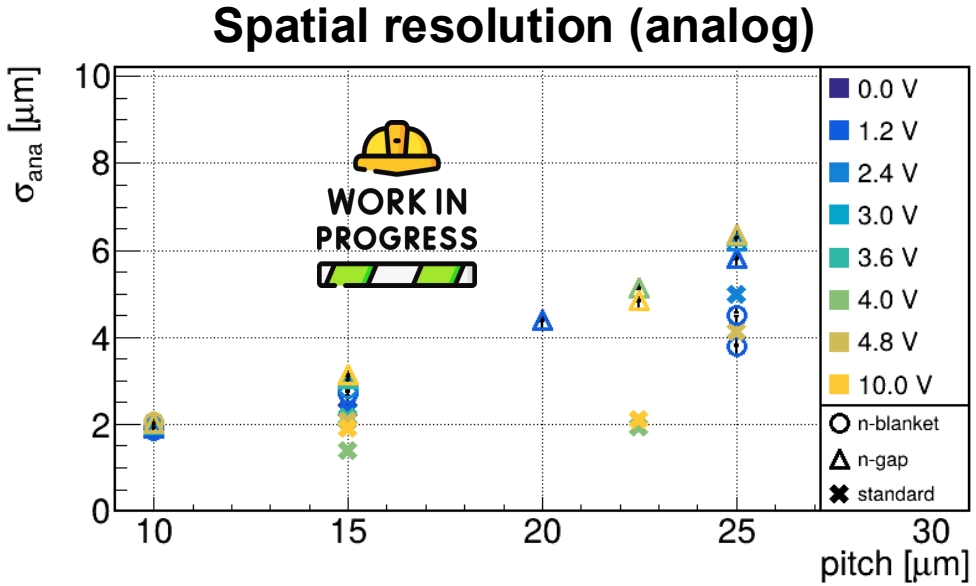
Substrate
Support wafer on which the Epi-layer was grown
~30-40 µm thick

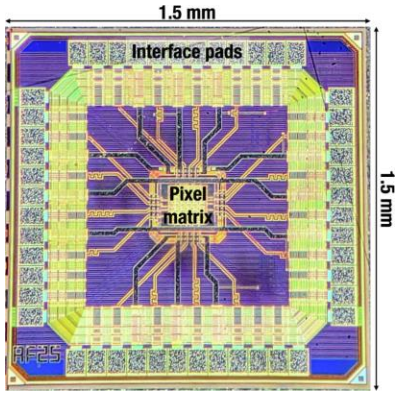
Epitaxial Layer
is the sensitive volume where impinging particles create e-h pairs via ionization
~10 µm thick

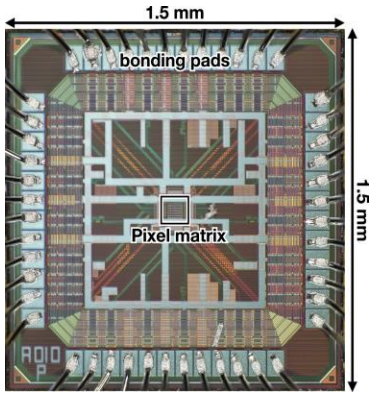
Ongoing Activities: Investigation of Previous Works

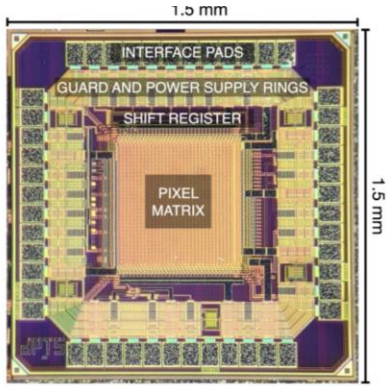
Summary Report on Sensor Produced in TPSCo 65 nm process

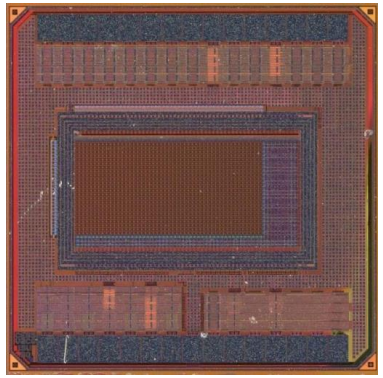
- Summarising results from recent studies on MAPS in TPSCo 65 nm process in the context of project goals
- Is the starting reference for OCTOPUS activities
- Investigated prototypes: APTS (SF-OA) [1], [2], [2], [4], DPTS [5], CE-65(V2) [6], H2M [7]

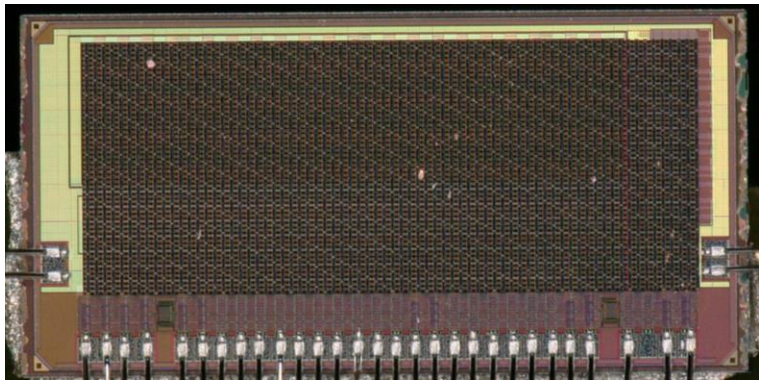












Ongoing Activities: Sensor Design Optimization

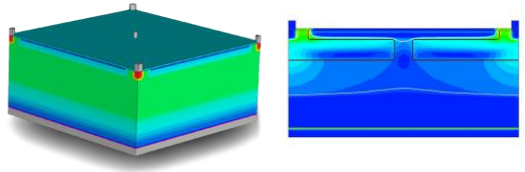
Using a Technology-Independent Simulation Approach

- Significance emphasis on simulations-based on a technology-independent approach
- Improve sensor layout by combining TCAD and Allpix^2
- Allows for an efficient and cost-effective development process by reducing the number of production iterations
- Use results from existing TPSCo 65 test chips to benchmark simulations
- Large parameter space of process variants, pitch, ToT resolution
- Trade-off between charge sharing (spatial resolution), efficiency, timing

Sentaurus TCAD SYNOPSYS® Silicon to Software™

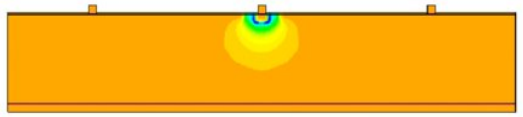
+

ap² allpix squared



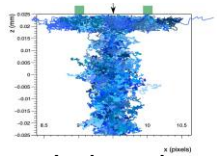
Generic doping profile

Realistic electric field

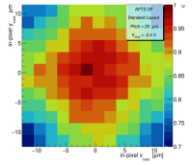


Weighting potential

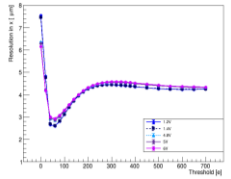
Particle interaction



Induced Signal



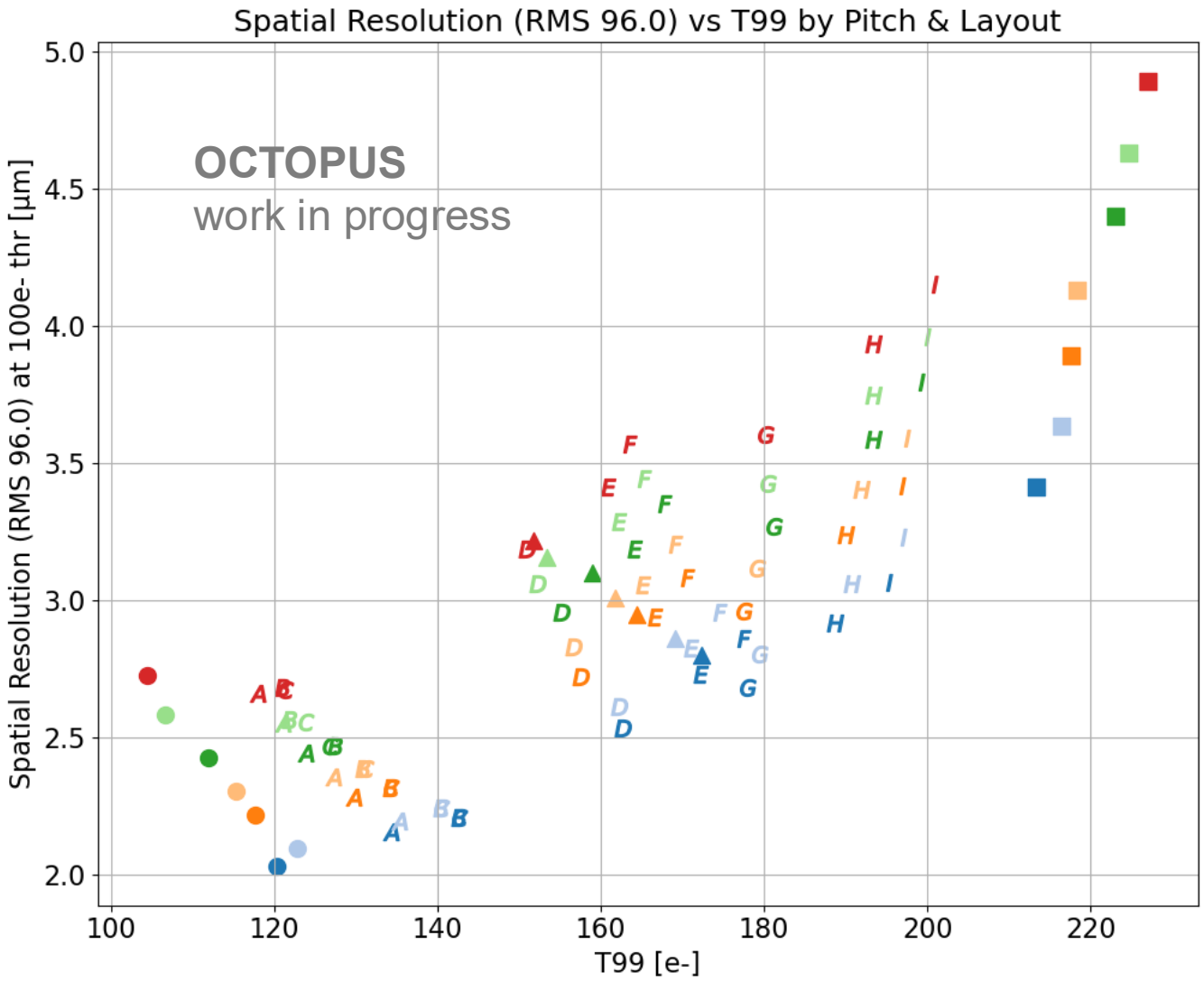
Efficiency



Spatial resolution

Ongoing Activities: Sensor Design Optimization

Preliminary Simulations Results

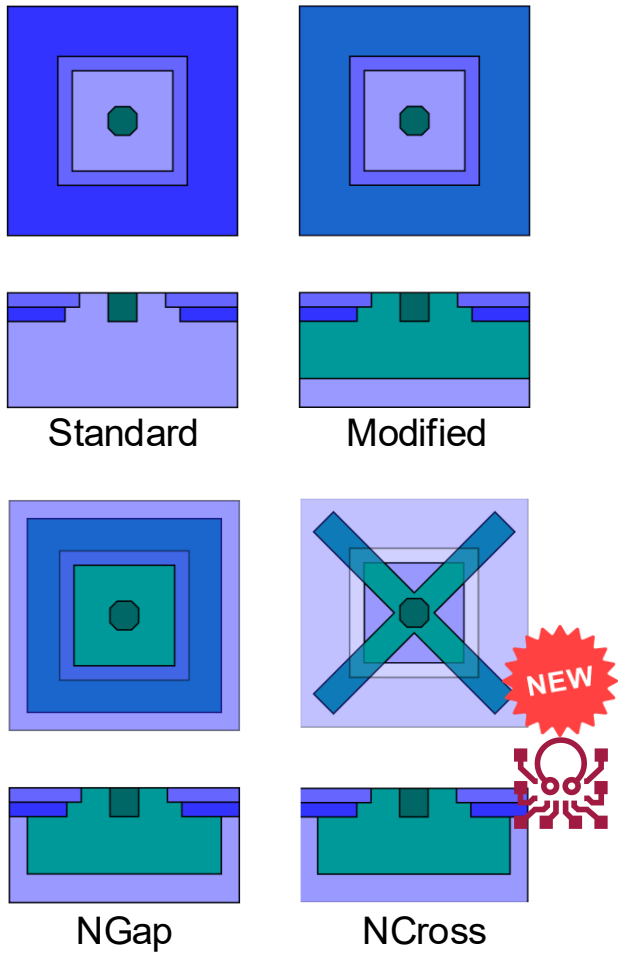


Pitch
- 15um
- 16um
- 17um
- 18um
- 19um
- 20um
- 21um

Layouts
- Standard layout
- NGap layout
- Modified layout

NCross
- A A=0.5, B=high
- B A=1.0, B=high
- C A=1.5, B=high
- D A=0.5, B=medium
- E A=1.0, B=medium
- F A=1.5, B=medium
- G A=0.5, B=1.0
- H A=1.0, B=1.0
- I A=1.5, B=1.0

Sensor Layout Variants

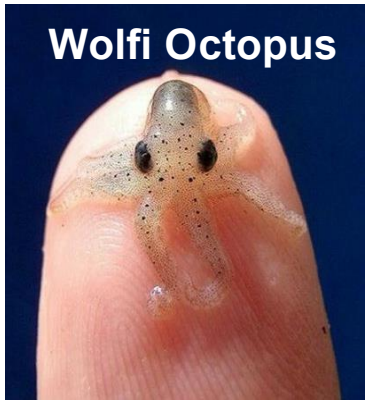


Ongoing Activities: ASIC Concept and Design

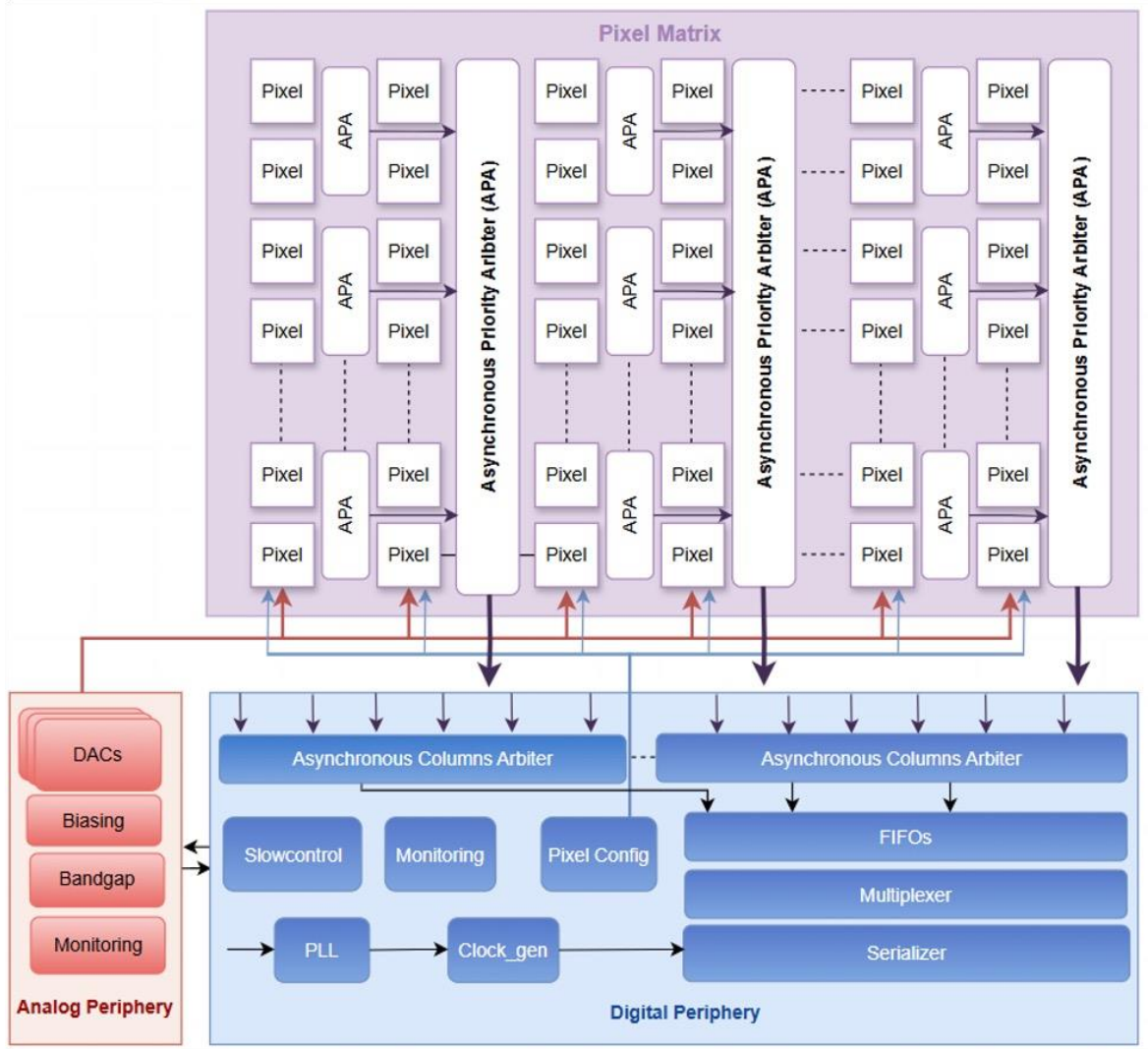
In Preparation for First Submission

WOLFI: First Large Scale Prototype concept

- Aiming for a full column height with flexible width
- Active Matrix with minimal intelligence
- APA (Asynchronous Priority Arbiter) readout of matrix with pixel grouping
- All biasing from the bottom of the chip



Wikipedia



Ongoing Activities: ASIC Concept and Design

In Preparation for First Submission

Front end

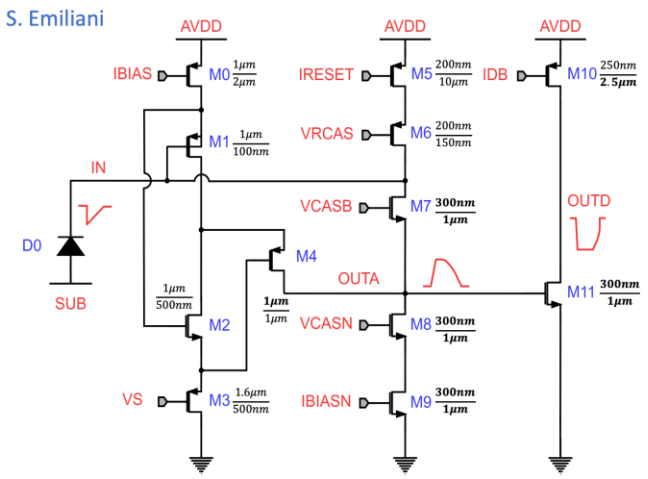
- FE based on MOSAIX, compact amplifier
- Sample rising and falling edge for offline ToT measurement
- Small footprint required to reach the target spatial resolution

Matrix readout: APA - Asynchronous Priority Arbiter

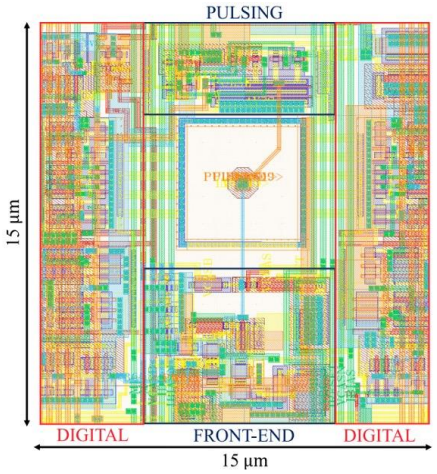
- Compact, low-power solution for high rate readout
- Moderate impact on time resolution, no time stamping clock in matrix
- 65nm proof-of-concept prototype (SPARC) already submitted

End of column & serializer

- Time stamping of hits after APA in end of column and buffer
- Focus on bit-efficiency in data transfer, limit TS and address bits
- lpGBT logic as preferred option, 40 to 50 Gbps for the reticle size chip

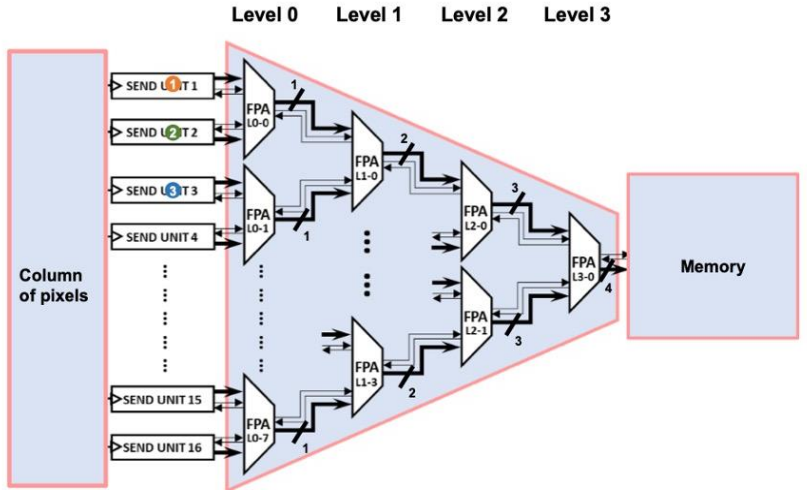


https://indico.cern.ch/event/1461789/



DPTS Pixel: 15 µm x 15 µm

F.Piro, A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology, 09.09.2023, IEEE Transactions on Nuclear Science

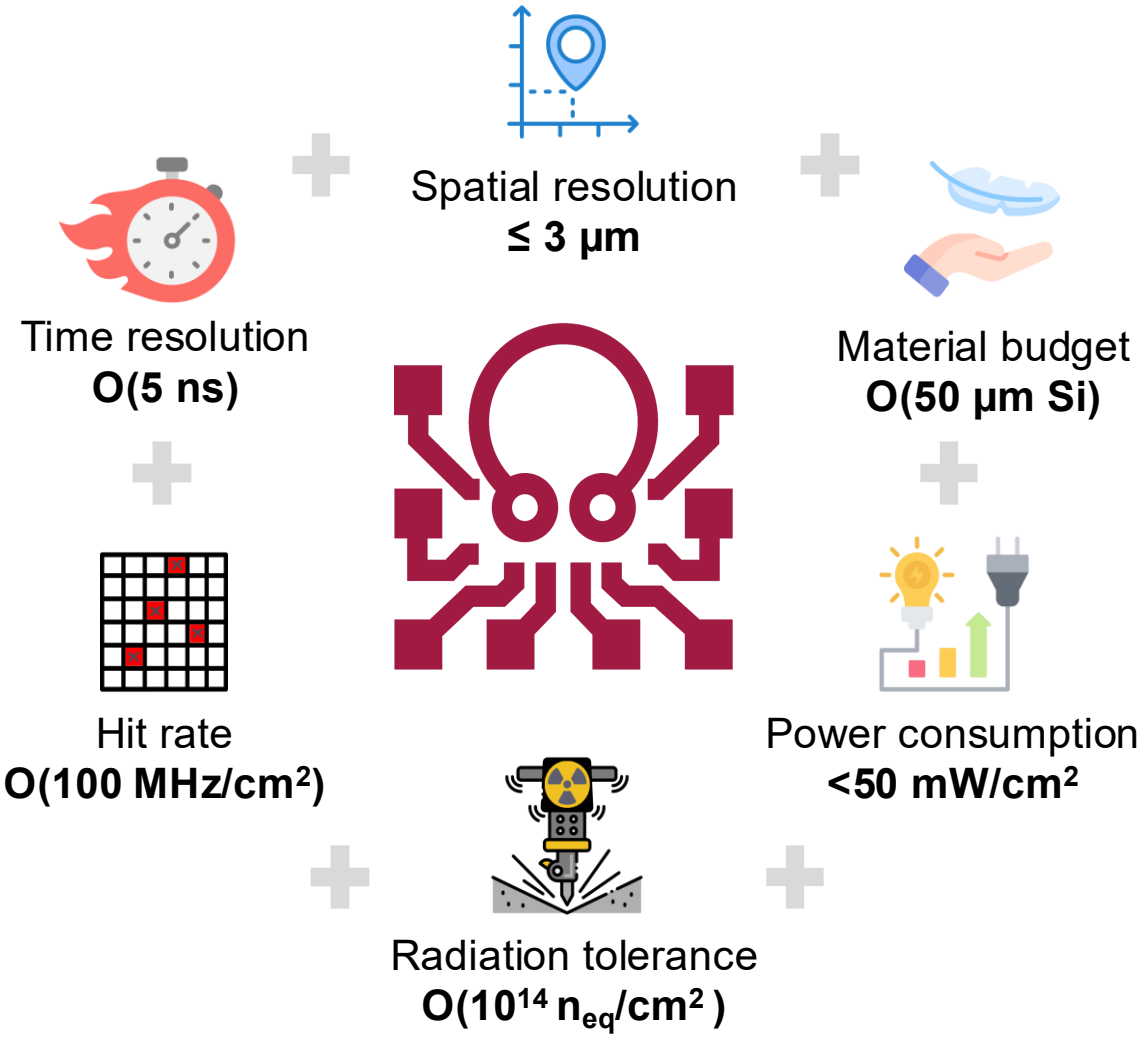


APA structure

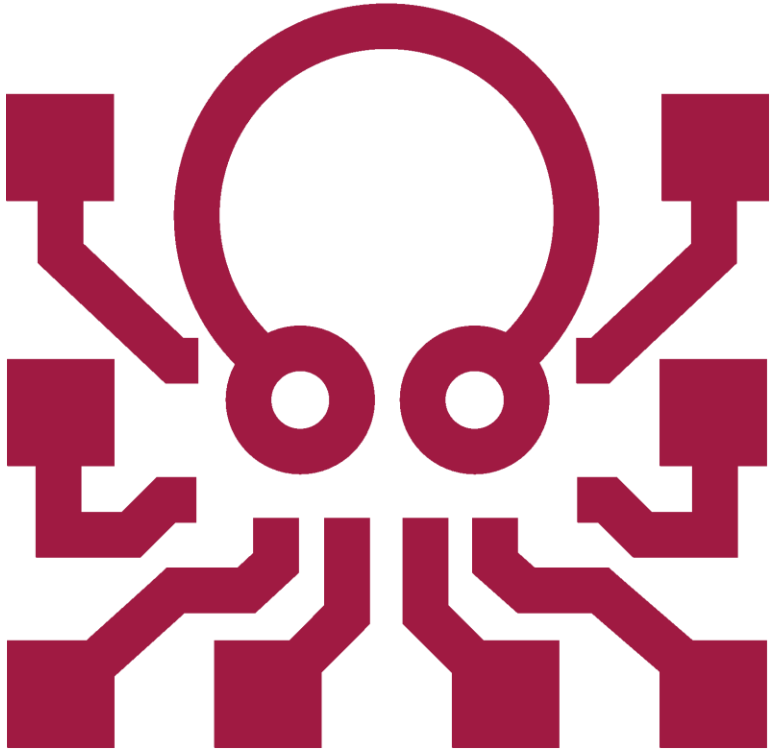
Summary & Outlook

Towards Lepton Collider Vertex Detector Demonstrator

- OCTOPUS aims to develop a reticle size MAPS vertex sensor demonstrator for future lepton colliders
- Staged approach, profiting from previous TPSCo 65 nm work and exploiting synergies
- Particular emphasis on simulations to enable efficient and cost-effective development process
- Exploring innovative options for sensor layout and matrix readout to achieve goals
- First large-scale prototype WOLFI In preaparation
- SPARC prototype to test APA is in production and will be tested by OCTOPUS in the coming months
- Investigations ongoing for first submission in 2026



Thank you.



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OCTOPUS Project Structure

Four Workpackages

WP1: Simulations

- TCAD simulations: sensor optimization
- Allpix^2 simulations: detector performance
- Contribution to Allpix^2 development
- Physics performance and geometry optimization

WP2: ASIC

- Pixel front-end and matrix architecture design
- Periphery, DACs & slow control design
- Transceivers and readout design
- Chip integration and verifications
- Submission coordination & interface with DRD7

WP3: Data Acquisition

- Chipboard design for prototypes & DAQ integration
- Chip/board assembly, bonding & logistics
- Contribution to Caribou development

WP4: Testing & Characterization

- Summary of current TPSCo65 demonstrator results
- Lab characterization, FE optimization, calibration
- Testbeam characterization, performance