ECFA
European Committee for Future Accelerators

DRD7.6b

MATTER AND TECHNOLOGIES

11th Annual MT meeting
Nov 3 – 6, 2025, GSI

DRD 7.6b
Shared Access to 3D Integration

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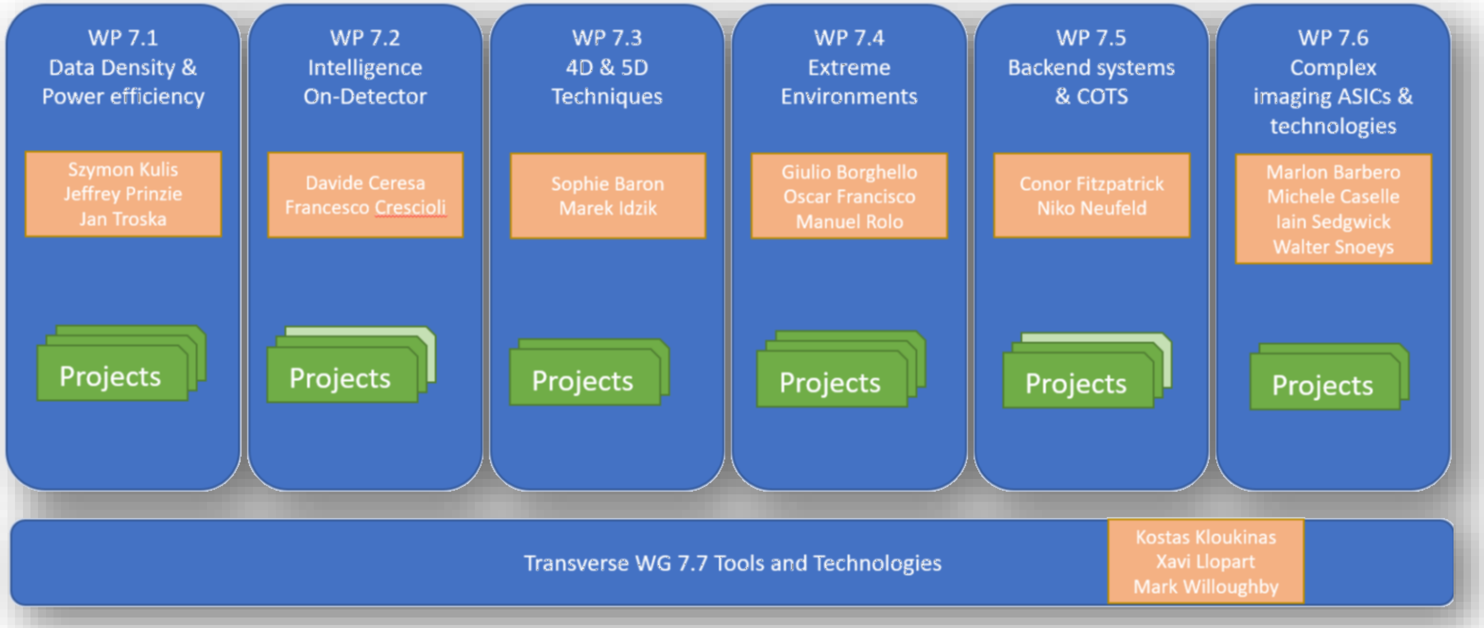
DRD7.6b

https://drd7.web.cern.ch/

https://indico.cern.ch/event/957057/overview

From ECFA Roadmap TF 7 to DRD7 collaboration (Electronics and On-detector Processing)

- The DRD7 collaboration is a concrete and dynamic R&D program focused on the development of critical detector technologies for future large-scale experiments, as identified by the ECFA Detector R&D Roadmap Task Force 7.



21 countries

- **64** Universities & research centers involved, **15** confirmed projects cover a wide range of novel detector technologies
- Research area: Data Density, Power efficiency, Intelligent On-Detector, 4D & 5D techniques, rad-tolerant and cryo-tolerant electronics, backed electronics/systems and COTS (Commercial-Off-The-Shelf), complex imaging ASICs & 3D-technologies

DRD7.6b

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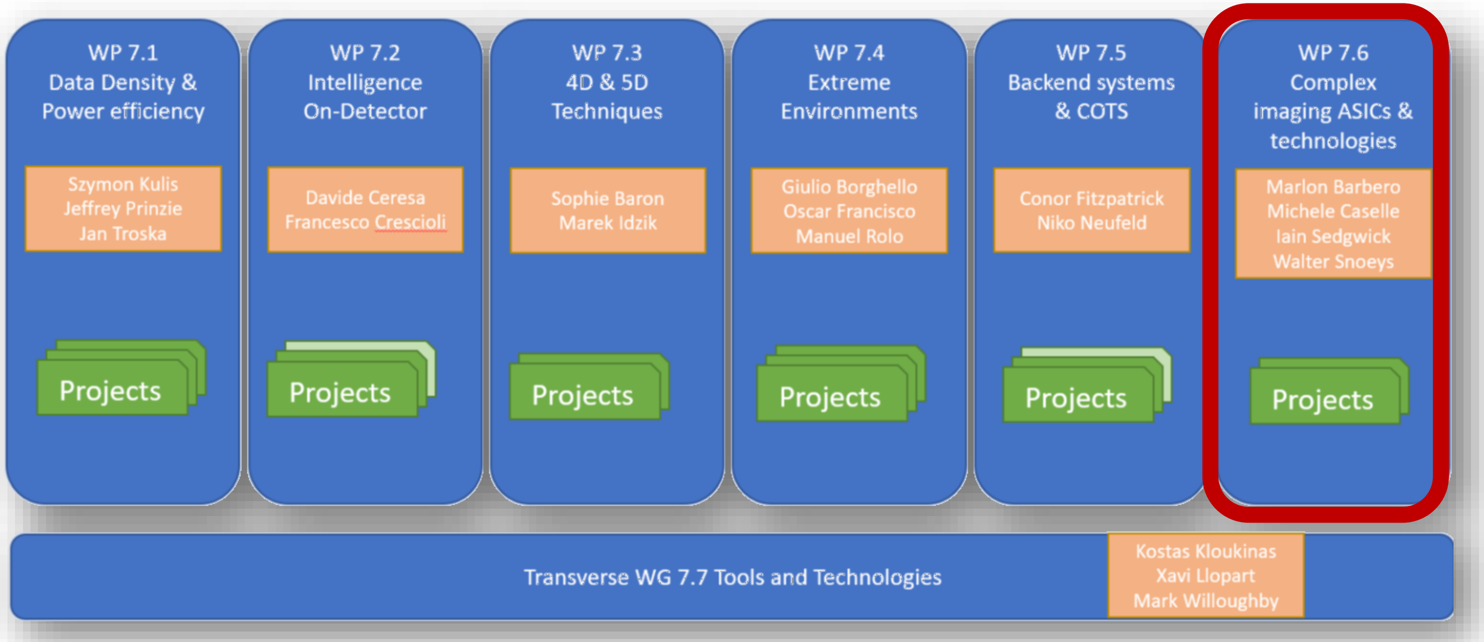

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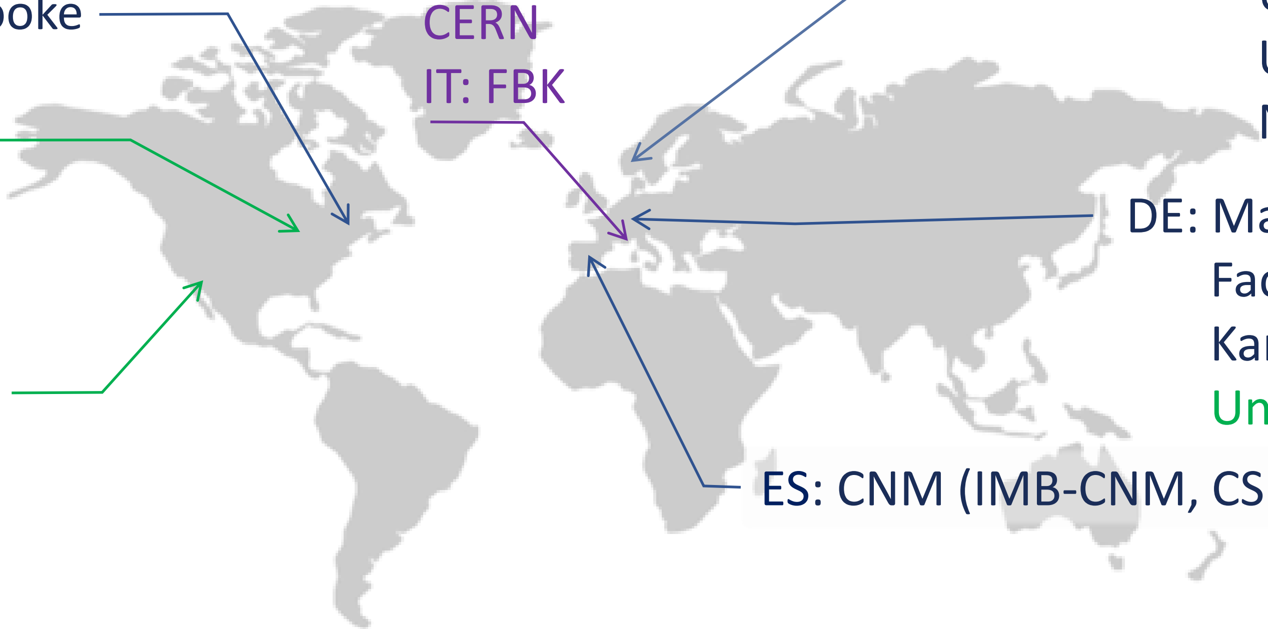
DRD7.6 – Complex imaging ASICs and technologies

- Working Package 6 deals with complex technologies merging multiple functionalities such as sensor and processing, multi-tier (2.5D and 3D) assemblies

- **Project 7.6a** → *Conveners: M. Barbero, M. Rolo, I. Sedgwick and W. Snoeys*
  - This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs. These are initially envisaged for the TowerJazz 180 nm, TPSCo 65 nm and the LFoundry 110 nm CMOS imaging technologies

- **Project 7.6b (Shared access to 3D integration)** → *Convener: M. Caselle*
  - This project aims to develop essential technologies for both 2.5D and 3D integration that can be quickly transposed to wafer-to-wafer 3D integration for a wide range of future particle physics applications, ranging from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors

DRD 7.6b - Collaboration *Update*



- Institutes that actively contribute to the project
- Institutes in the process of joining as contributors
- Institutes joining as observers

15 institutes, 5 large national labs with well-renowned experience in interconnection technology and detector production

DRD7.6b – Shared Access to 3D Integration

- Today, 2.5D Chiplet architectures and 3D W2W integration stand at the forefront of microelectronics innovation, driving progress across both the semiconductor industry and the consumer market

- 2.5D and 3D integration technologies are a key enabler for the assembly of future detectors

2.5D and 3D are expensive
(especially for prototype)

Only a few vendors are willing to produce small-volume prototypes at a reasonable cost

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- Leverage in-house infrastructure and expertise for the rapid fabrication of high-value prototypes, demonstrators, and test vehicles
- Provide access to the community and ensure long-term availability of the technologies
- Forge strong, concrete links with industrial partners

Enable technologies to be quickly transposed to industrial partners

DRD7.6b

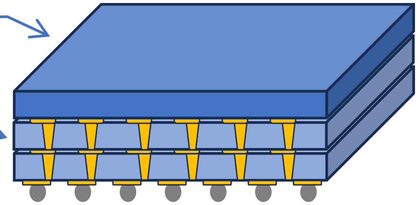
Which are the key technologies that are expected to have a disruptive impact on the detector community?

Enabling Technologies and Main Objectives

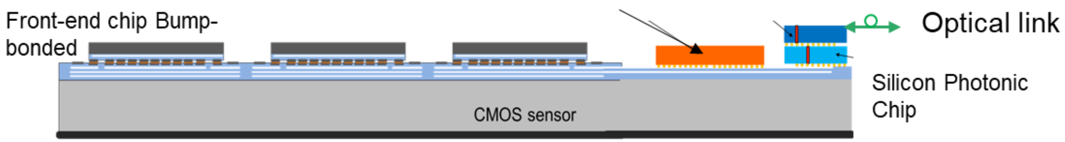
- **3D-ASIC integration on a single die** as a low-cost, low-risk demonstrator that paves the way to future large-area 3D-ASIC detector modules assembled via (expensive) wafer-to-wafer (W2W) bonding

Monolithic sensor (TJ, TPSco, LFoundry)

Digital memory + processing (65/28nm TSMC, UMC, etc.)



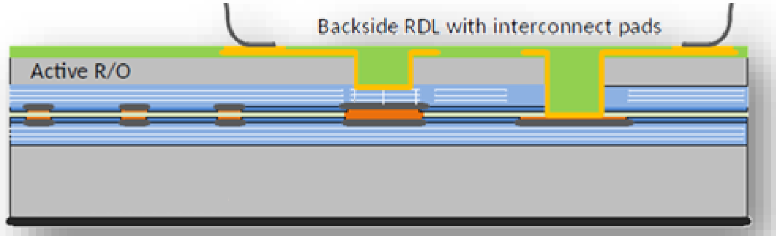
- **Silicon interposers** are the key enabler to integrate sensors, ASICs, FPGA/AI, and photonics from multiple CMOS nodes into a unified, scalable detector module



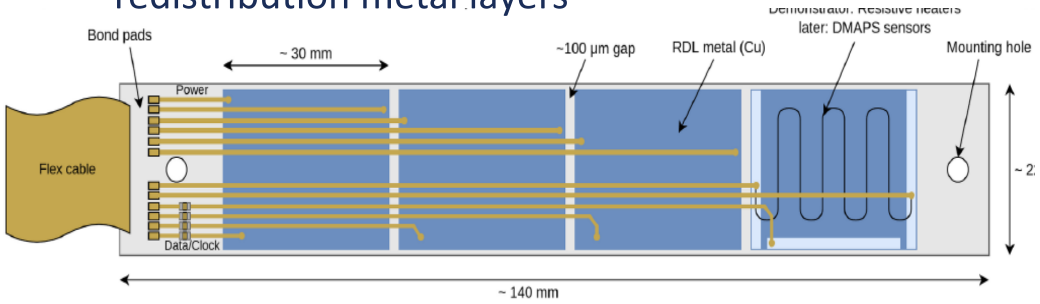
- **Large-area detector modules** on wafer level based on ultra-low mass, ultra-thin large-area detectors in future experiments

Monolithic LGAD

Digital front-end 65 or 28 nm CMOS

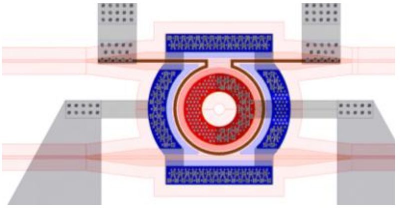


How can the connections of large-area detector modules be improved by using one or multiple redistribution metal layers



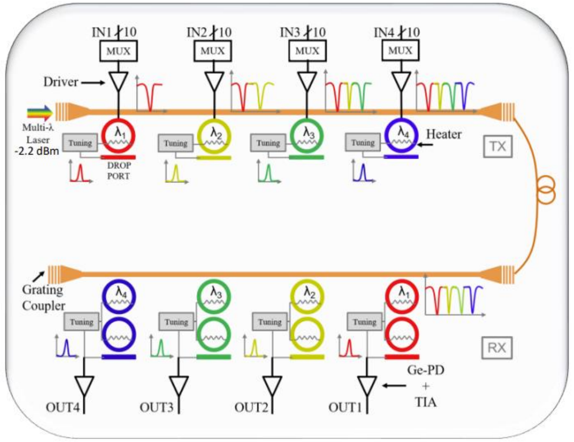
SiPh Packaging & Fiber Attachment

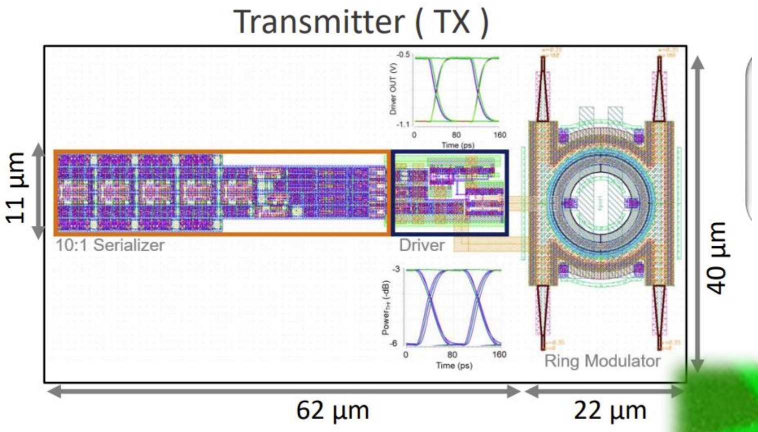
- SiPh packaging and fiber-attachment, at detector-module or wafer level. Automated fiber alignment using pick-and-place machines further enhances assembly precision and throughput

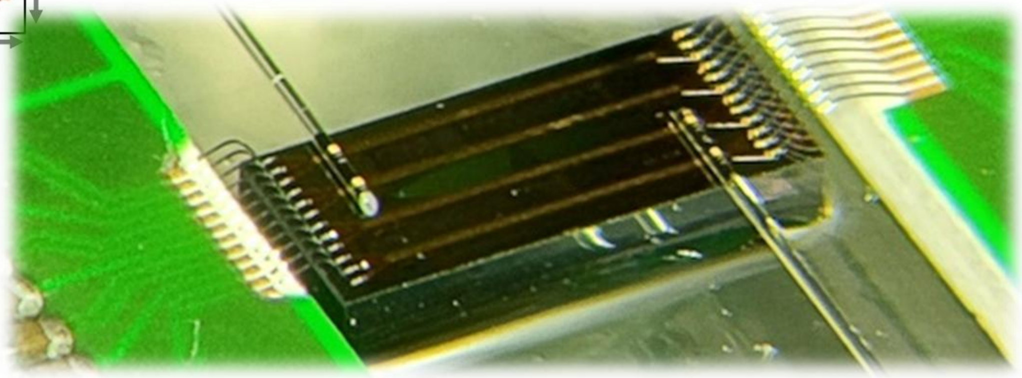


Ring modulator
Courtesy Marc Schneider (KIT)

Source: Karsten Hansen (DESY)







Courtesy Marc Schneider (KIT)

Helmholtz InnoPool Project ‘Sophie’
Partners: DESY, GSI, and KIT”

How can we work together ?

Collaborative Concept:
By joining forces, sharing competences, and pooling infrastructure, we can accelerate technology development and grow collective capabilities

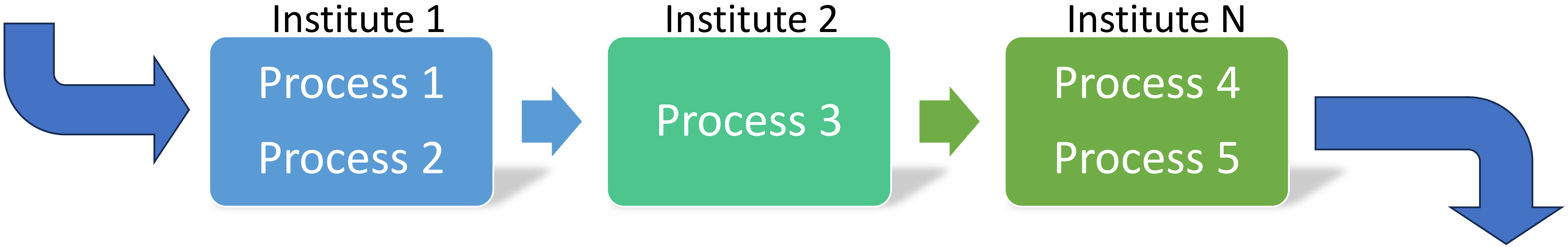
DRD7.6b

International Distributed Detector Laboratory

- Establish a distributed laboratory that operates as a hub-service for the community
- Each institute highly specialized in one or more technological processes

<u>From community</u>:
- Request of process/service
- Rapid prototyping of new detector
- Detector production (large scale)

Key parameters, are:
- Interface between institutes/processes
- Redundancy
- Complementary
- Development of new processes that are not currently in place



Maintaining a strong connection with application/experiment requirements

<u>To community</u>
(institute/experiment)

Pilot Project to validate and implement distributed workflow (ECFA-DRD7.6b-2025)

The Pilot Project is a full-wafer engineering run, entirely developed and fabricated in-house by DRD 7.6b contributors

- **Define interfaces across institutes and laboratories –** Develop clear and standardized communication channels, processes, and operational protocols to ensure seamless collaboration and integration

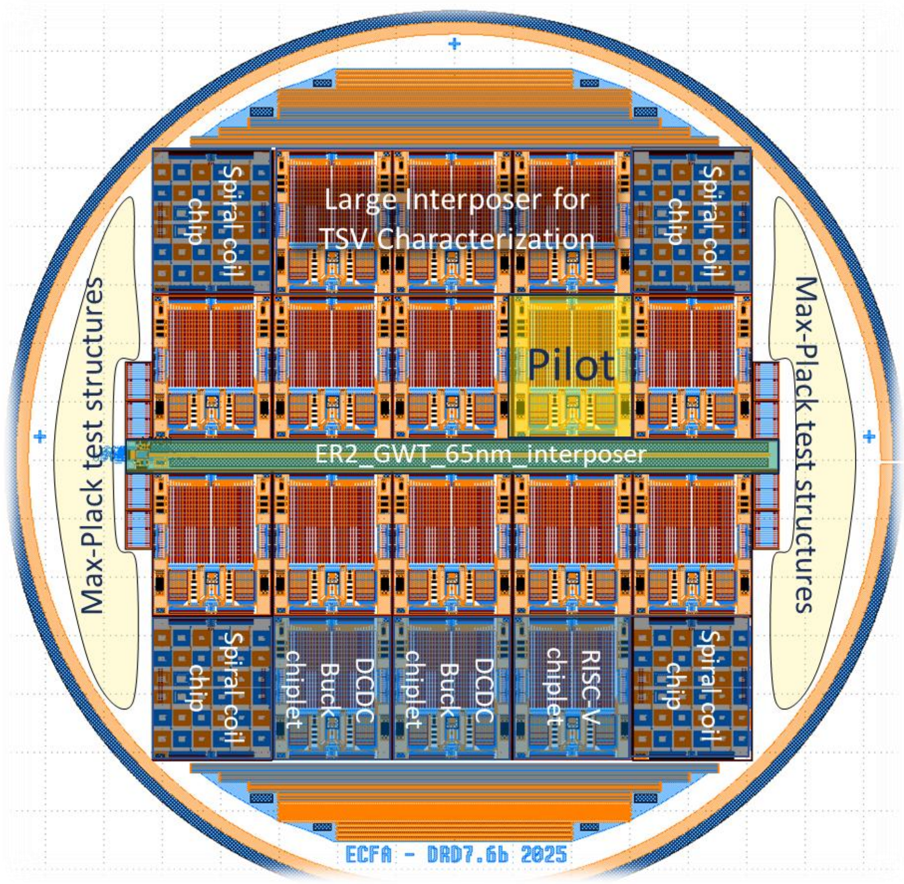
- **Identify potential incompatibilities** – Detect mismatches in processes, technologies, or tools early in the workflow

- **Develop and implement solutions** – Address incompatibilities with efficient and practical resolutions to maintain production consistency

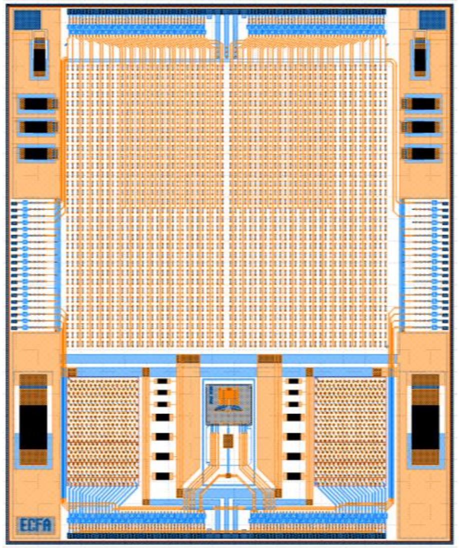
Pilot Project to validate and implement distributed workflow (ECFA-DRD7.6b-2025)

The Pilot Project is a full-wafer engineering run, entirely developed and fabricated in-house by DRD 7.6b contributors

- Simple enough to efficiently validate the distributed workflow
- **Key structures are**:
  - **Pilot Project** to assess chiplet integration, providing insights toward the development of TSVs and RDL capabilities. Thermal and mechanical studies and signal integrity over **large areas** (wafer scale)
  - **ER2_GWT**_PSI chiplet designed for testing of the 10.24 Gb/s GWT-PSI serializer embedded in the **MOSAIX** stitched sensor ASIC
  - **RISC-V / AI accelerator** chiplet for AI-detector module
  - High-Frequency **DC-DC Buck** converter as a showcasing power management integration



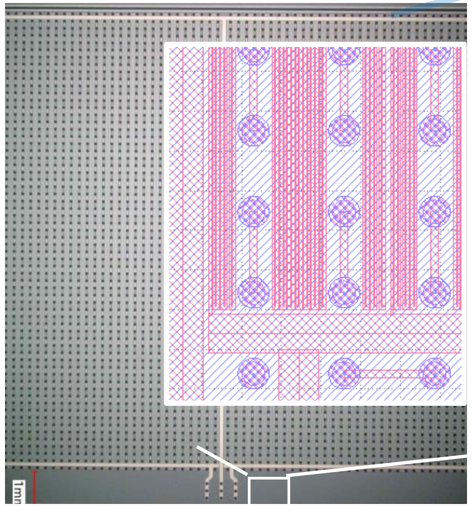
6-inch wafer size

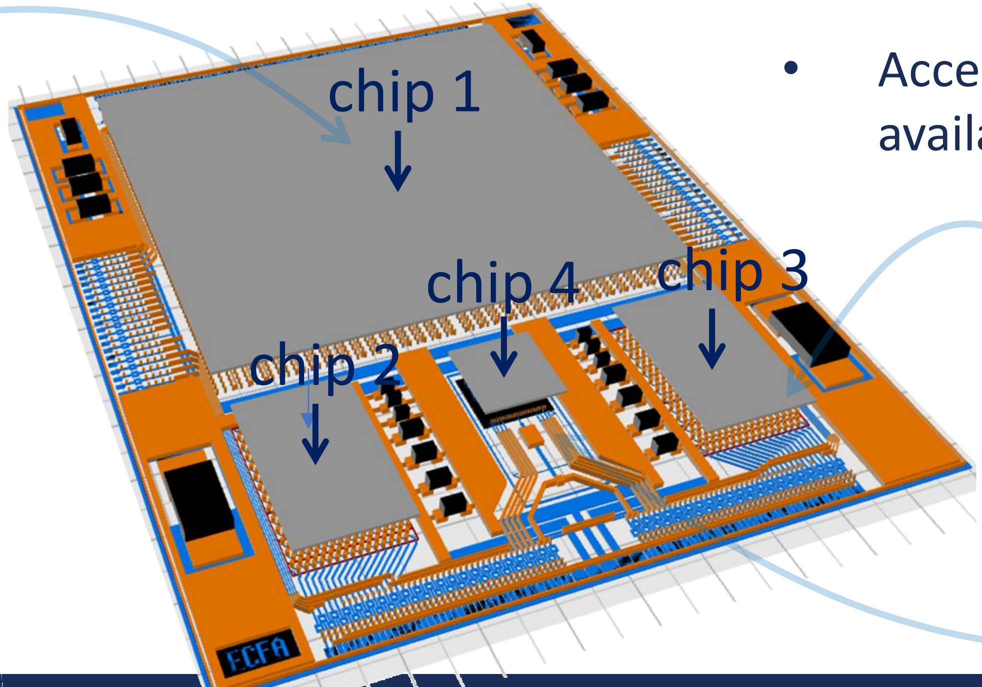


Layout

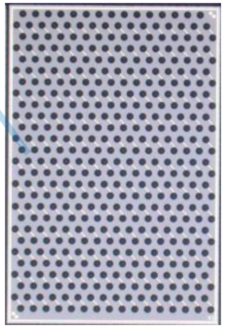
Pilot Project – Interposer

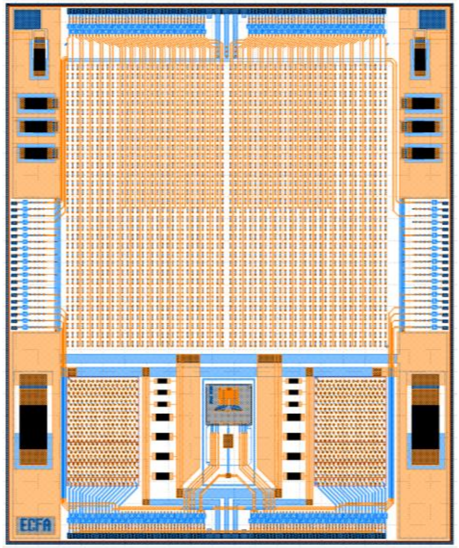
- **Key Features**:
  - Four chips bump-bonded with different bump pitches down to 50 µm, with full bump-to-bump daisy-chain provided for electrical testing and characterization
  - Integrated on-chip heater system to simulate power consumption





- Accelerate the project by using available chips from Max Planck (HLL)

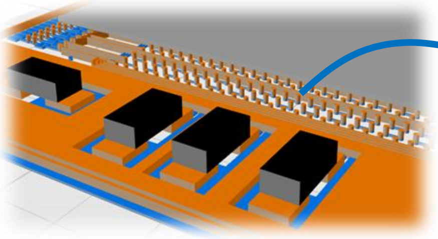




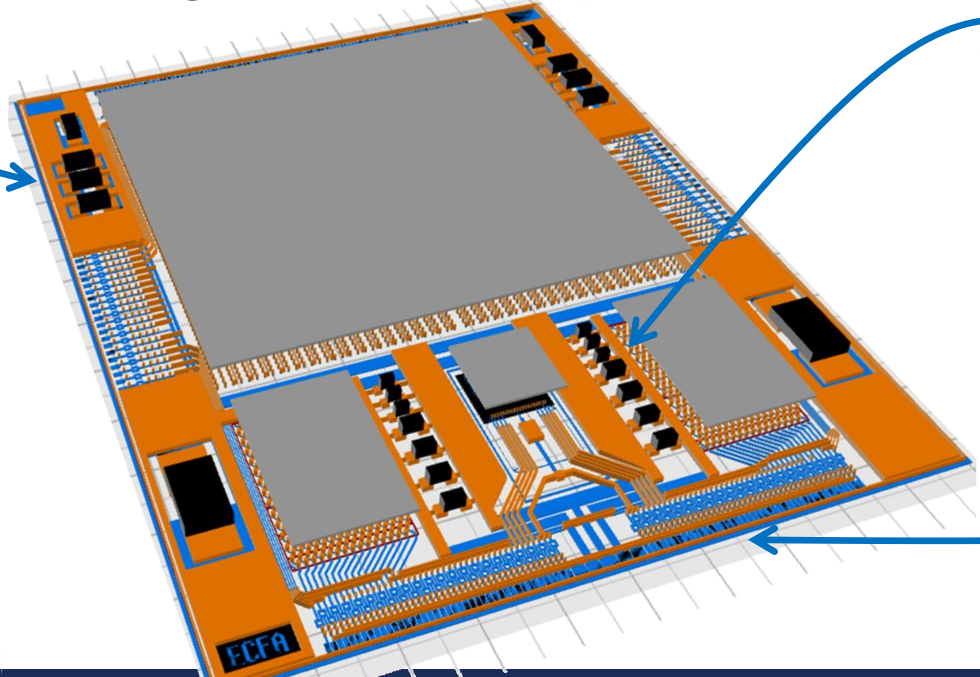
Pilot Project – Interposer

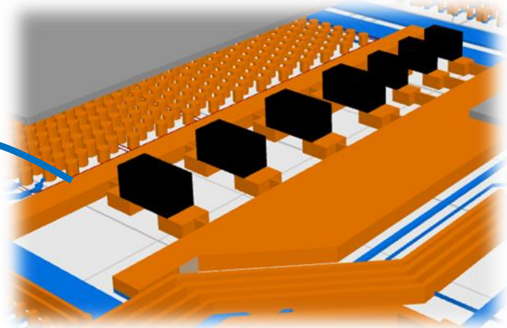
Additional detail → parallel session

- **Key Features**:
  - SMD components assembled in multiple package sizes (ranging from 0805 to 01005)
  - Ti/W-Cu redistribution layer (RDL) implemented and Ti:W/Cu UBM
  - Openings prepared for Through-Silicon Via (TSV) formation

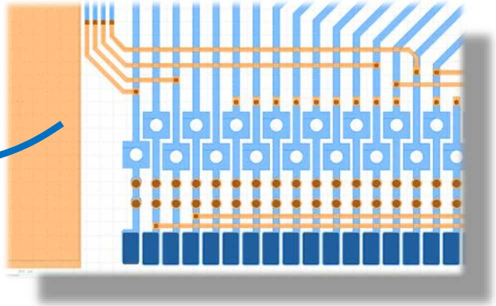


SMD 0805 & 0402
(soldered on Al/Si by UBM)





SMD 0201 & 01005
(soldered on RDL Cu-layer)



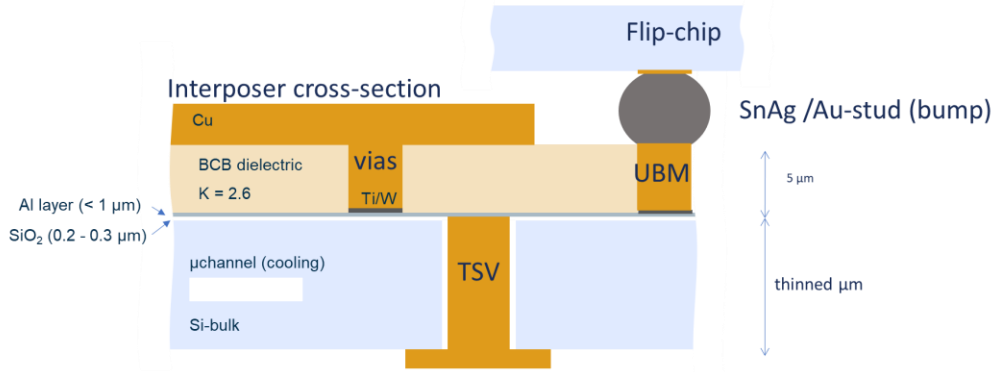
DRD7.6b Pilot Project - Fabrication workflow

Chiplet Designers → Wafer Layout → Al/RDL (Cu) → Flip Chip → Mechanical/Electrical tests

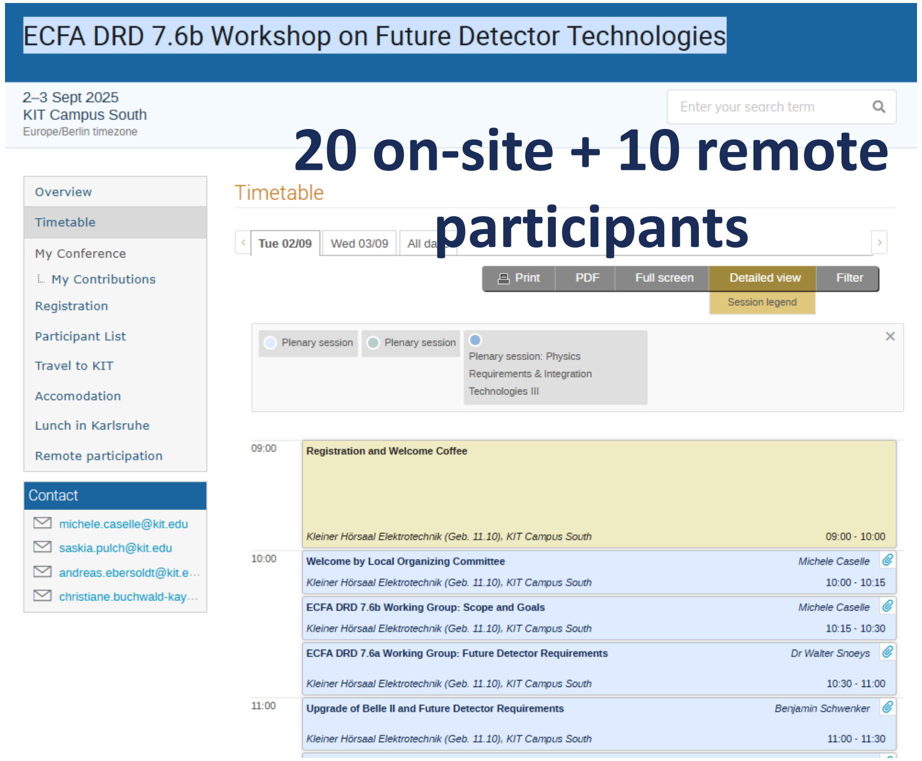
Chiplet Designers	Wafer Layout	Al/RDL (Cu)	Flip Chip	Mechanical/Electrical tests
KIT	KIT, HLL	HLL	Norway	FH-Dortmund
HLL		CNM	KIT	Norway
FH-Dortmund		FBK (?)		FBK for TL

Al/RDL (Cu) → TSVs

TSVs: Development of TSV
KIT, HLL (?), CNM (?)



ECFA DRD 7.6b Workshop on Future Detector Technologies @ KIT



20 on-site + 10 remote participants

Organized into three sessions:

- Future Detectors and Requirements
- Current Status and Emerging Technologies
- Integration Technologies and Future Perspectives (contributors)

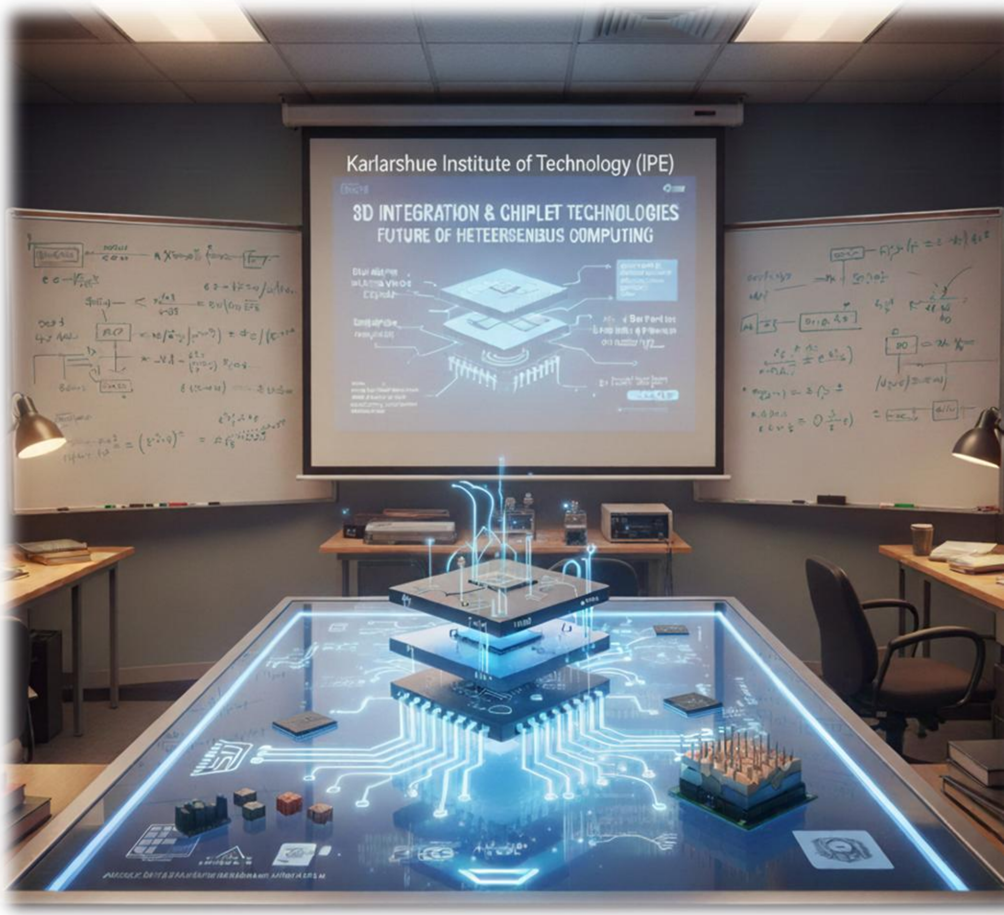
Conclusions

- **Establishing a distributed detector laboratory:** fabrication of the Pilot Project will begin immediately, next step W2W bonding on 8-inch wafer

- The **collaboration** works in **strong synergy**, **sharing infrastructure and expertise** under a **clear** and **unique vision**, with the firm intent to continue working together and ensuring broad community access to this technology

- **Looking ahead:** the next DRD7.6b workshop will take place in Barcelona (Sep/Oct 2026, one week after TWEPP)

- **2.5D chiplet and 3D integration are key enablers** for next-generation detector modules, will be a highly specialized disciplines, like ASIC design. Fostering expertise in these areas positions **Helmholtz as a strategic leader** in cutting-edge integration technologies for future large-scale experiments



Thank you very much for your attention

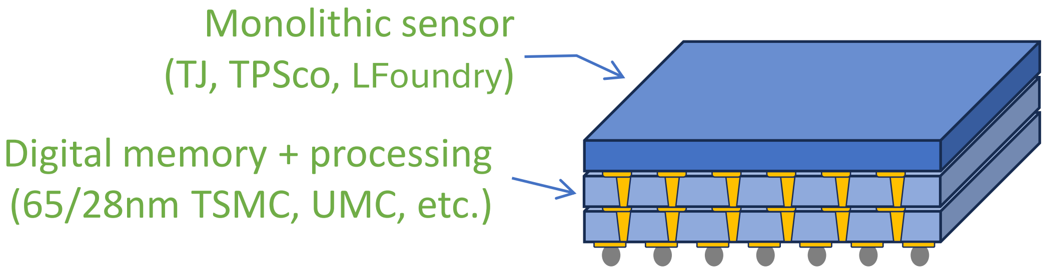
DRD7.6b *ID card*

Project Name	Shared Access to 3D Integration (WP7.6b)
Project Description	Develop advanced chiplet and 3D integration technologies, including the integration of SiPh chips on detector, by in-house infrastructures and third-party vendors
Initial duration	3 years with potential for further prolongation beyond
Innovative/strategic vision	Potential of silicon interposer and chiplet technologies. In-house infrastructure for quick production of prototypes/demonstrators and test vehicles, by employing bump-bonding and detector packaging technologies already available. To establish a concrete connection with the industrial partners
Performance Target	*Shared competences/experiences* and infrastructures/processes. *Build up and maintain the capability* for a quickly transposed to 3D integration. *Keeping a cost-effective access to selected technologies*
Multi-disciplinary, cross-WP content	Strong connection with 7.1 for the integration of SiPh chip and optical fiber on detector module. Strong connection with 7.6a (e.g. 3D integration/chiplets)

DRD7.6b

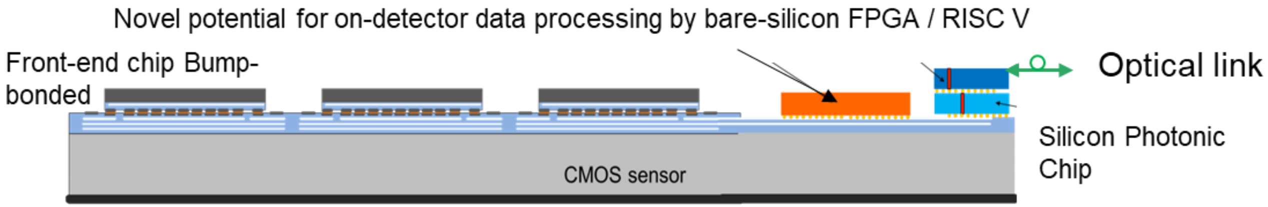
3D-ASIC on a single die

- 3D-ASIC integration on a single die as a low-cost, low-risk demonstrator that paves the way to future large-area 3D-ASIC detector modules assembled via (expensive) wafer-to-wafer (W2W) bonding
    - Risks & mitigation: demonstrator validates partitioning, power distribution, clocking, BER, and thermal, the parts that dominate risk in W2W, before scaling to reticle-stitched, W2W bonding



2.5D passive/active silicon interposer

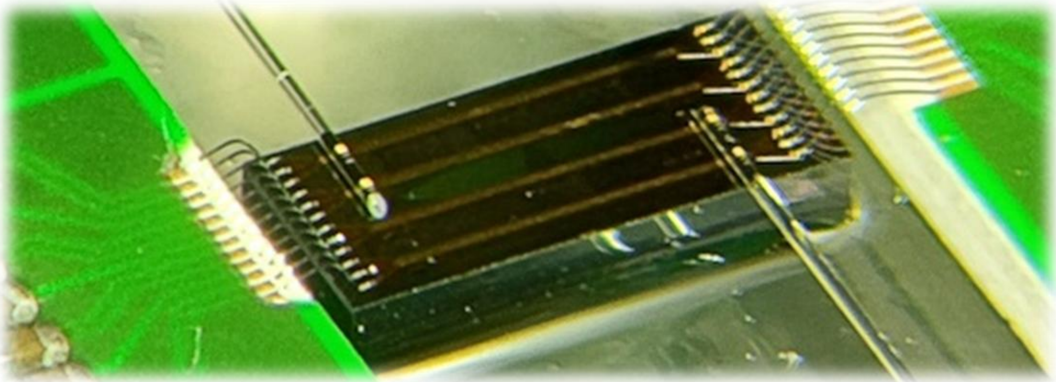
- Silicon interposers are the key enabler to integrate sensors, ASICs, FPGA/AI, and photonics from multiple CMOS nodes into a unified, scalable detector module
    - System-in-package (SiP): interposer becomes the substrate that unifies all domains (sensor, readout, data transmission, on-detector processing)

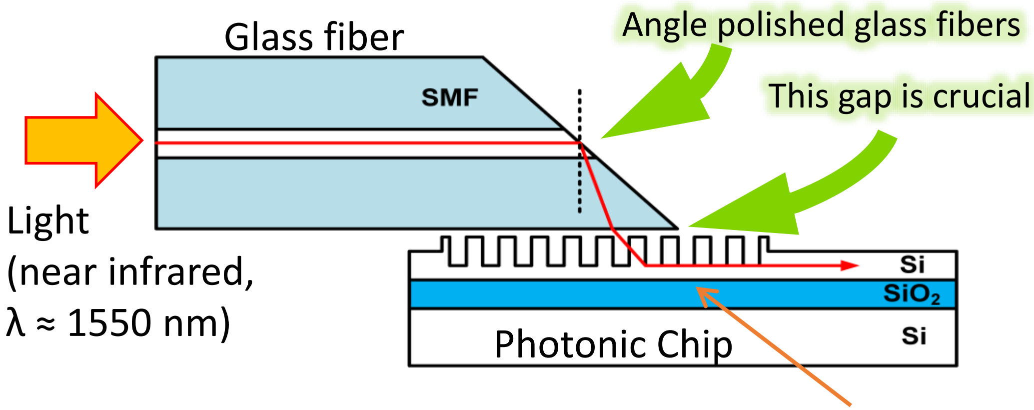


SiPh Packaging & Fiber Attachment

Marcel Stanitzki's presentation: SOPHIE: Silicon Photonic Integrated Electronics for Detector Applications

- SiPh packaging and fiber-attachment, at detector-module or wafer level, are essential for next-generation optical data links. Automated fiber alignment using pick-and-place machines further enhances assembly precision and throughput.
- Coupling geometries (SiPh ↔ fiber)
  - **Edge couplers**: high coupling efficiency, broadband and negligible polarization dependence, but more complex passive alignment (sub-micron lateral tolerance)
  - **Grating couplers**: compatible with wafer-level testing and probing, simple vertical fiber access, but higher insertion loss, higher insertion loss, narrow bandwidth, polarization sensitive

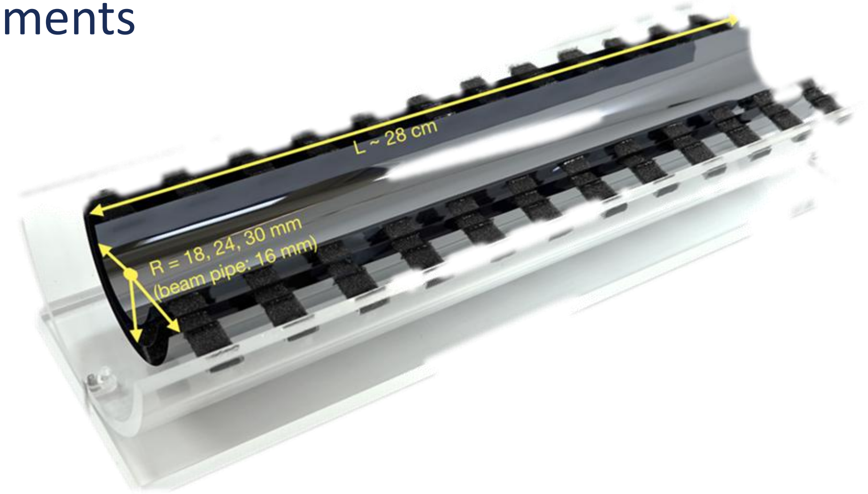




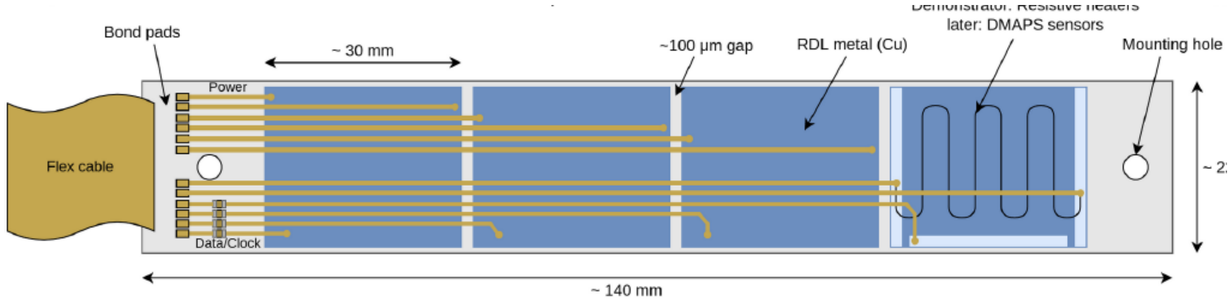
DRD 7.6a <-> DRD 7.6b

Detector packaging technologies for large-area detector modules

- Advanced packaging is vital to achieve ultra-low mass, precise assembly, and robust high-speed power/data links required for large-area detectors in future experiments
  - **From DRD 7.6a**: Fabrication of wafer-level dummy interposer structures, emulating state-of-the-art monolithic pixelated detectors
  - Featuring only the top metal layer, enabling interconnection testing, including of SiPh chip Integration



Large module based on Monolithic active CMOS pixel sensor OBELIX



- All-Silicon Ladder Concept: Single silicon piece with 4 sensors cut from one wafer
- Post-Processing: Addition of redistribution metal layers for data and power

Parallel session:

David Novel "FBK platform for low mass flexible interconnections"

Fabian Huegging "Development of ultra-thin hybrid pixel detectors using wafer-to-wafer bonding"

Pilot Project - Wafer and Chip Design Overview

Square spiral coils chip

Transmission lines

Cross-Collaboration
DRD7.6a ⇆ DRD7.6b

Cross-Collaboration
DRD7.2 ⇆ DRD7.6

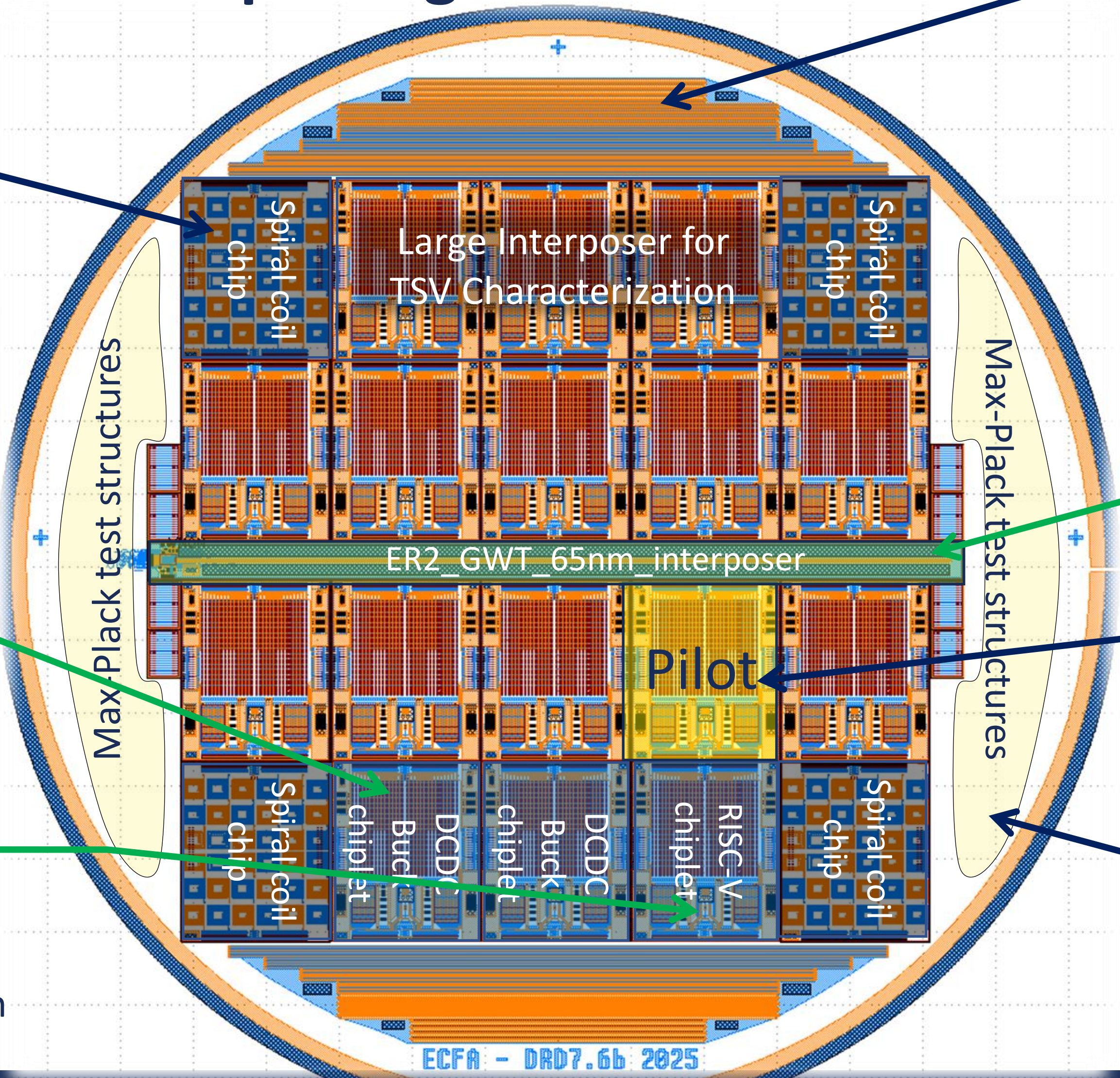
High-Frequency DC-DC Buck Converter interp.

ER2_GWT_PSI 65nm TPSCo interp.

Pilot Project-interposer

RISC-V interposer

Max-Planck tests

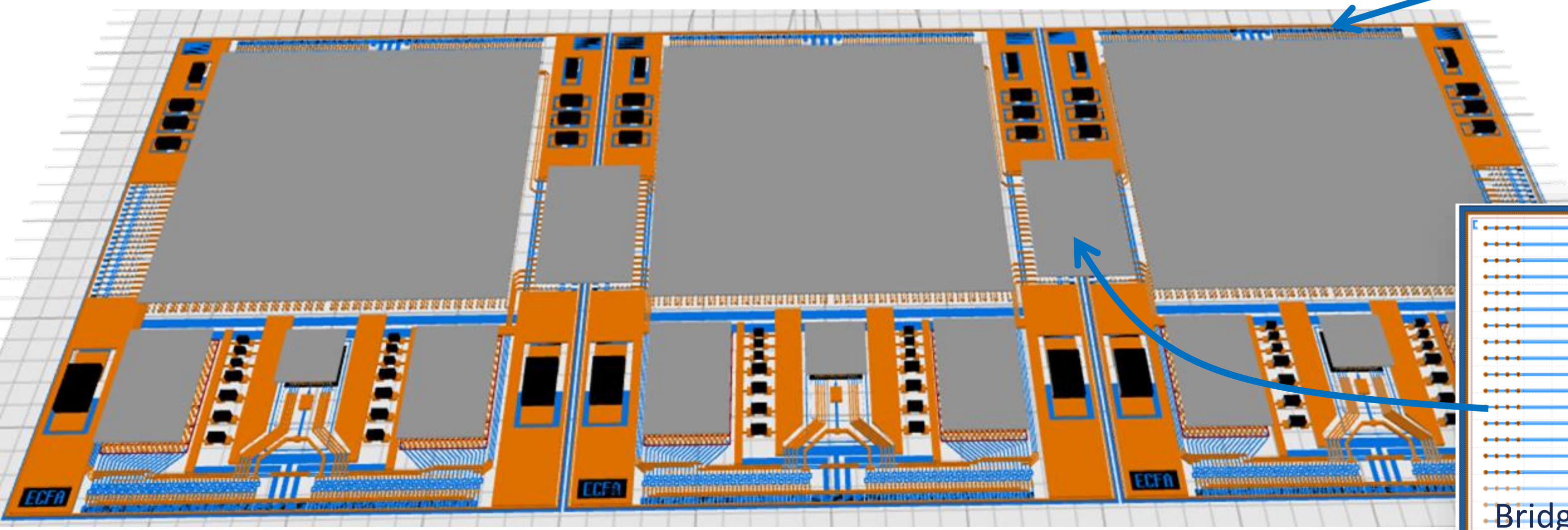


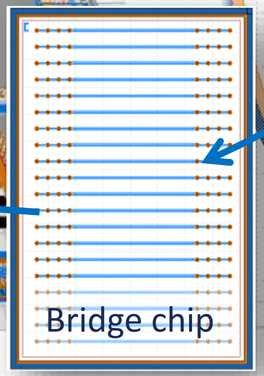
Additional detail → parallel session

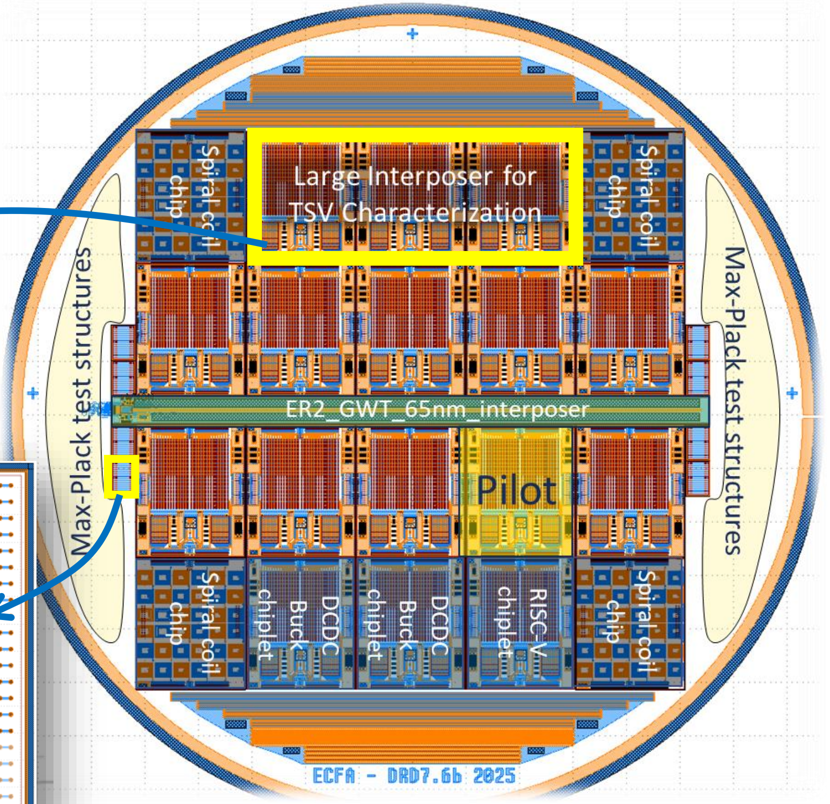
DRD7.6b

Pilot Project – Interposer

- **Modular Design, Large-Area Interposer (up to Wafer Level)**



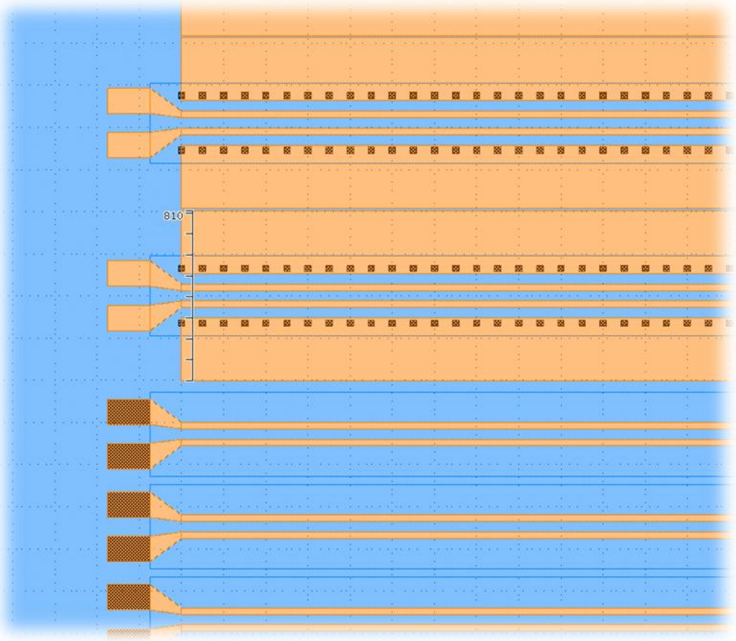


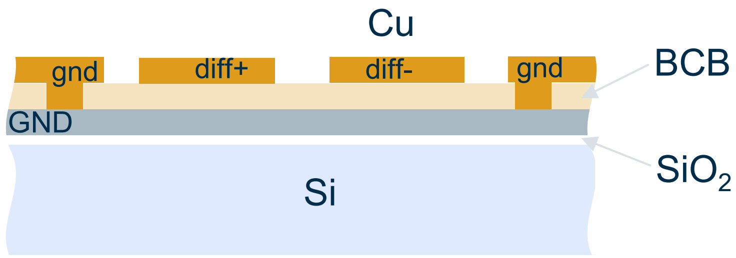


- Scalable architecture enabling interposers from module-size up to full wafer-level implementations
- Designed to support thermal studies of large-area interposers, addressing heat distribution and mechanical stability
- Provides a platform to evaluate the signal integrity across extended dimensions

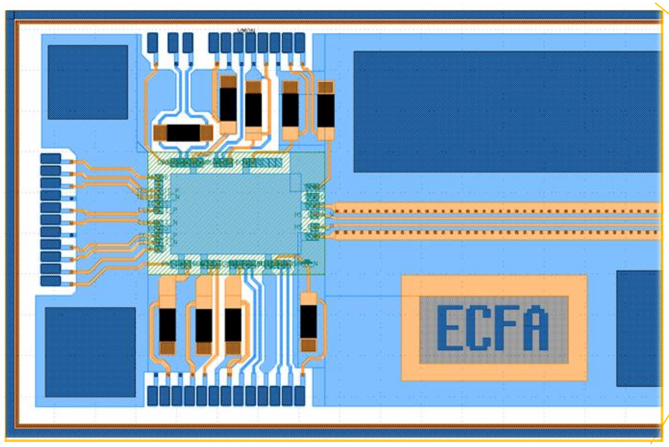
Pilot Project – High-Bandwidth Transmission Line

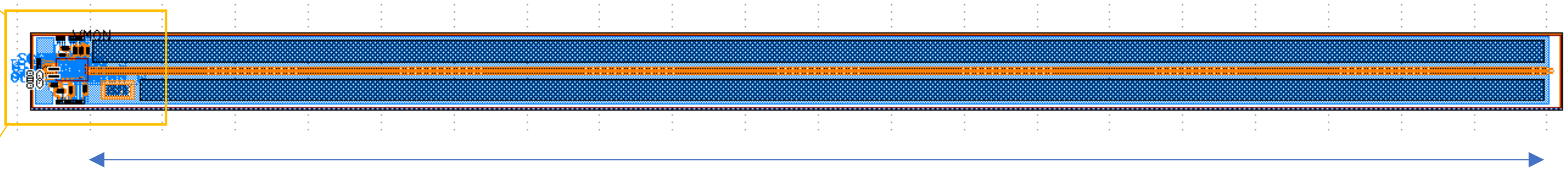
- Transmission lines implemented in Al/SiO_2 and Cu/BCB/Al stacks
- Designed to study and characterize signal propagation at >10 Gb/s
- Different combinations of line width and gap to explore impedance control and loss mechanisms
- Supports extraction of S-parameters, insertion loss, return loss, and crosstalk
- Provides test vehicles for validating electromagnetic simulations against measurements
- Includes structures for evaluating manufacturing tolerances and repeatability





Cross-Working Group Contributions – DRD7.6a ⇆ DRD7.6b

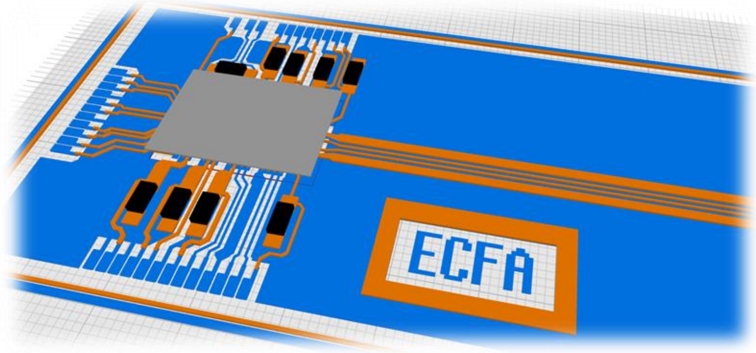


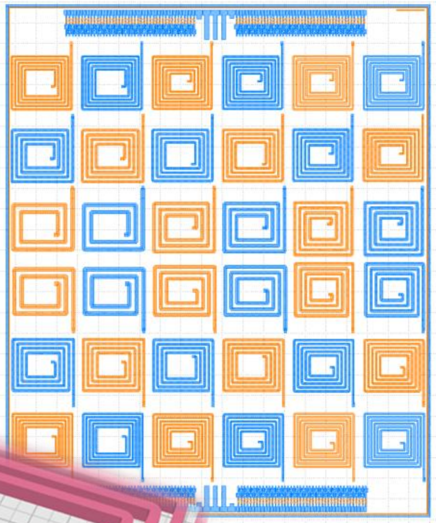


TL 10 cm

ER2_GWT_PSI chip
(Bump-bonded)

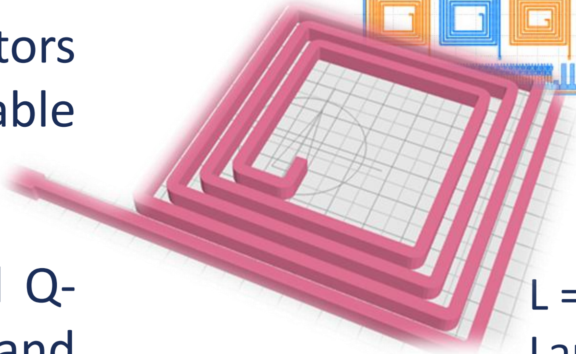
- **Design Objective:**
  - ER2_GWT_PSI chiplet designed for standalone testing of the 10.24 Gb/s GWT-PSI serializer embedded in the MOSAIX stitched sensor ASIC
- **Key Features:**
  - Integrated transmission lines for high-speed signal validation
  - Serves as test vehicle for high-speed data link via RDL
  - Provides a test bench for the new transceiver developed in 65 nm TPSCo
  - Realistic measurement of parasitic and channel losses, signal integrity, dispersion, attenuation



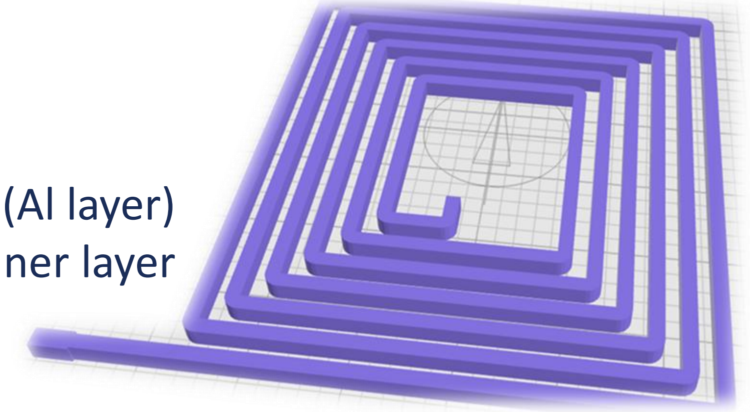


Pilot Project – Design Spiral Inductors chiplet

- **Role of inductors**: beyond DC-DC converters, they are indispensable also for impedance matching
- **Dedicated test chip development**: dense array of Al/Cu spiral inductors (20–100 nH) designed to cover a broad operating range and enable systematic evaluation
- **High-value measurements**: accurate extraction of inductance and Q-factor, considering the impact of parasitic resistance (R) and capacitance (C), essential to assess real performance vs. simulation
- **Strategic outcomes**: improved compact models of passive components, optimized power management blocks, and robust mixed-signal/high-frequency designs



L = 40nH (Cu layer)
Large inner layer



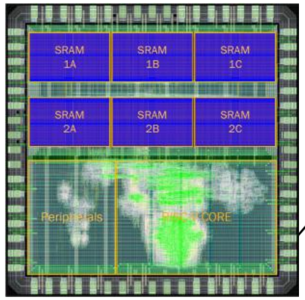
L = 100nH (Al layer)
Large inner layer

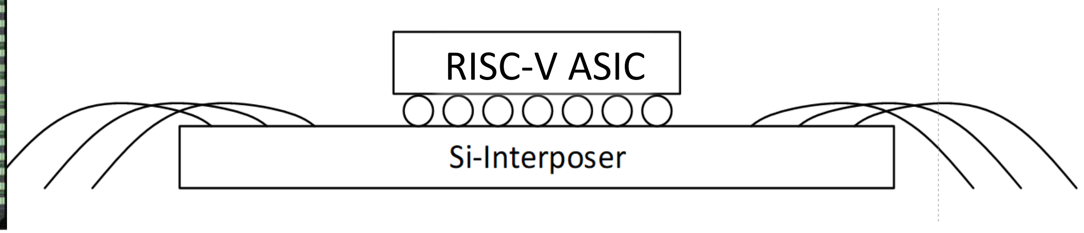
Cross-Working Group Contributions – DRD7.2 ⇆ DRD7.6

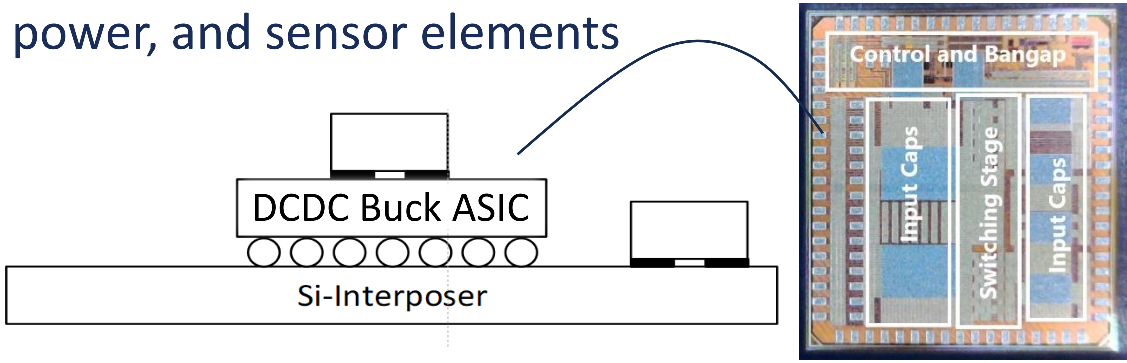
- **Collaborative Development:**
  - Joint effort between DRD7.2 and DRD7.6 to advance interposer-based integration technologies
- **Key Demonstrators:**
  - RISC-V Microcontroller Processor + SMD: Implemented on an interposer platform
  - High-Frequency DC-DC Buck Converter: Showcasing power management integration
- **Interposer Features:**
  - Integrated passive components for compact functionality
  - Bond pads for modular chiplet integration and external connectivity
- Path towards scalable heterogeneous integration of logic, power, and sensor elements

→ Michael Karagounis’s *talk*

→ *Levi Mariën’s talk*





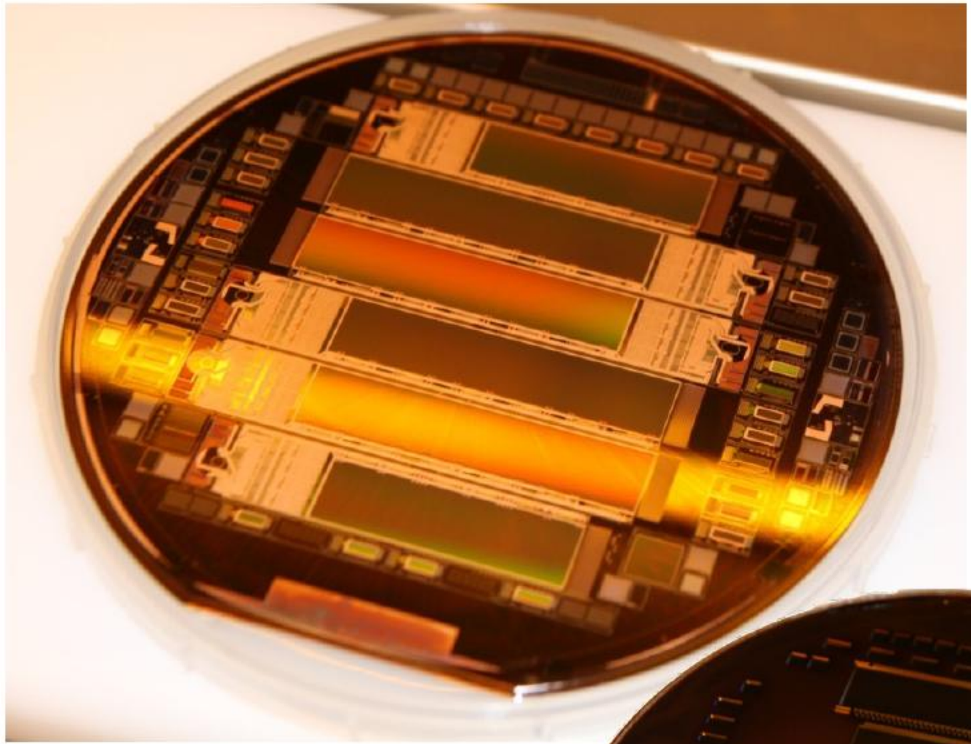


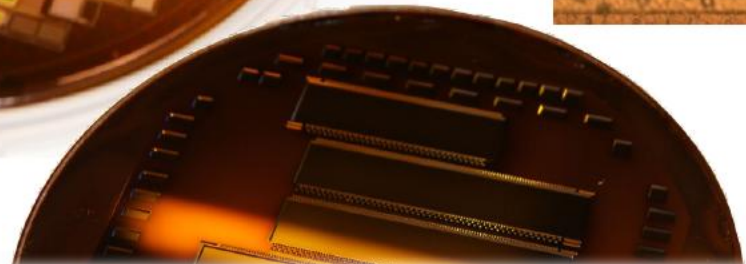
MAX PLANCK
SEMICONDUCTOR
LABORATORY

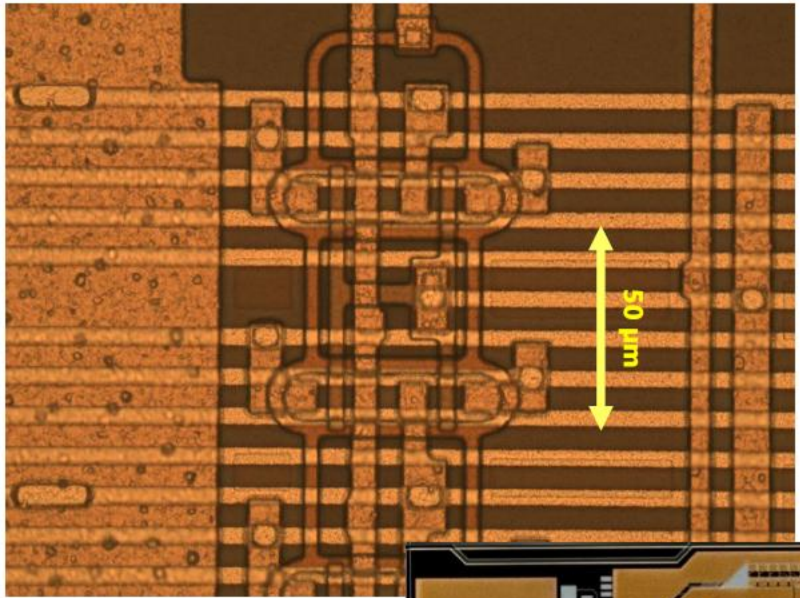
SEMICONDUCTOR LABORATORY
OF THE MAX PLANCK SOCIETY

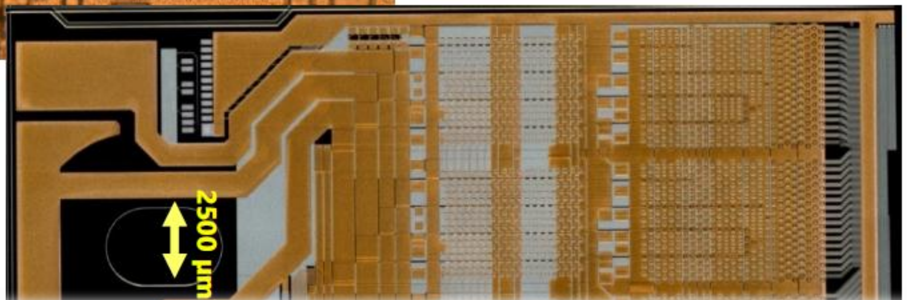
Courtesy: Ladislav Andricek

Module design on wafer level









Ti:W/Cu RDL on wafer level

- The RDL process already developed forBelle PXD can be quickly transferred to the pilot project
- A maskless aligner in operation enables fast and flexible photolithography without the need for physical masks

The way forward: **Wafer bonding**

- Very versatile basic process step for (heterogenous) integration
  - ↳ Wafer-to-wafer or collective chip-to-wafer bonding
    - ↳ Si to Si, Si to other materials like compound semiconductors, e.g.
    - ↳ "Hybrid bonding": embedded Cu-Cu bonds for electrical interconnections

Plasma activation: EVG810

Cleaning/prep: EVG301

Direct and adhesive (temporary) bonding: EVG501
↳ SOI, C-SOI

Hybrid Bonding: EVG Smart-View
↳ Aligned W2W bond

- Wafer preparation
  - ↳ "Bosch" Process for C-SOI
  - ↳ Post-processing: RDL on ASIC and sensor wafer
  - ↳ CMP
  - ↳ Re-constitution of Wafer from KGDs

▷ **all tools ordered, infrastructure in prep, installation expected Feb. 2026**

Institute of Microelectronics of Barcelona (IMB-CNM, CSIC)

Integration Technologies at IMB-CNM and Future Perspectives

Miguel Ullán

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Centro Nacional de Microelectrónica IMB

EXCELENCIA MARÍA DE MAEZTU

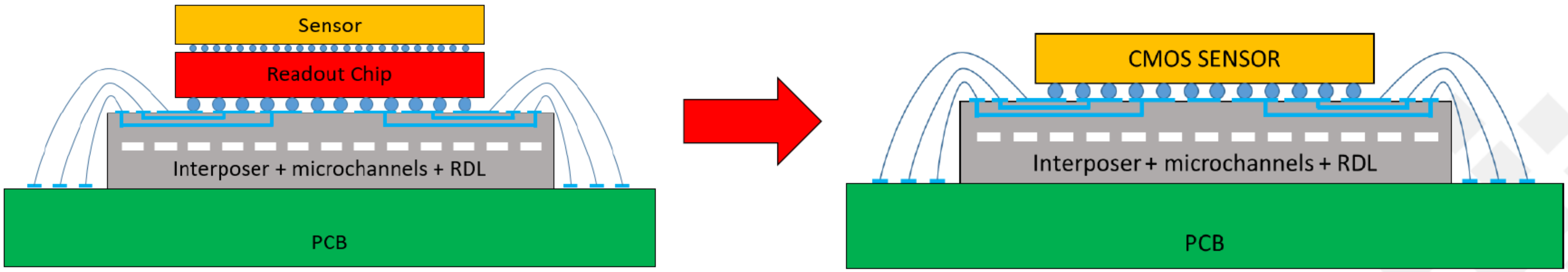
CSIC Consejo Superior de Investigaciones Científicas

MICRO nano FABS Red Española de Salas Blancas de Micro y Nano Fabricación

www.imb-cnm.csic.es

Heterogeneous integration

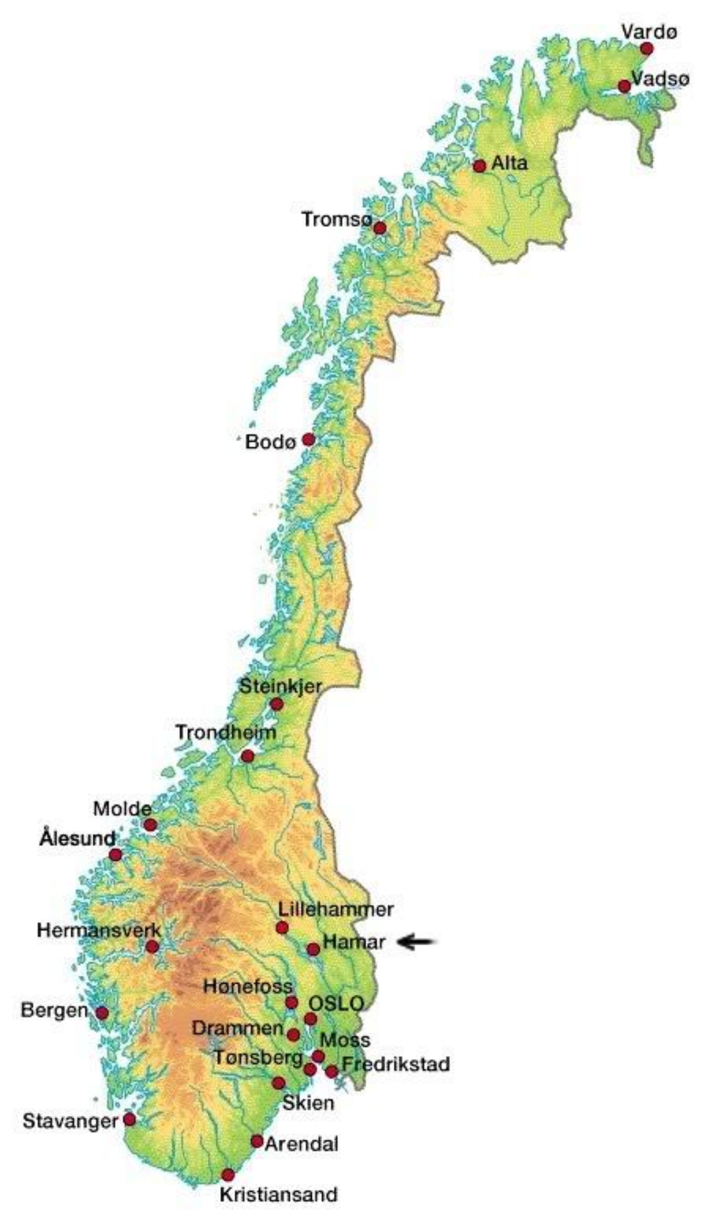
- Microchannels embedded in functional silicon interposers with integrated signal and power routing
  - Combining the cooling capabilities with the electrical connection of the CMOS detector
    - For signal and power routing → Redistribution Layer (RDL)



Assembly & Integration Technologies for Microelectronics & Microsystems

Expertise & Future Prospect - Norway

Hoang-Vu Nguyen, PhD
Associate Professor at Department of Microsystems
University of South-Eastern Norway

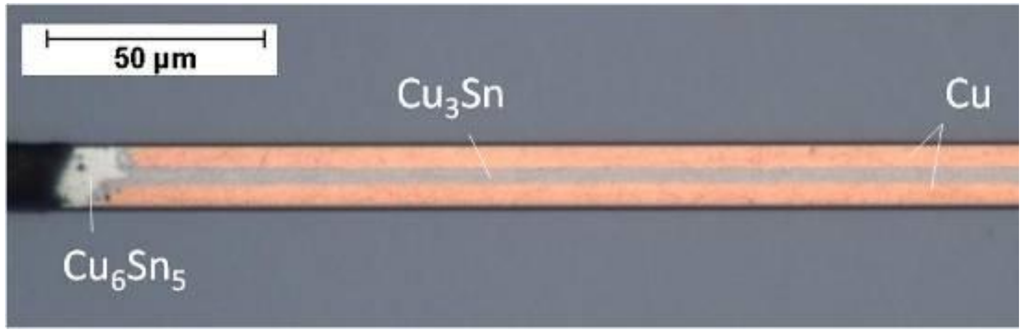


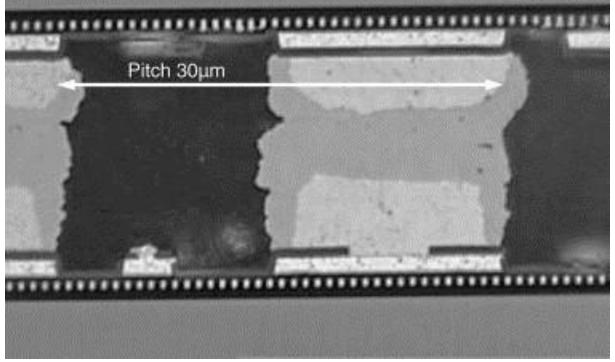
Development of advanced bonding technique
Solid-Liquid InterDiffusion (SLID / TLP) - Motivation

- Original motivation: High-temperature stability
  - High-Temperature applications
  - High Temperature during manufacturing
  - Resists repeated processing temperature
    - Eliminates need of solder thermal budget

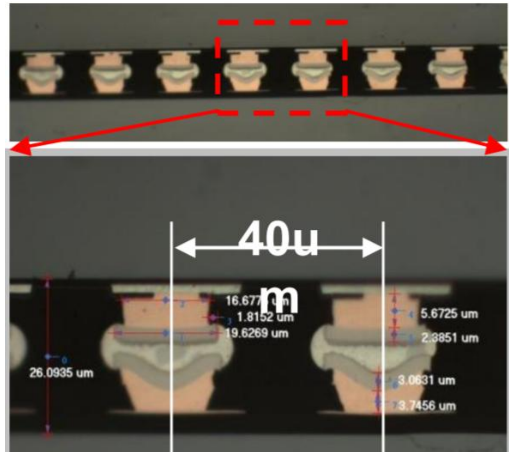
- Well-defined, thin metallic interconnects
  - Bondline thickness ~10 µm

- Fine pitch possible
  - 30 µm pitch demonstrated already in 2006
  - Similar to “Cu pillar” technology





H. Hübner *et al*, Microelectronic Eng. **83** (2006), p. 215



Source: ASE Group

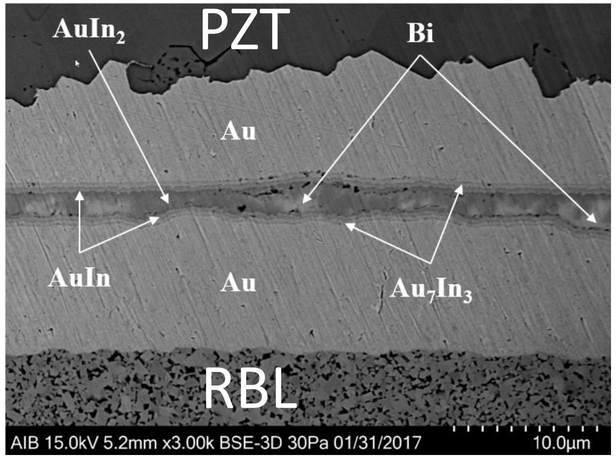
"Low-temperature" SLID bonding
Our focus in coming years

- Temperature-sensitive materials:
  - Piezoelectric materials (poled)
    - Not to approach T_c (Curie temperature)
    - T_c ~150 °C for PZT (ultrasound transducers, actuators, etc.)
  - Ferromagnetic materials
  - Polymers

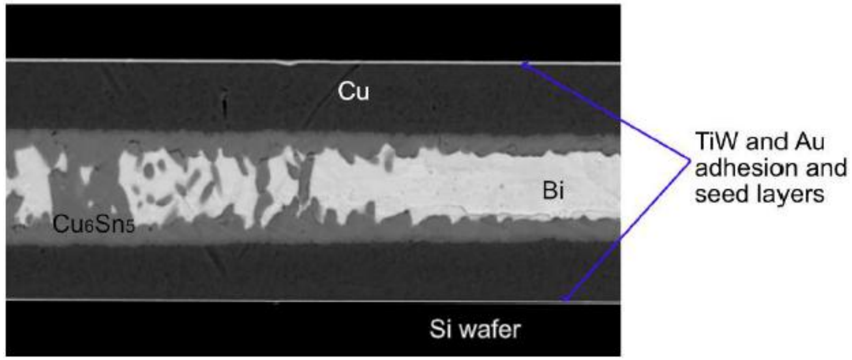
- Need for low-temperature bonding

- Low-temperature solders
  - In: T_m = 156 °C
  - In–Bi : T_m = 72.7 °C
  - Allows only low to moderate application temperatures (must be significantly lower than T_m)

- Low-temperature SLID bonding
  - Bonding is not limiting factor for application temperature



Au-(In-Bi) SLID bond for stacking ultrasound transducer



Cu-(Sn-Bi) SLID bond for Si on Si

FBK platform for low mass flexible interconnections

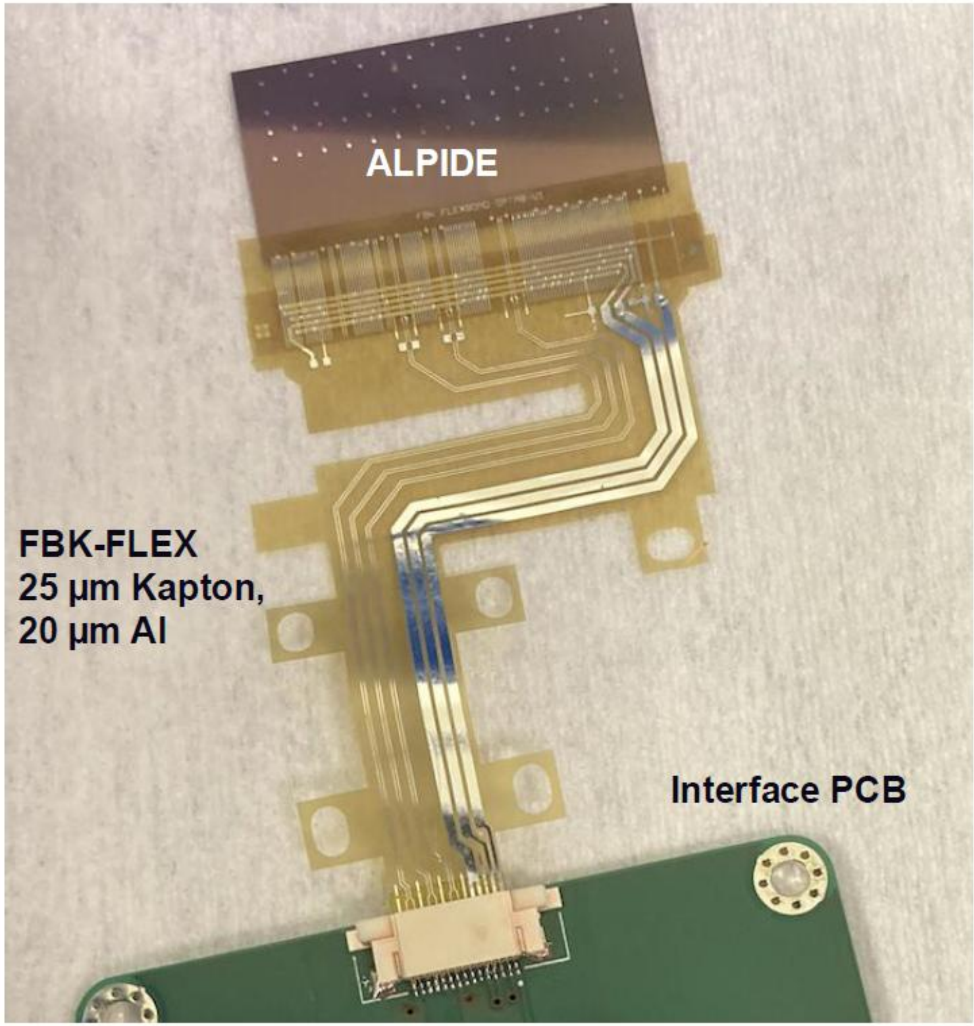
22/09/2025
ECFA DRD 7.6b

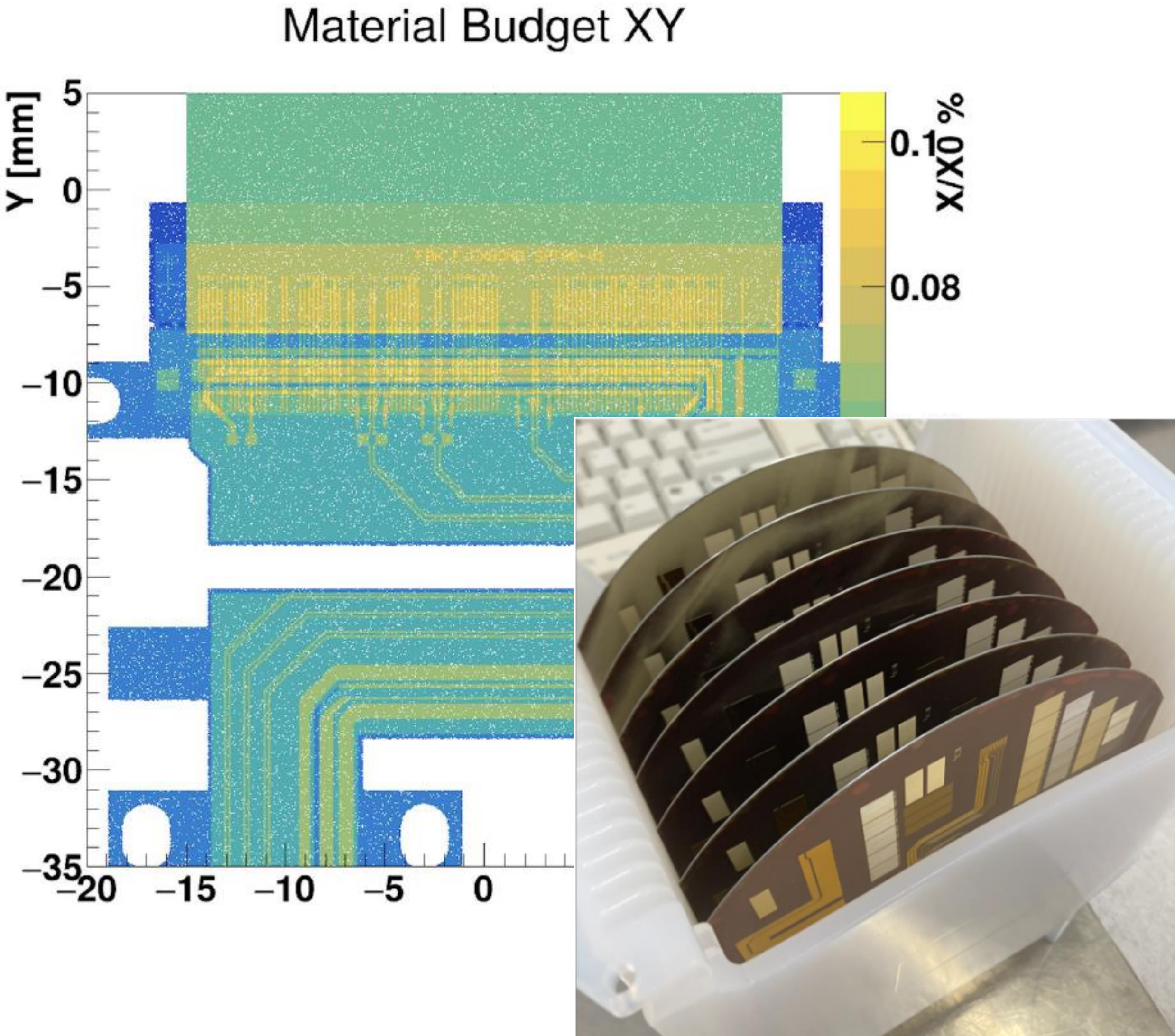
David Novel, Alessandro Lega, Maurizio Boscardin
novel@fbk.eu alega@fbk.eu boscardi@fbk.eu

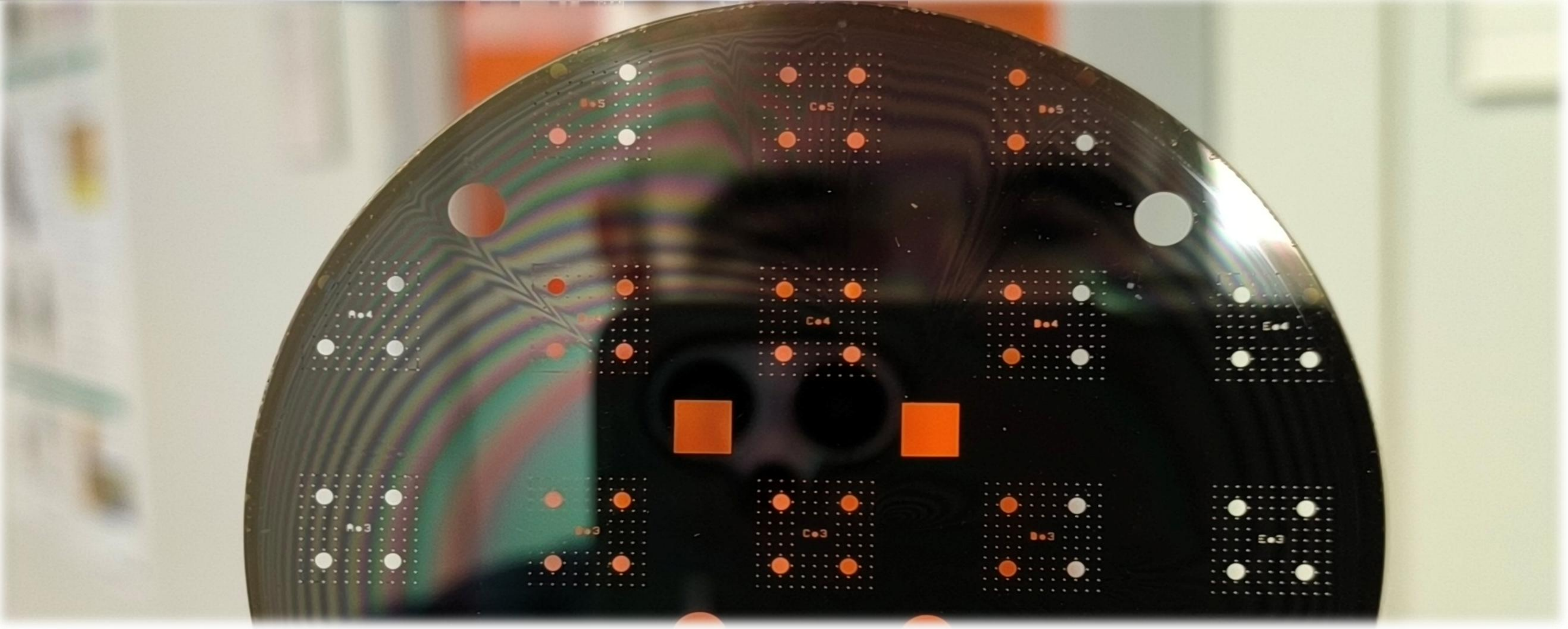
with the contribution of several colleagues of the Sensor and Devices Center

Low mass Aluminium Flex Platform
Final PCB and Material Budget

Courtesy: Mathias Wegner







TSVs formation (machine and infrastructures)

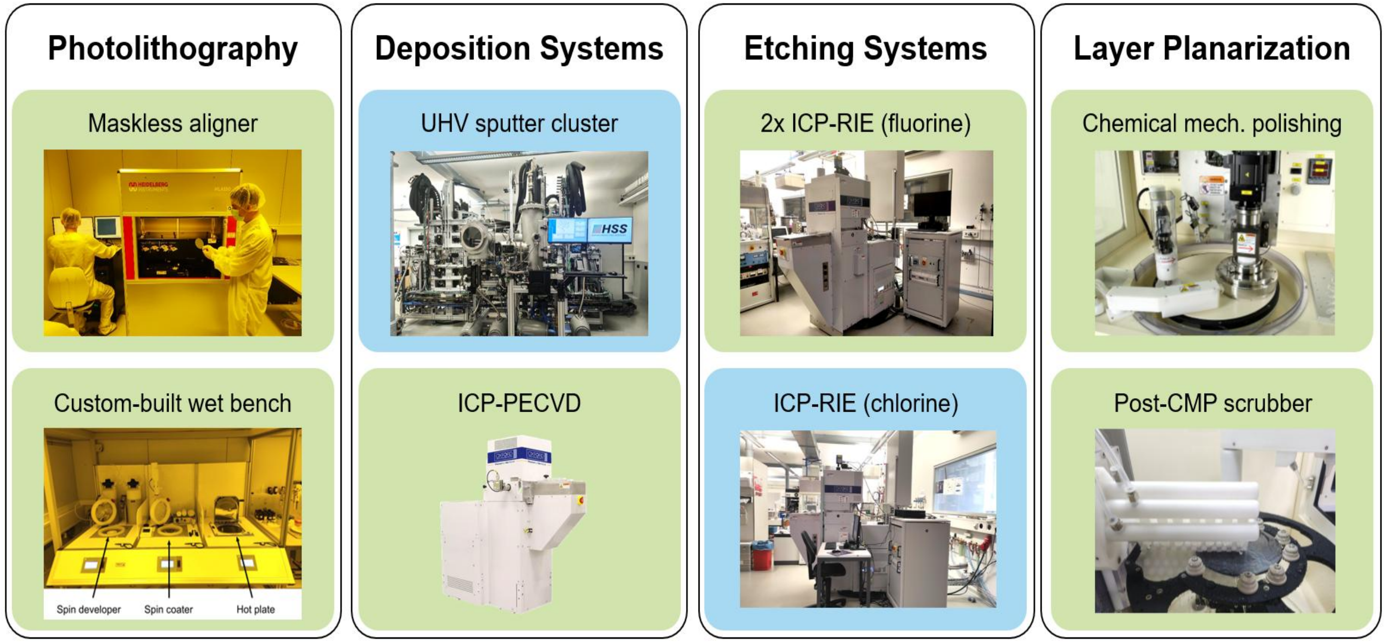
Key enablers for next-generation chiplet and 3D-ASIC technologies

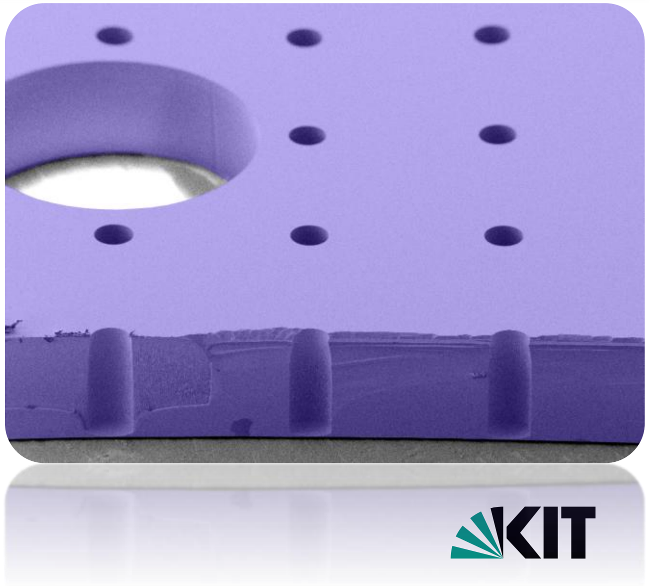
TSV formation by DRIE
Current status & results

Courtesy: Mathias Wegner

Main HSS machinery @ IMS

operation Delivered



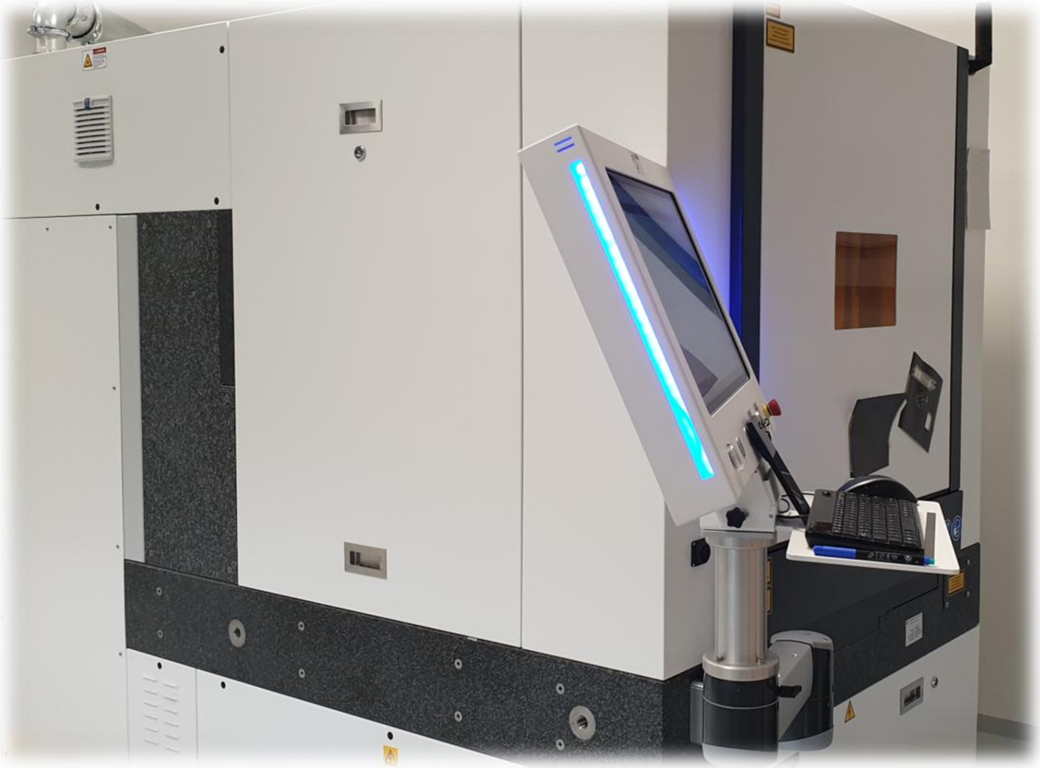


- All key equipment for TSV formation is installed and operational, including the MLA150 (Maskless Aligner), photoresist-based process flow, and the Oxford system using the Bosch profile. The target is to achieve small-size TSVs *O (10 µm)* thin substrates. High-density interconnections will be a major focus of investigation

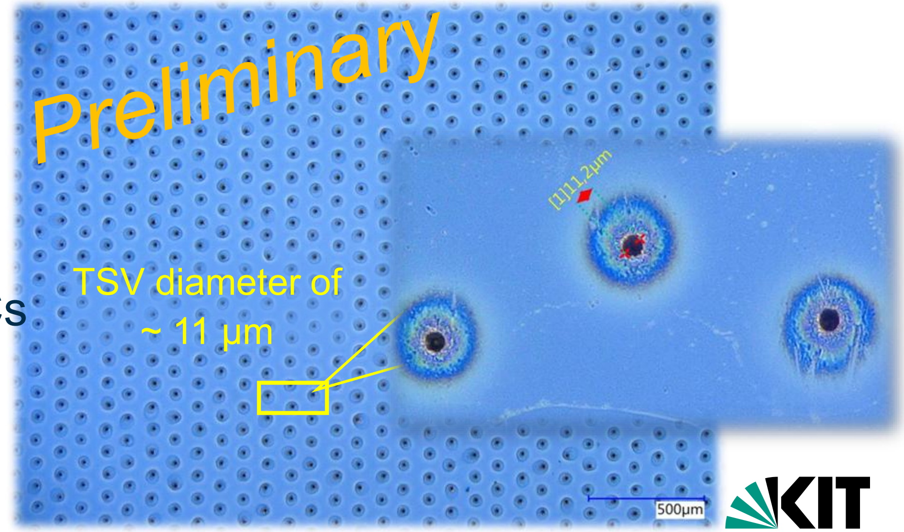
TSV formation by laser drilled
Maskless process for wafer and single die

Courtesy: Felix Steiner and Thoms Blank

Laser machine DR2000 from Photonic System



- Laser spot diameter: 20 µm with a large working area (610 × 520 mm²)
- Fully installed and operational
- Enables precise Through-Silicon Via (TSV) hole formation on single-chip level. Supports wafer dicing for edgeless sensor technologies



- Laser-drilled TSVs can be employed in interposer substrates or ASICs with large tolerance between the TSV region and active structures.

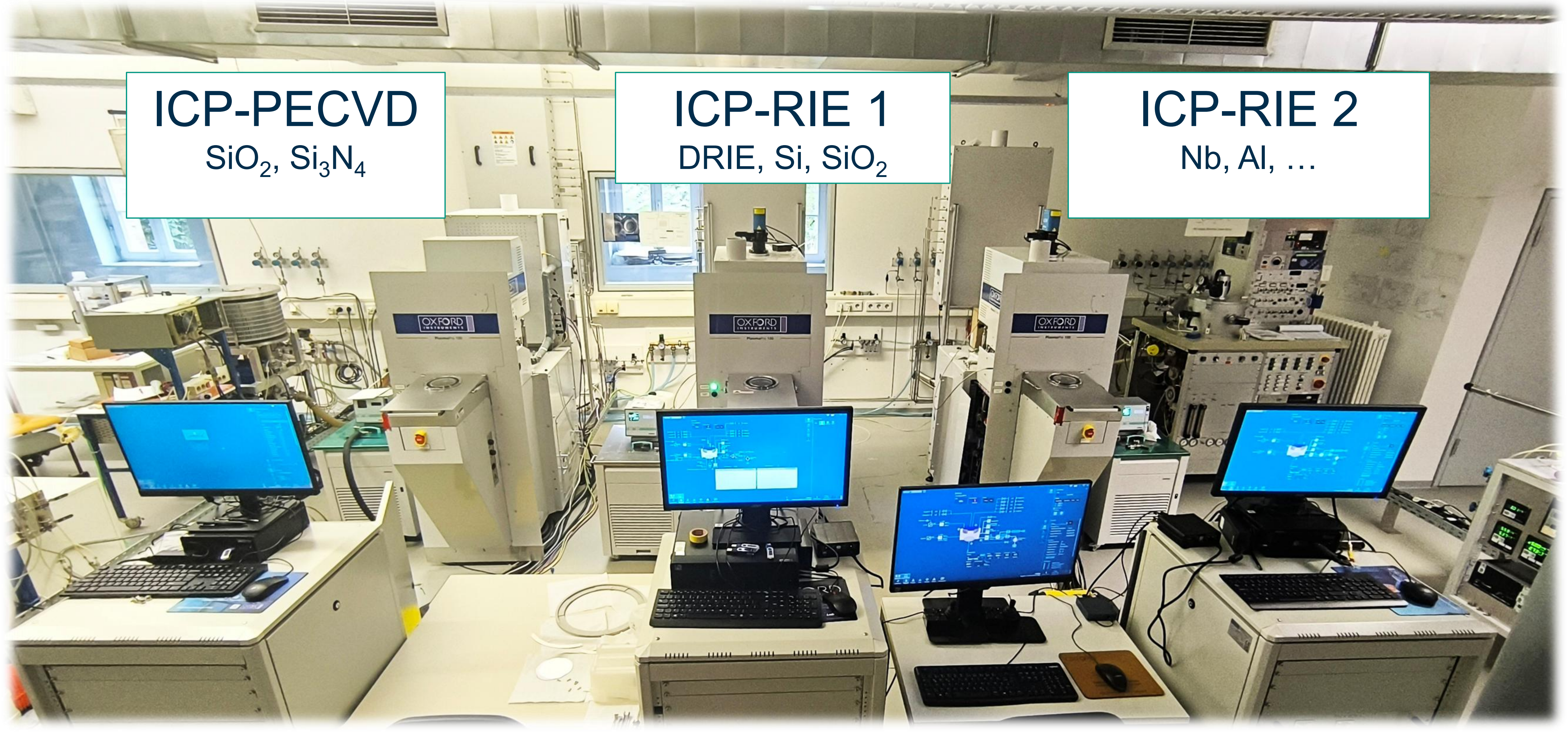
Process capabilities (*near future*)

- Electroless immersion: 4” and 6” wafers
- Dedicated electroless plating stations, each optimized for a specific metal
  - Metals: Zn, Pd, Ni, Au, Cu, Sn (exchangeable with Ag)
- Electroplating stations, single and double-side wafer processing
  - Metals: Cu, Au, Ni
- Applications: TSV metallization, Redistribution layers (RDL) on wafers and interposers
- Advanced packaging for next-generation detector modules

TSV formation by DRIE

Three new machines from Oxford Instruments Plasma Technology

Courtesy: Mathias Wegner



Courtesy: Mathias Wegner

Main HSS machinery

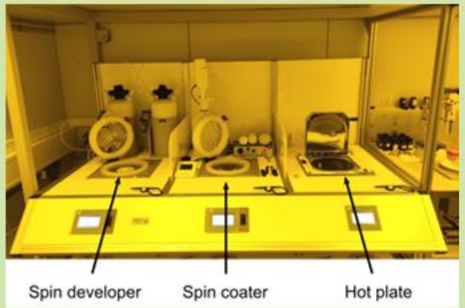
In operation | Delivered

Karlsruhe Institute of Technology

Photolithography

Maskless aligner

Custom-built wet bench



Deposition Systems

UHV sputter cluster

ICP-PECVD

Etching Systems

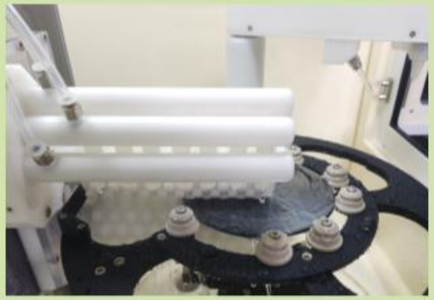
2x ICP-RIE (fluorine)

ICP-RIE (chlorine)

Layer Planarization

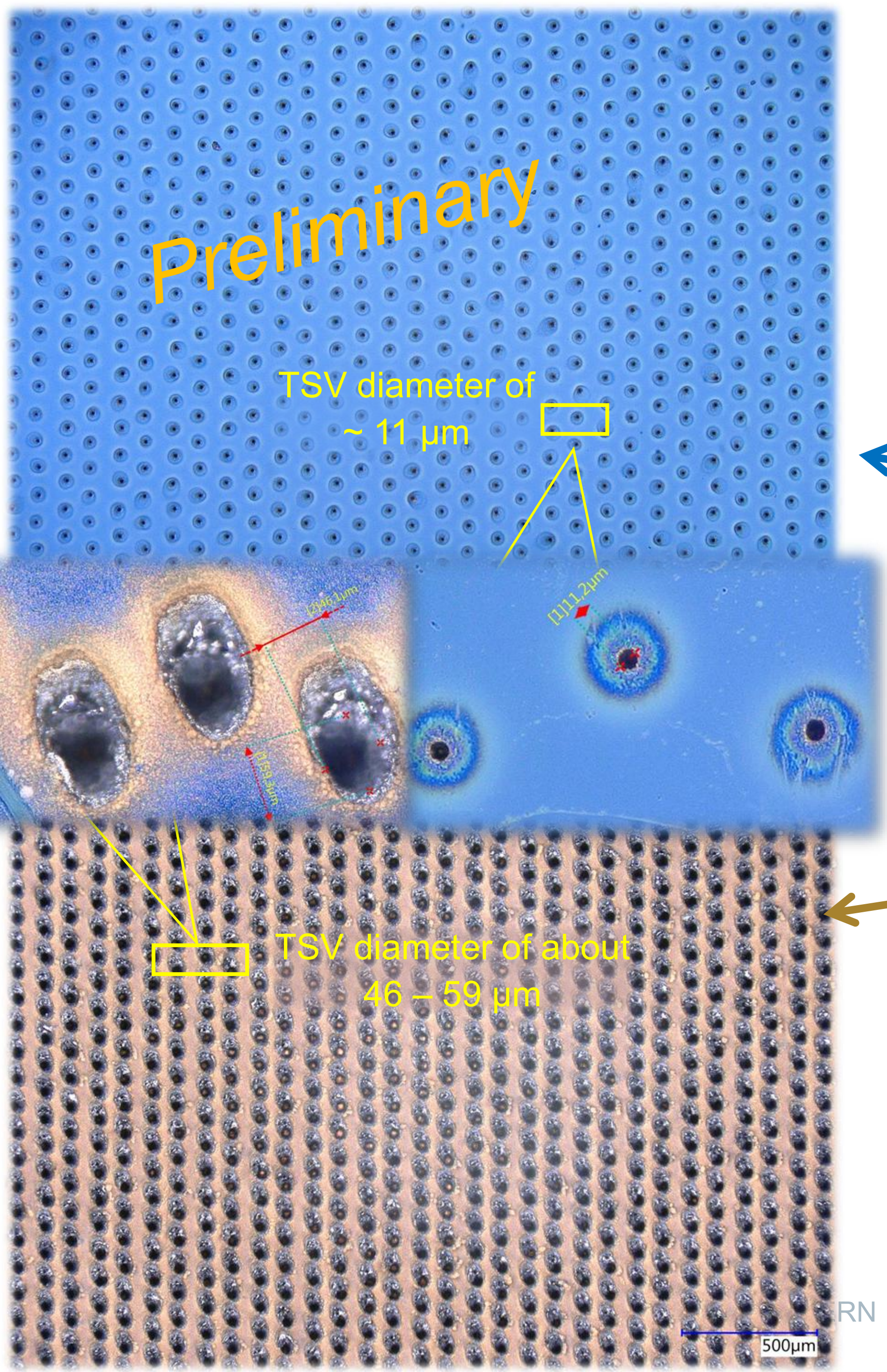
Chemical mech. polishing

Post-CMP scrubber

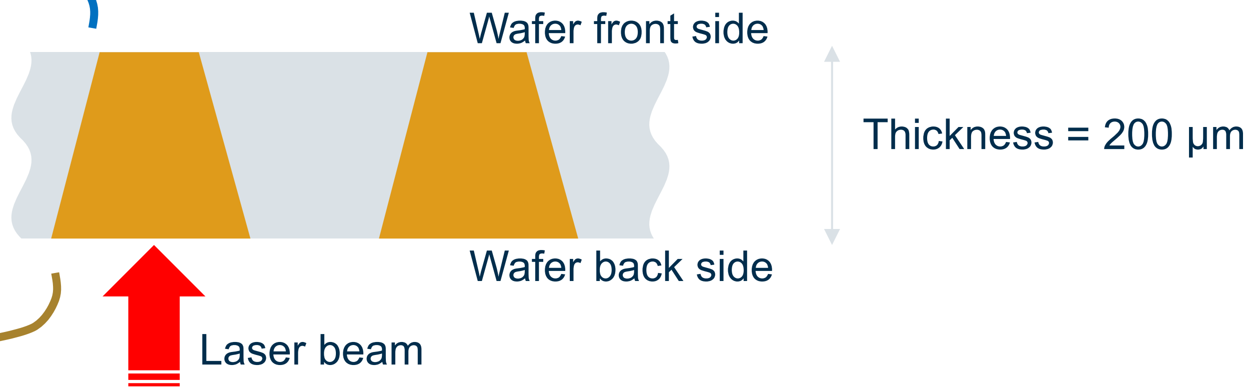


TSV formation by laser
Current status & results

Courtesy: Felix Steiner



- High-density TSVs are possible with laser-drilled formation, combined with outstanding flexibility in via placement since no photolithography process is required



- A burned area around the laser-drilled TSVs is evident, which can be removed by CMP
- Laser-drilled TSVs can be employed in interposer substrates or ASICs with large tolerance between the TSV region and active structures.