

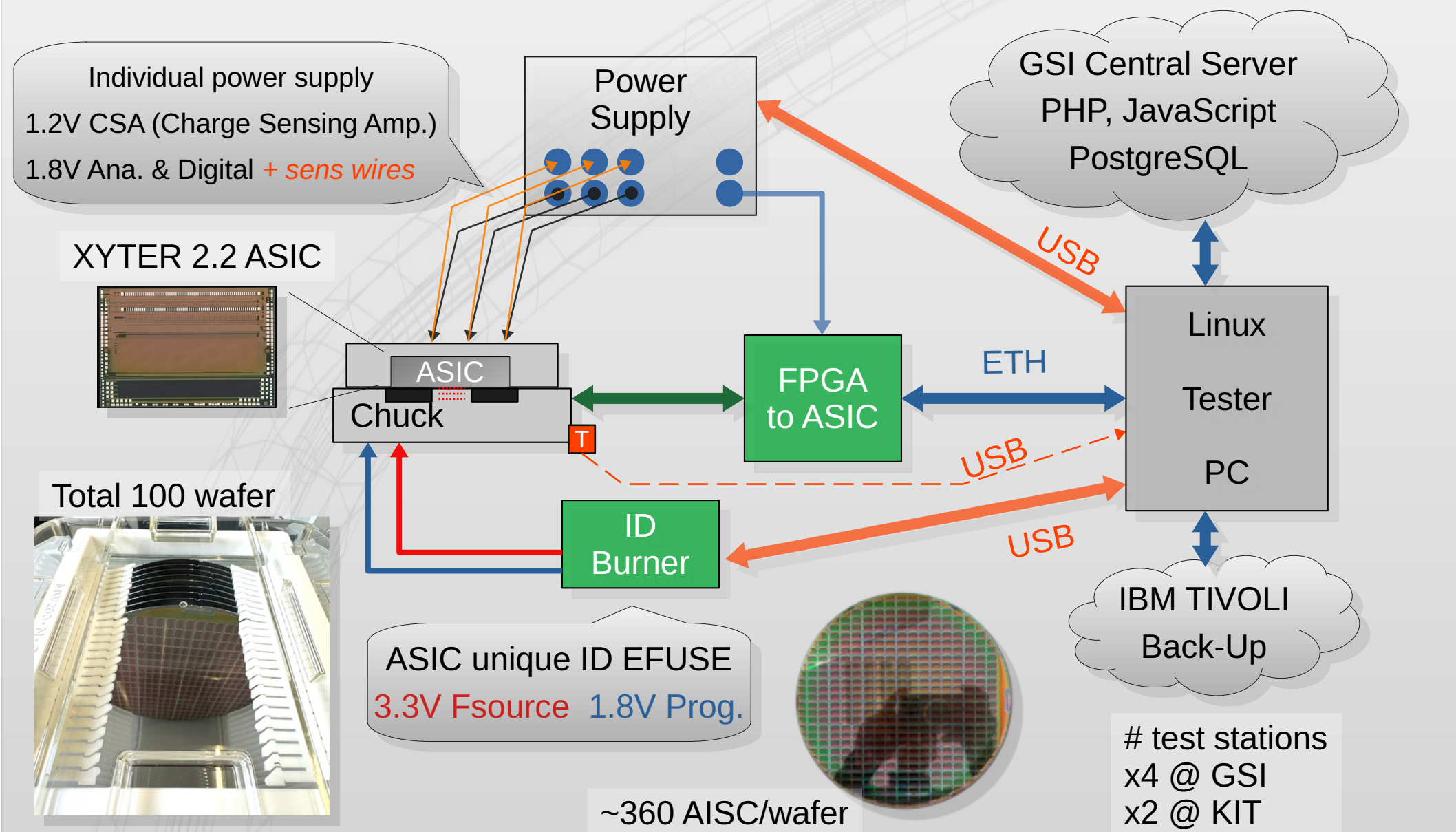


Introduction

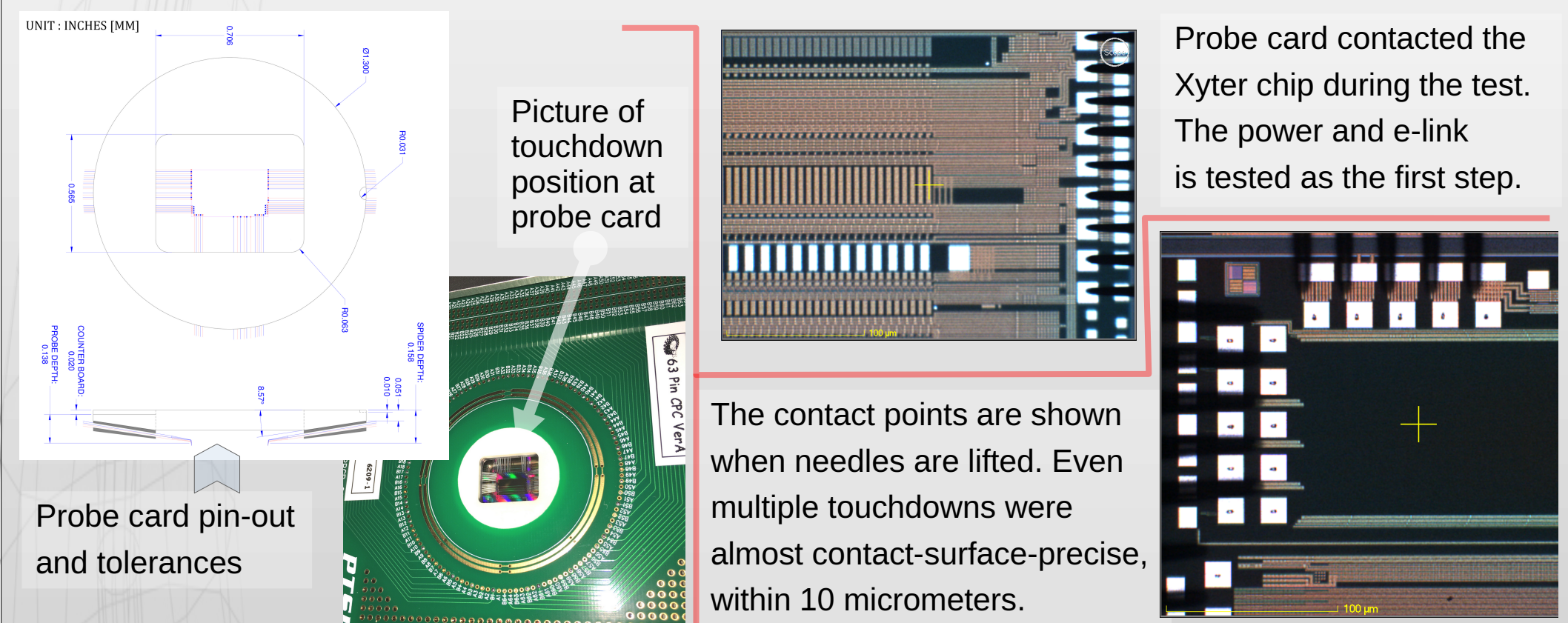


Last year, we developed and successfully utilized a serial test system comprising 80 wafers, each with 360 chips. Each chip was tested individually for various parameters under predefined conditions. The data was analyzed and displayed via a web interface almost immediately after the measurement was finished. The file for laser dicing of each wafer is automatically generated and in an industrial format. In this presentation, the system will be discussed, and a summary will be given.

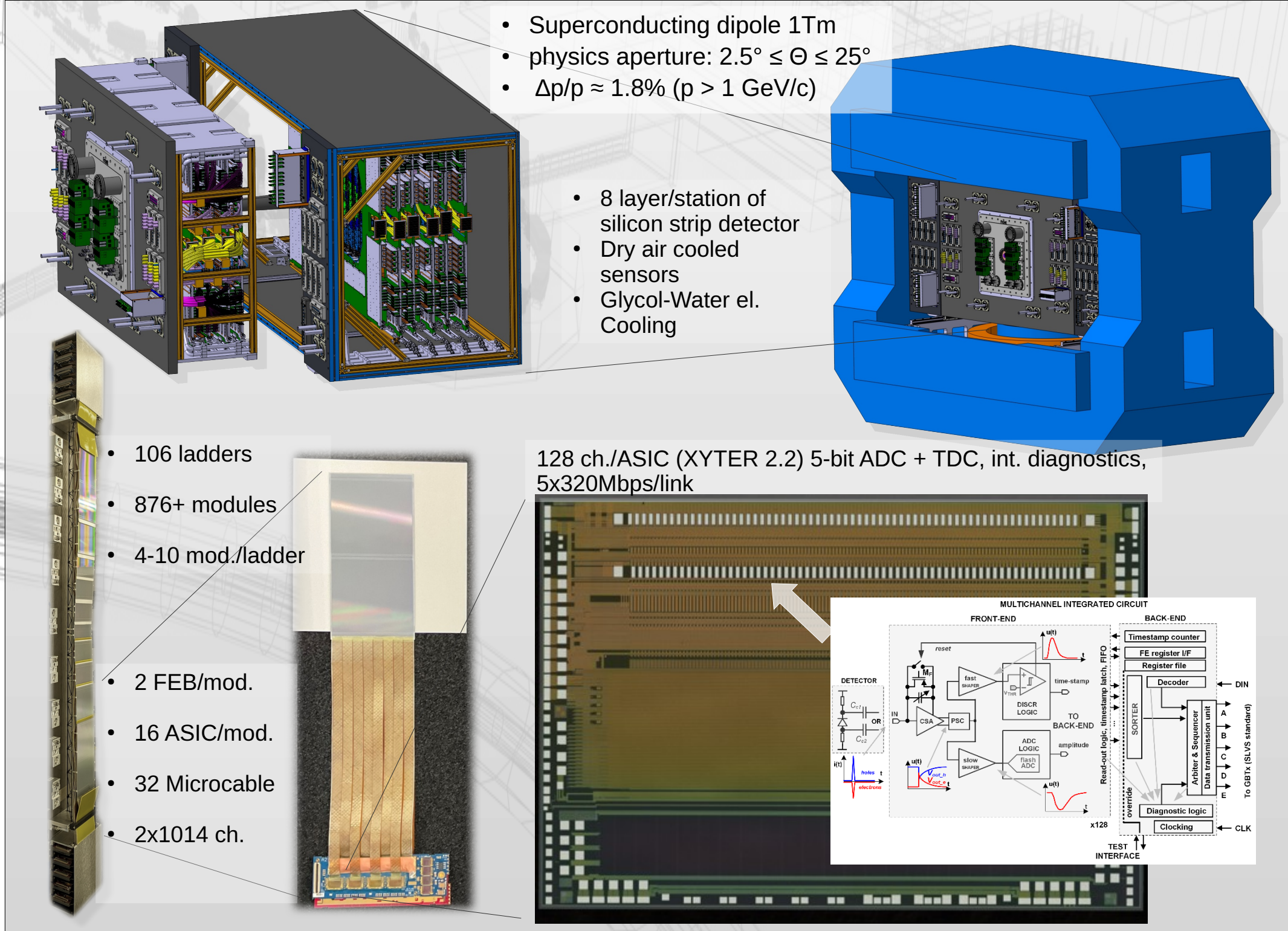
ASIC Test Procedure



Wafer/ASIC Probe Card



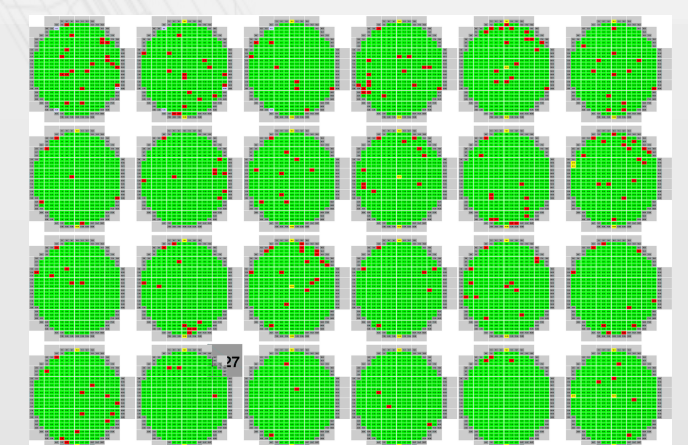
The Silicon Tracking System (STS)



Software Control System for the Wafer Test

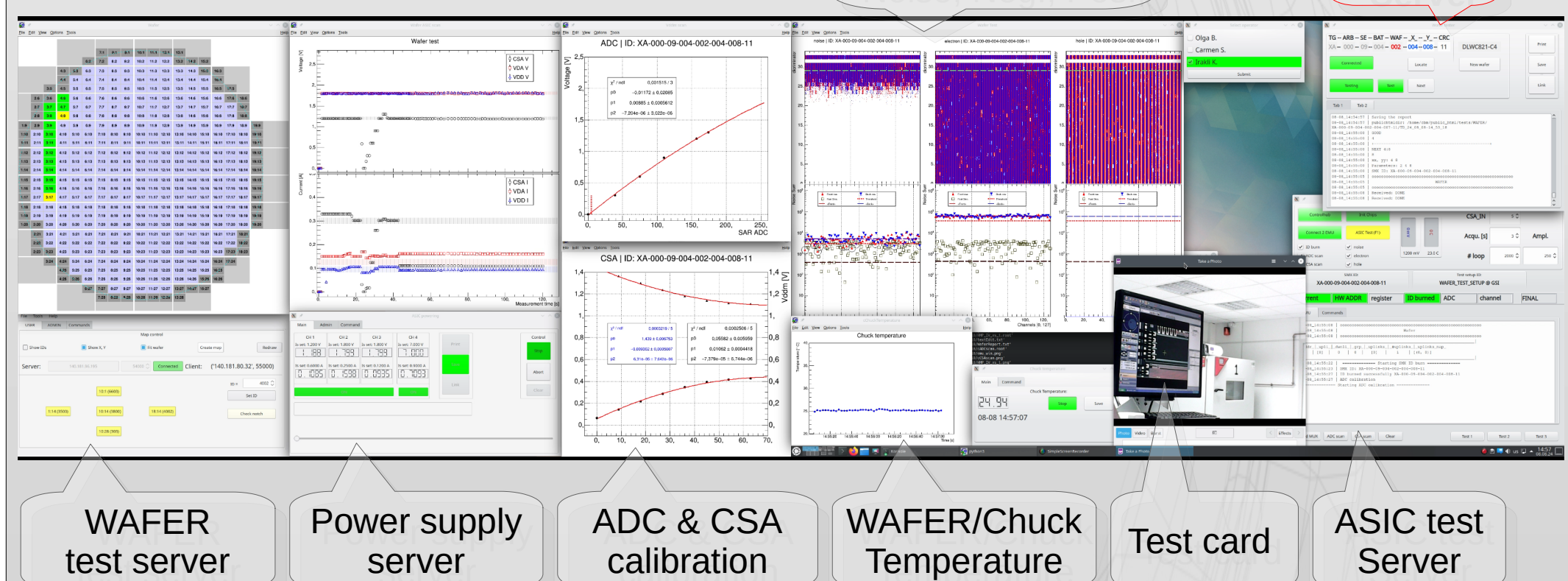
- Custom developed test software
- Adaptive test procedures
- Configurations via YAML and CSV
- Python, PyQT5, PyROOT, Ipbus
- Fully integrated automated system
- *Software more than 10k lines of code*

Random wafer with broken ASIC. The pattern is random for all qualities.



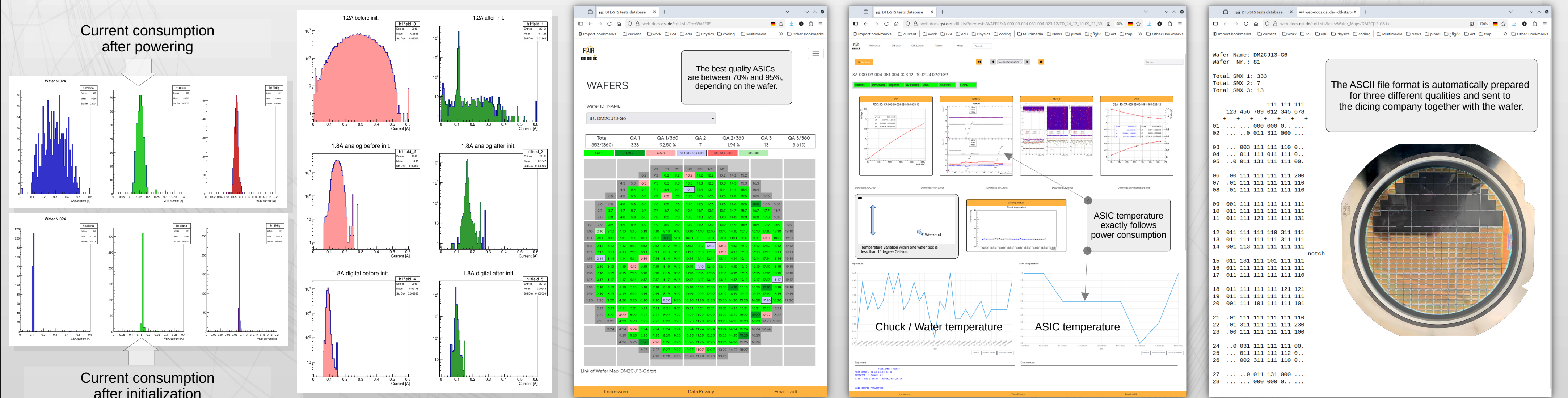
Channel test
Noise, Neg., Pos.,

**MAIN
Server**



Data Base + Web Interface <http://web-docs.gsi.de/~dtl-sts/>

Custom developed front and back-end PHP, Python, and PostgreSQL-based data monitoring system in collaboration with Jagiellonian University, Krakow.
front&back10K lines of code.



Summary

- The ASIC test software was developed during manual testing of the Xyter chips. The ID burning procedure and device were also tested multiple times. All this knowledge has been applied to the wafer test complain plus many more new developments.
- In total, more than 20 wafers were tested manually using a pogo pin socket, and 80 were tested using an automatic probe station. The probe card is custom-made for the Xyter ASIC. It has lasted for all 80 wafers plus a few more test chips during the adjustment process. Contact needles were cleaned after every wafer was tested.
- Overall, it has been a very successful process. We managed to test on average more than one wafer per day. The process is fully automatic, and it has been reduced to a manual exchange of the wafer. The results were online analyzed, and the maps were generated after the test was finished. <https://web-docs.gsi.de/~dtl-sts/?m=WAFERS>