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Serenity-S: A versatile data processing card for CMS Phase-2

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The upcoming high-luminosity upgrade of the Large Hadron Collider (HL-LHC) necessitates the replacement and updating of several sub-detectors within the Compact Muon Solenoid (CMS) experiment. A key challenge of this upgrade is the backend data processing of multiple terabytes of data generated from hundreds of millions of collisions each second. This processing is handled by the L1-Trigger system, which comprises hundreds of state-of-the-art FPGAs connected via high-speed optical links reaching up to 25 Gb/s. For this system we have contributed in the Serenity collaboration to develop Serenity-S, a versatile FPGA processing card based on Advanced Telecommunications Computing Architecture (ATCA) technology fitting the requirements of the backend systems of multiple sub-detectors. The card is designed with a modular philosophy, including a space-optimized service area to provide the ATCA infrastructure, advanced board management features, and a performance-optimized payload area featuring one of the most powerful FPGAs commercially available. This FPGA supports 124 bidirectional high-speed links, enabling data processing rates of up to 3.1 terabits via synchronous or asynchronous clock paths. In total more than 700 of these cards will be produced for multiple CMS systems with emphasis on to the sub-detectors HGCAL (300) and Tracker (216).

Speed talk:

Normal speed talk selection

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