HGCAL SiPM-on-Tile Full-Stack Integration with the Serenity Phase-2 DAQ Hardware

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11th Annual MT Meeting
GSI, Darmstadt

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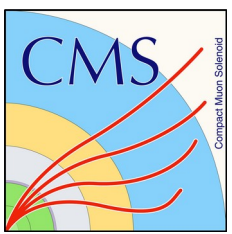
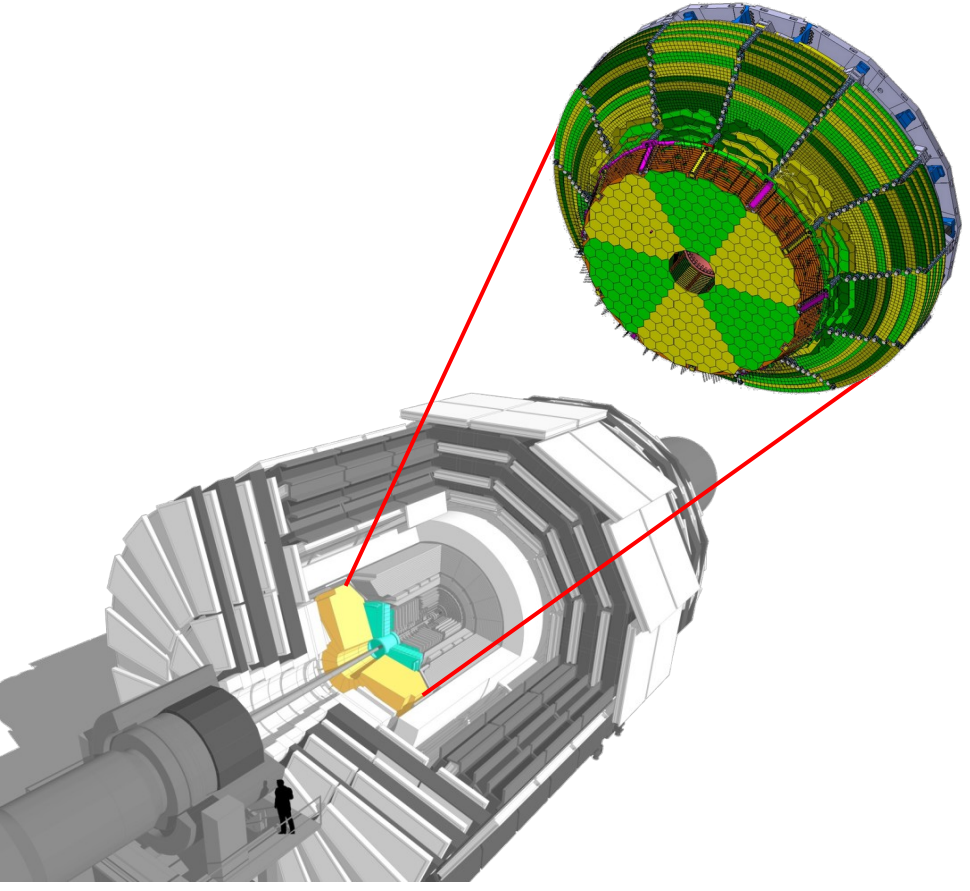


CMS needs fresh endcap calorimeters...



… and that’s how they will look like

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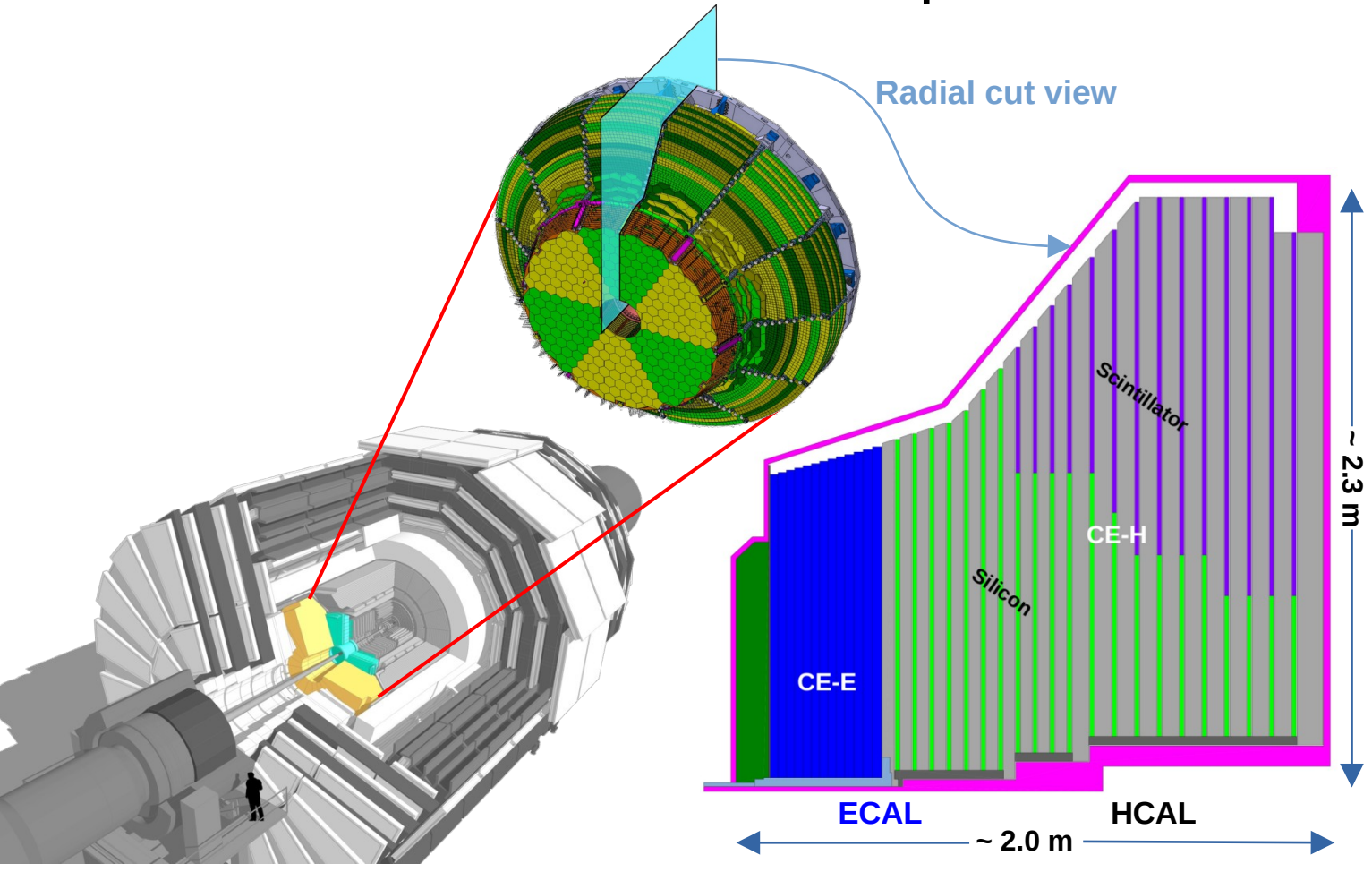

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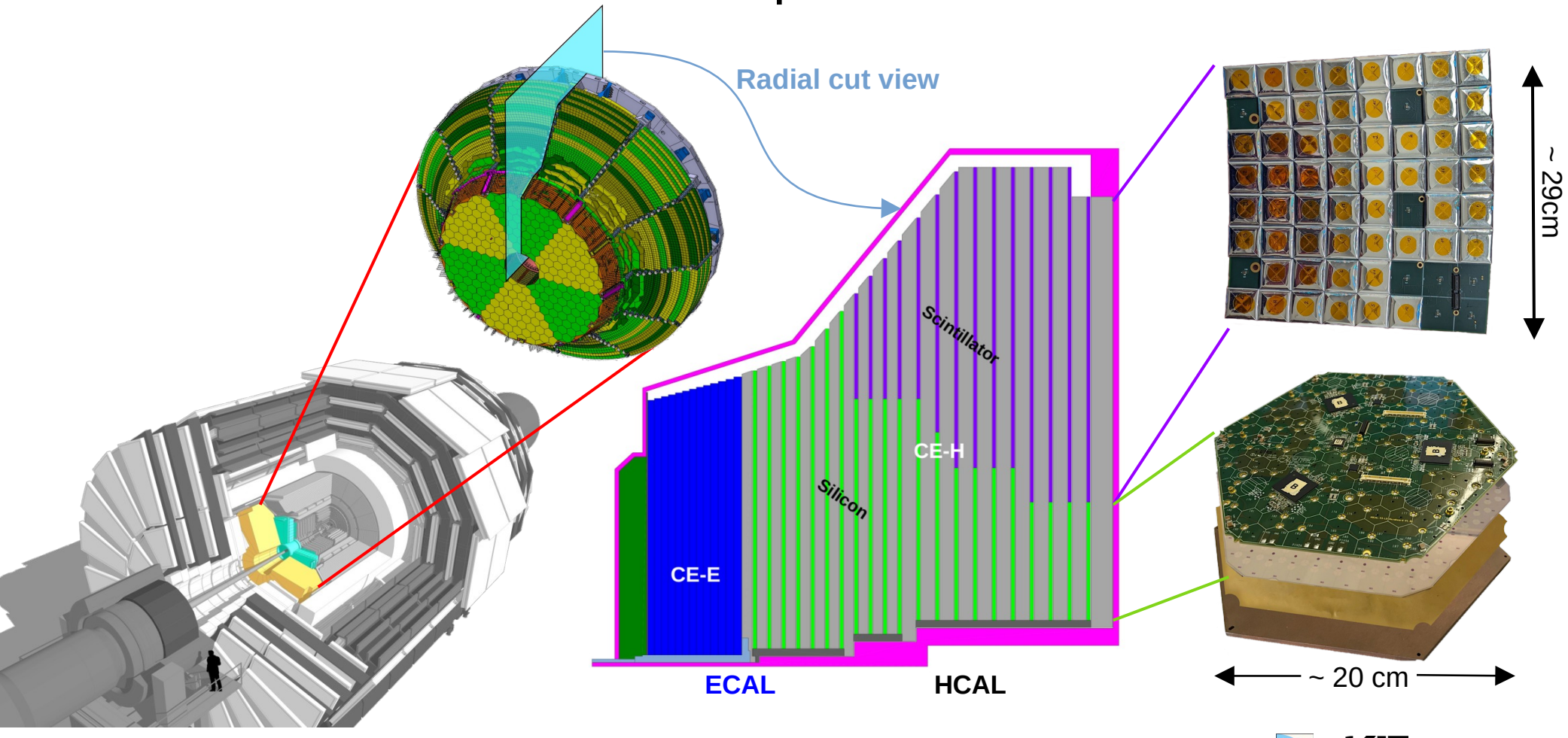
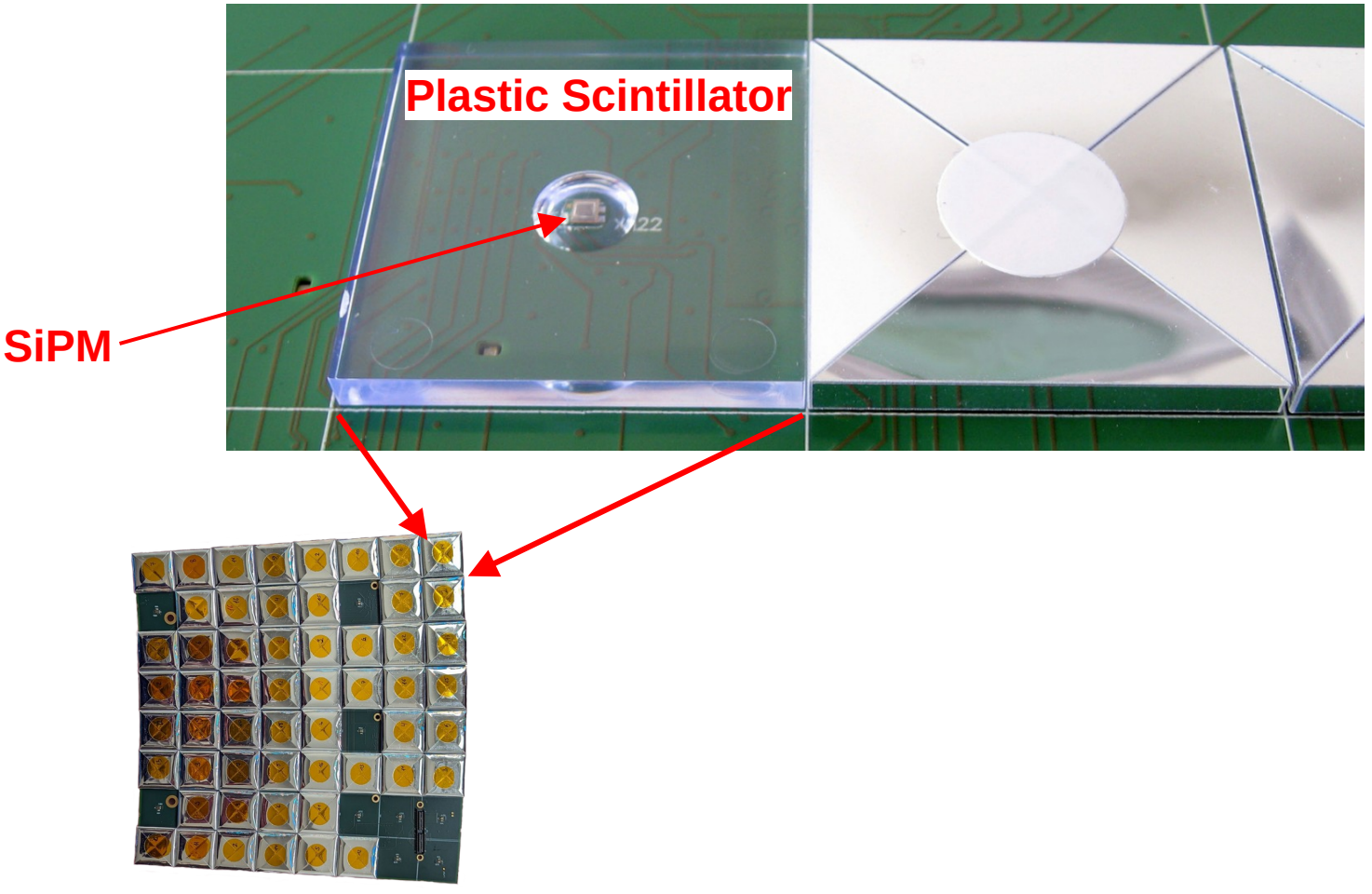
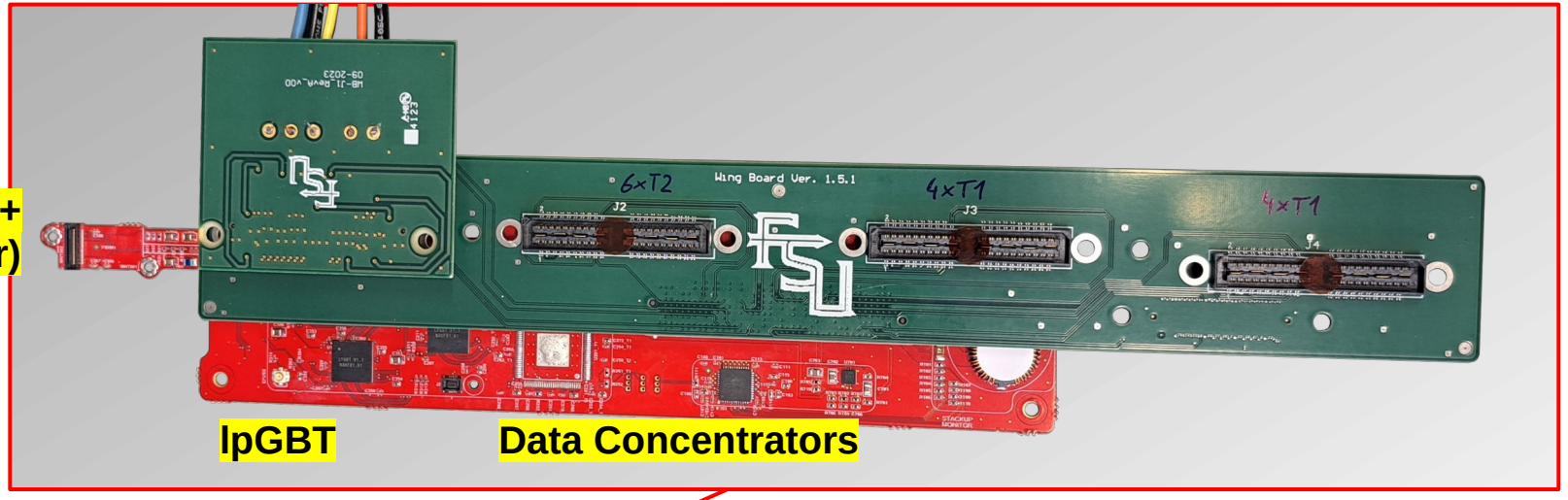
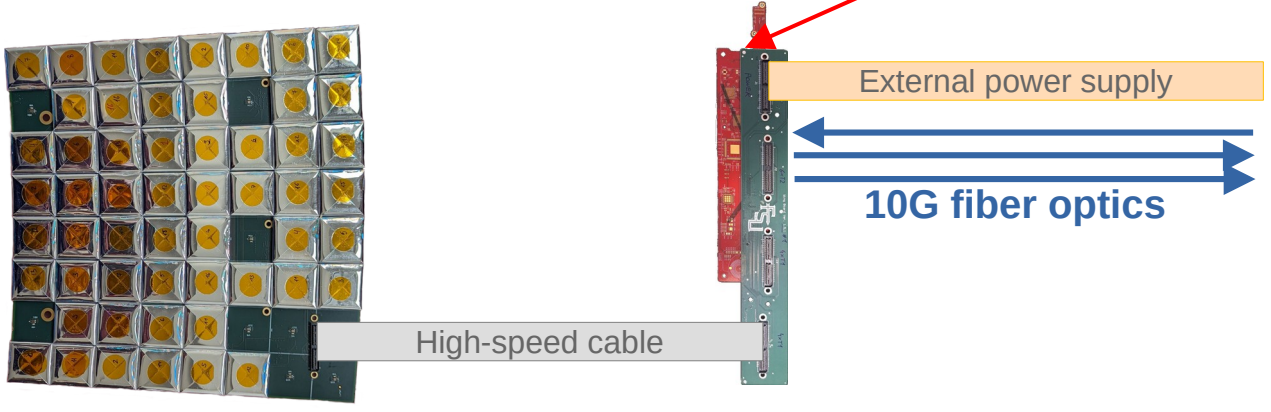
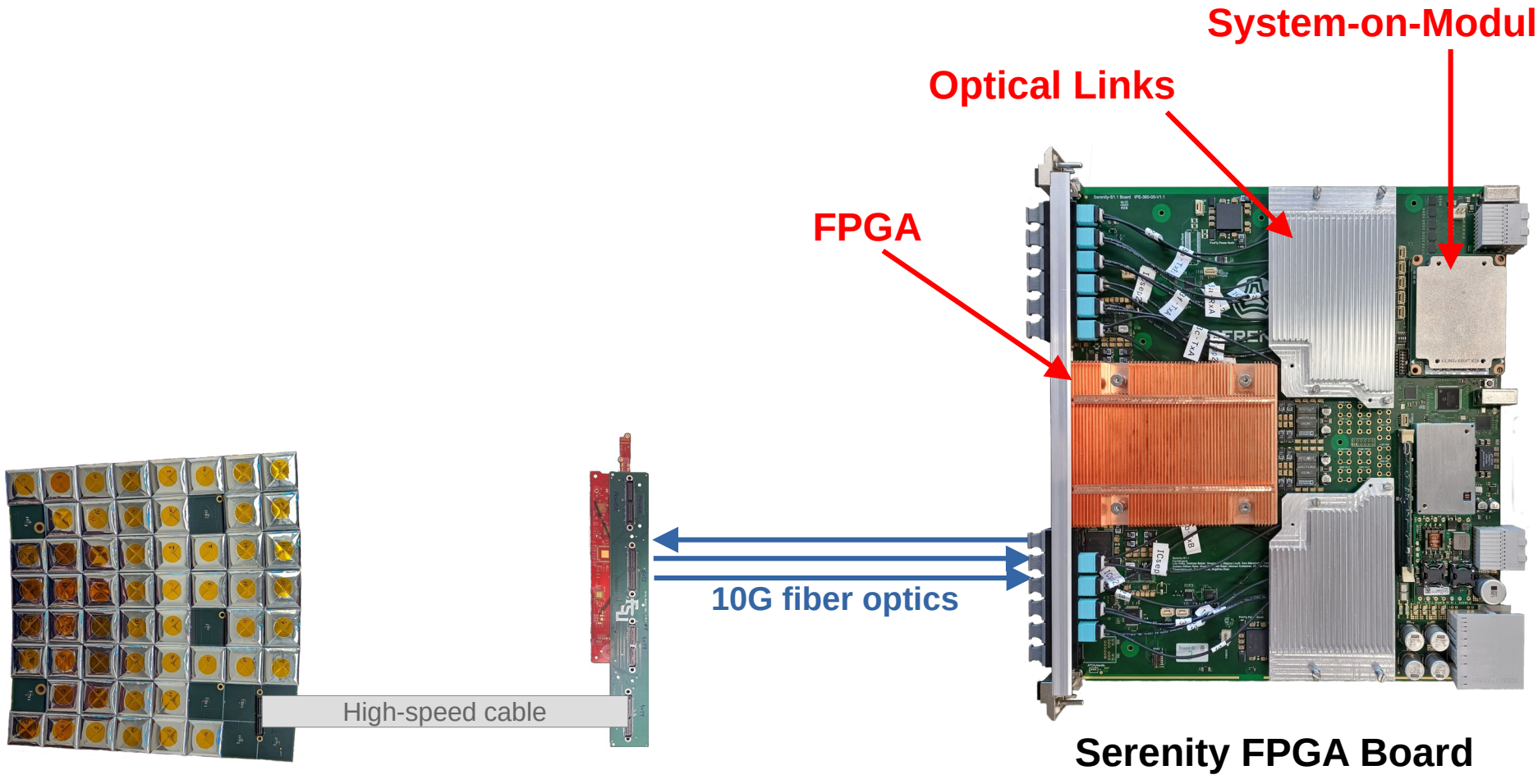



Plastic Scintillator
SiPM

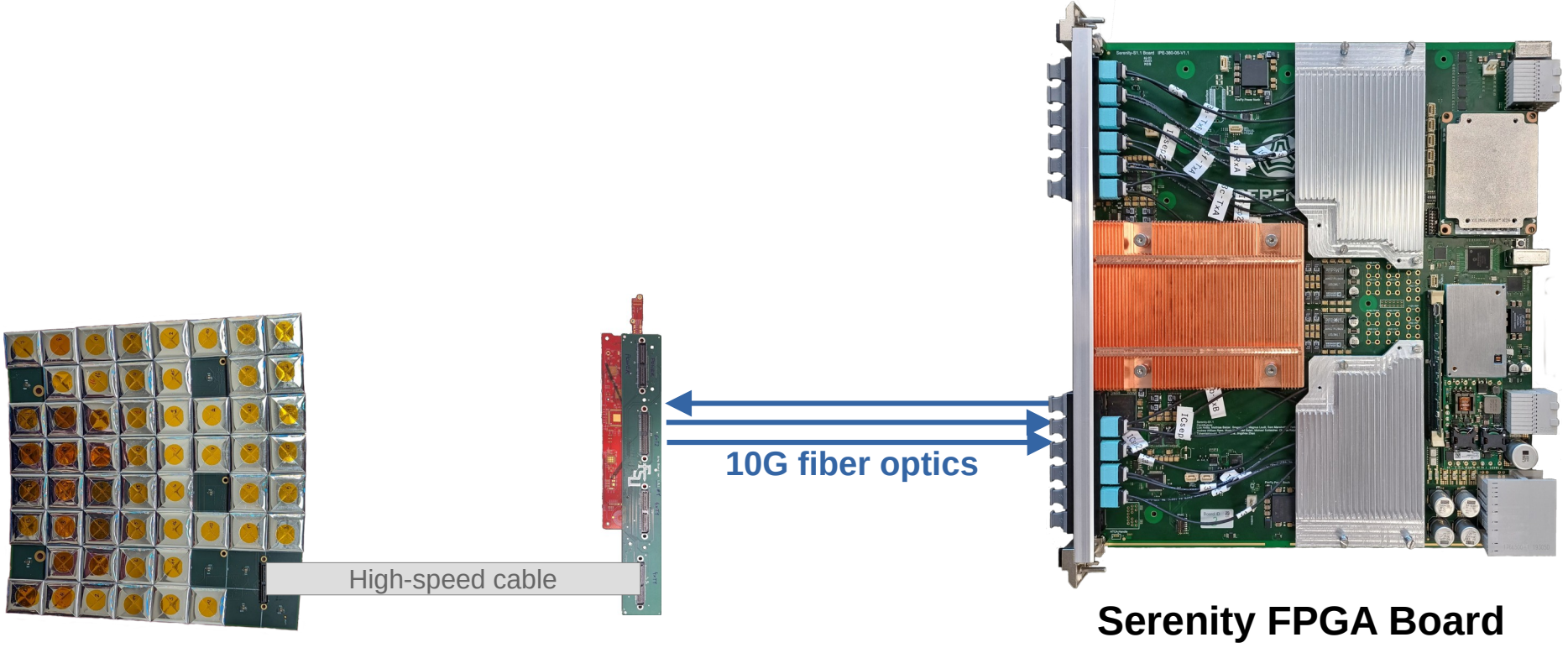
VTRx+
(optical transceiver)



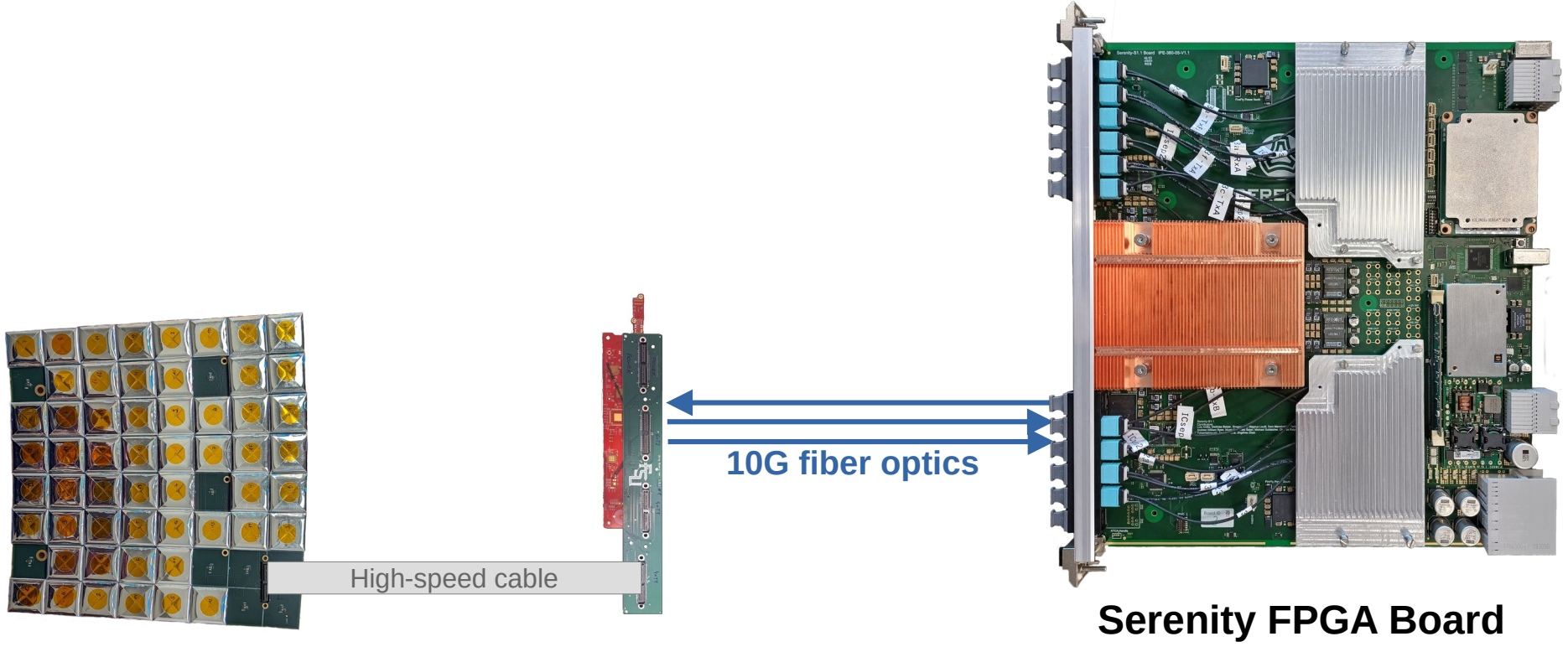



System-on-Module
Optical Links
FPGA
10G fiber optics
High-speed cable
Serenity FPGA Board

What was necessary to get a working readout chain?



What was necessary to get a working readout chain?
How do we make sure the system will work in CMS?



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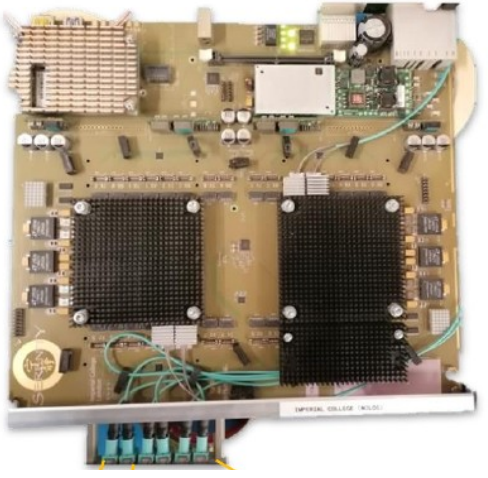
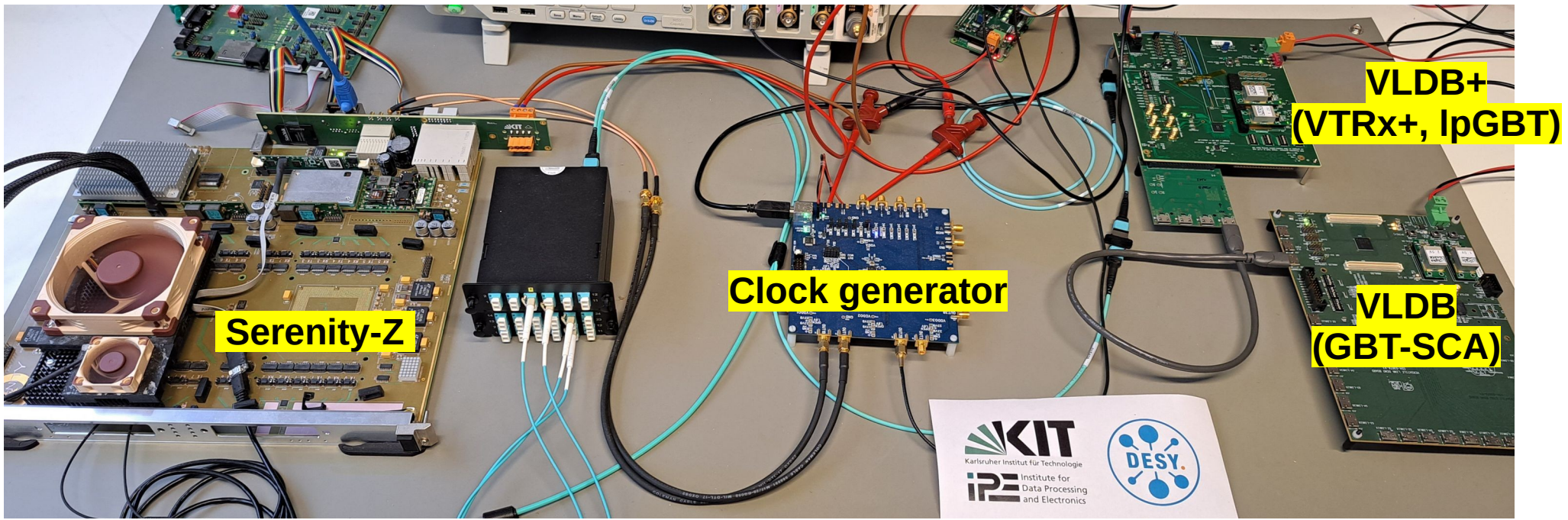


… we started only with a prototype Serenity board

Tileboard → Serenity readout: Step 1

- GBT-SCA chip provides I²C, GPIOs, ADCs, DACs to tileboards
- This chip is not present on silicon modules → no existing firmware/software
- Step 1: establish connection with GBT-SCA → use development boards



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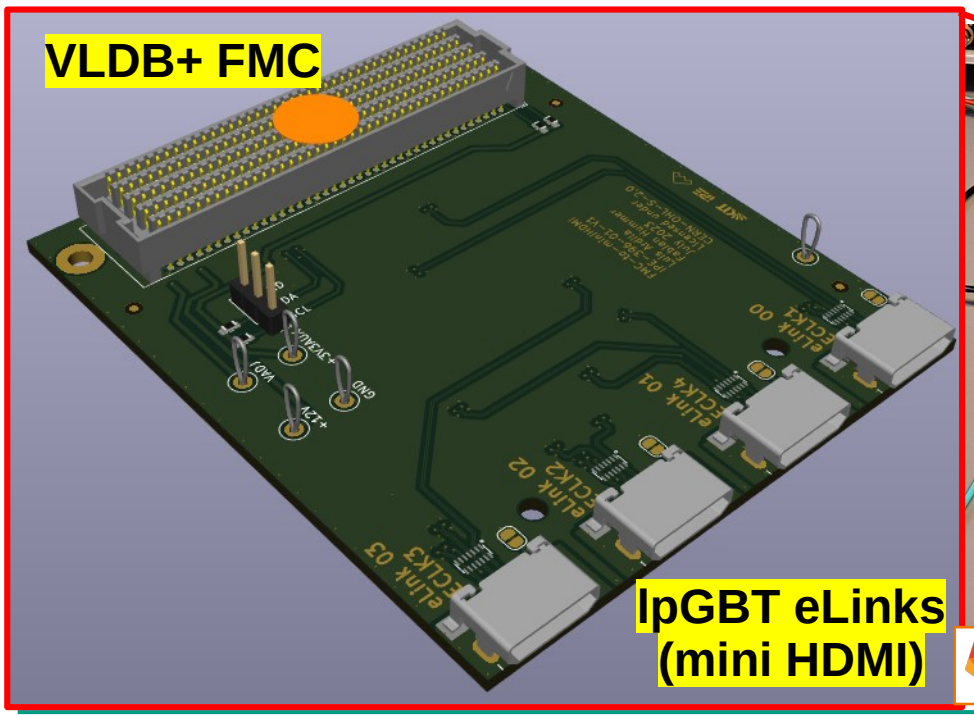
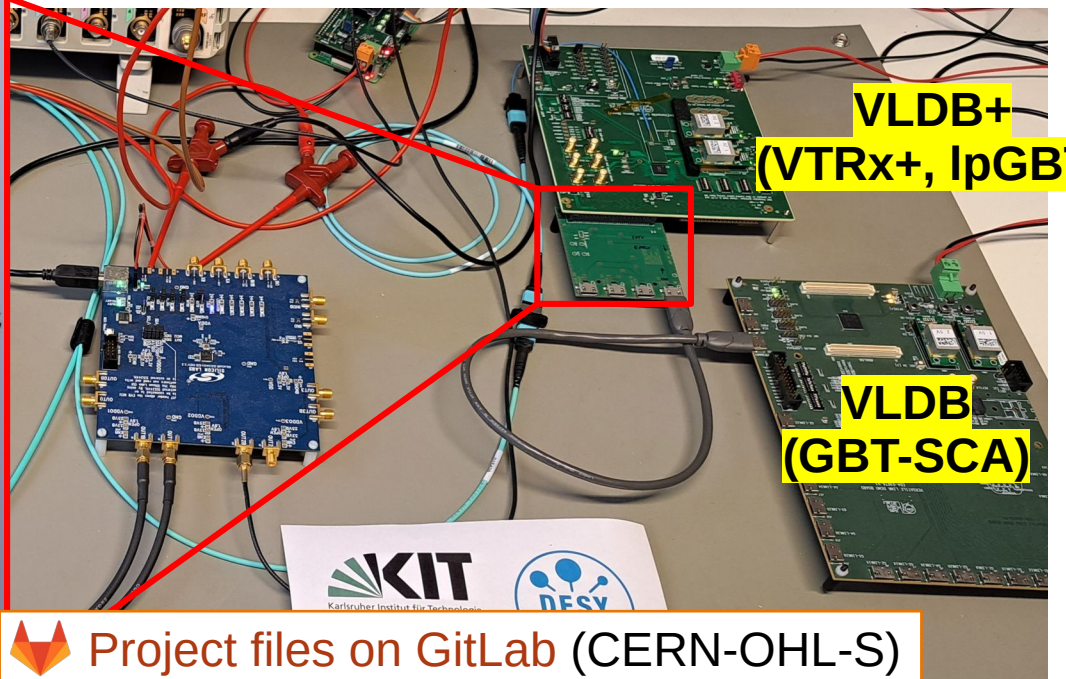
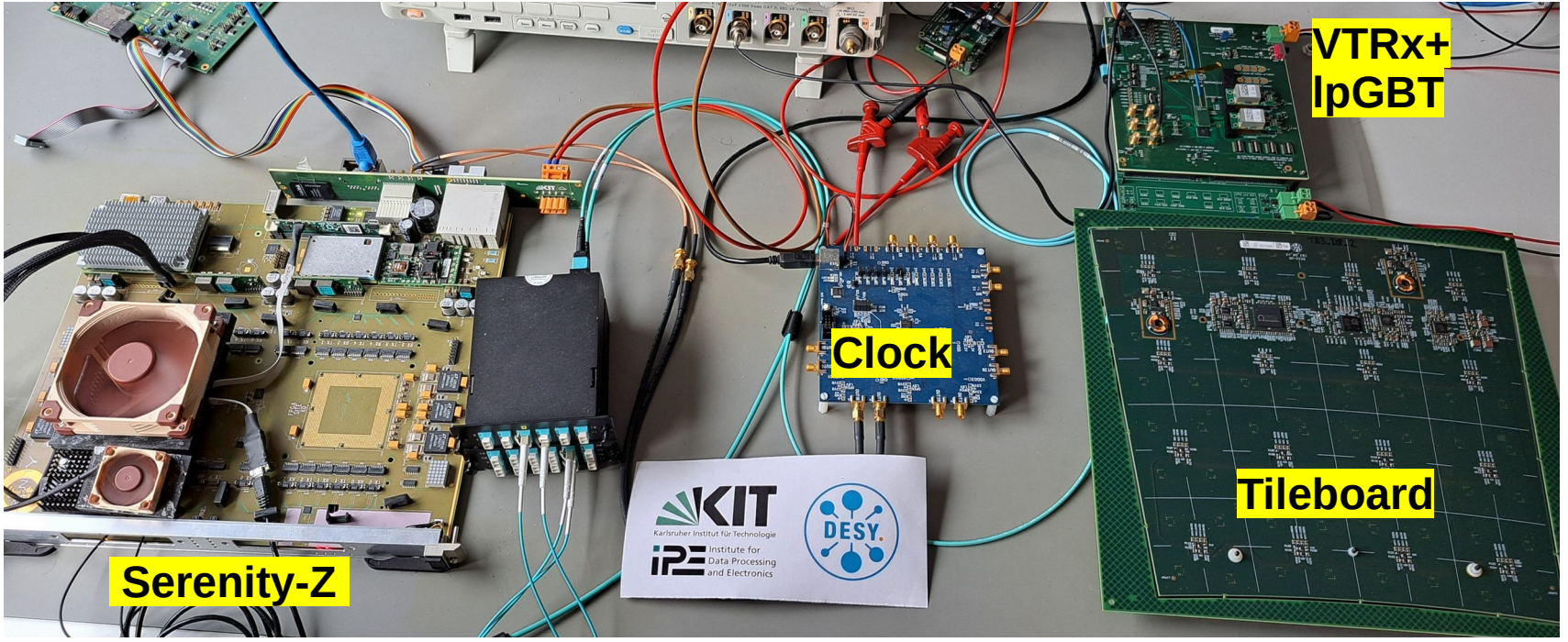




Project files on GitLab (CERN-OHL-S)

Tileboard → Serenity readout: Step 2

- Fall 2023: motherboard not yet available → **VLDB+ = „motherboard without ECON's“**
- Custom adapter board to connect tileboard to VLDB+ → develop FW and SW
- First readout of tileboard data with Serenity in January 2024



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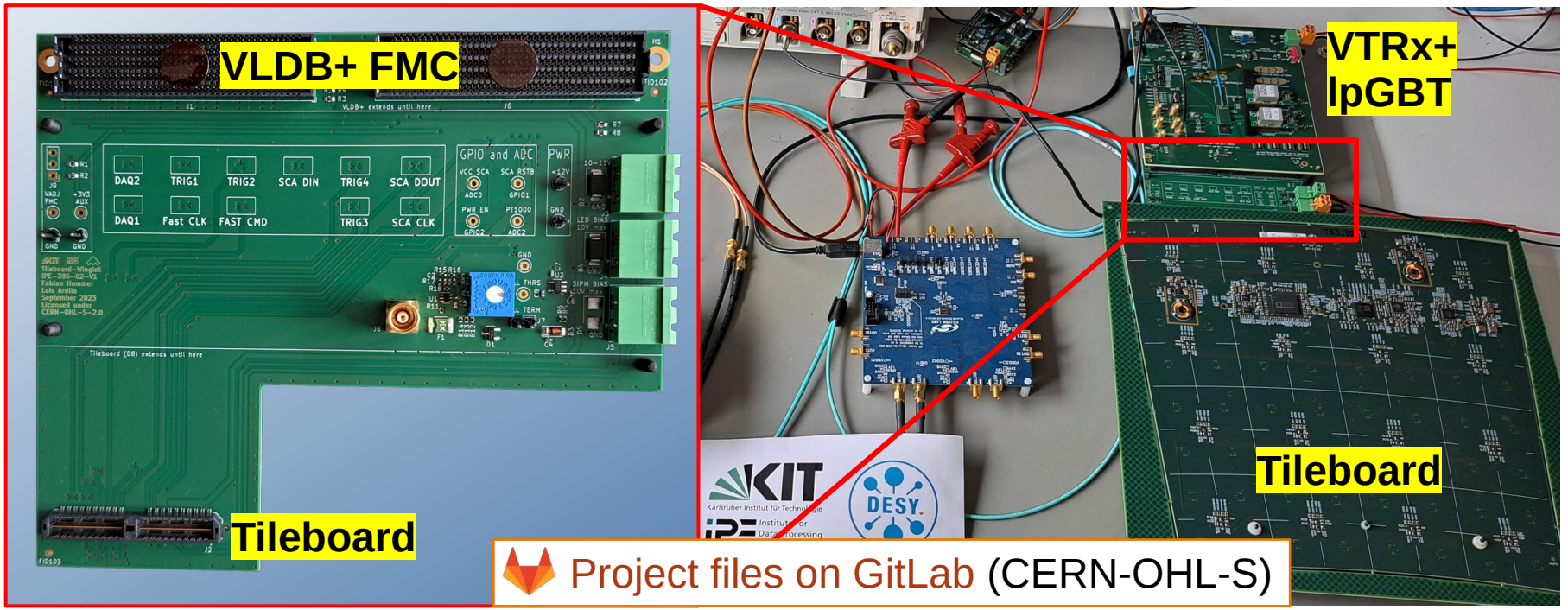
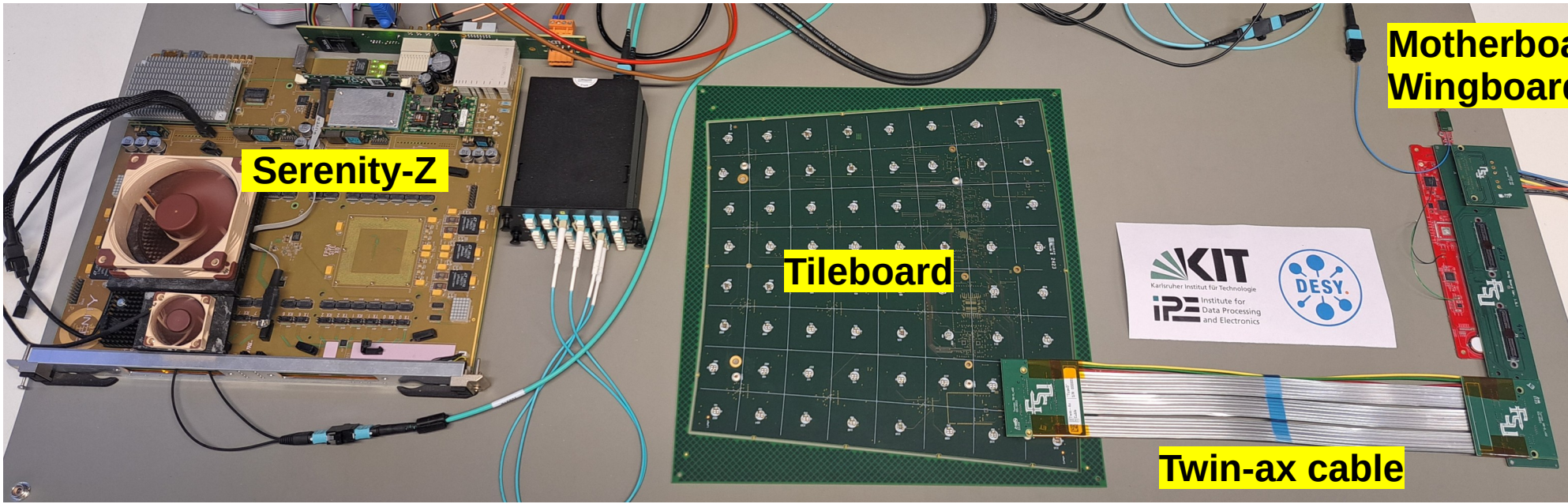


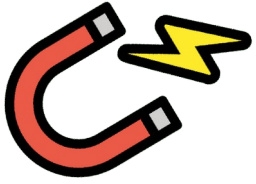
Tileboard → Serenity readout: Step 3

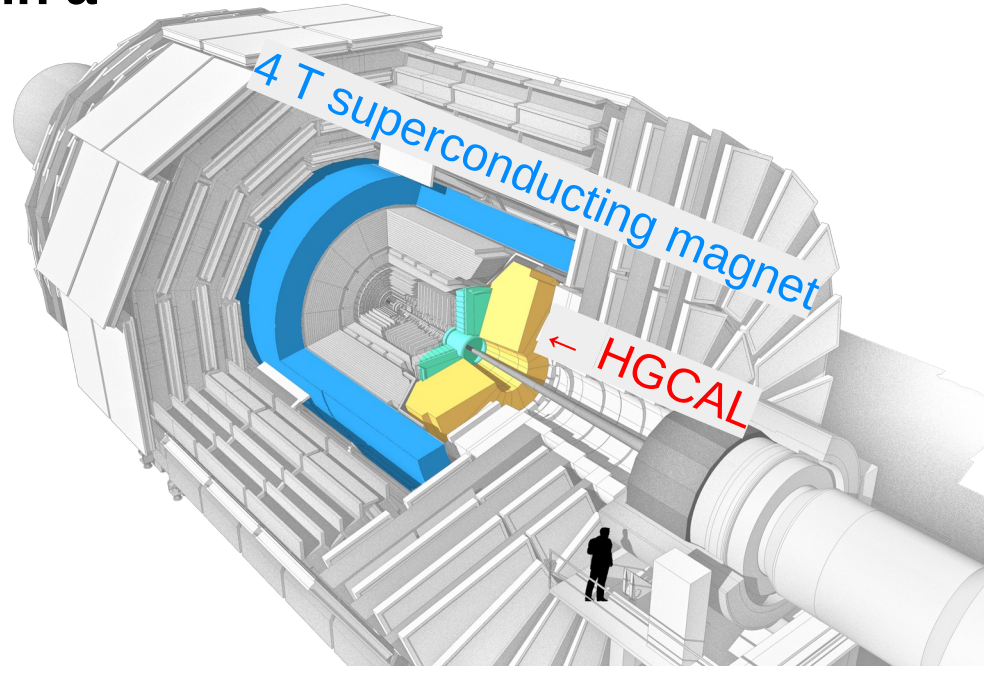
- Winter 2023: two prototype motherboards received & assembled at KIT
  - Missing DAQ data concentrator → different data format, but fully functional
- Spring 2025: per-series motherboards received → final data format



How do we make sure the system works in CMS?

Does HGCAL work in a magnetic field?





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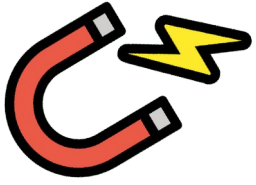

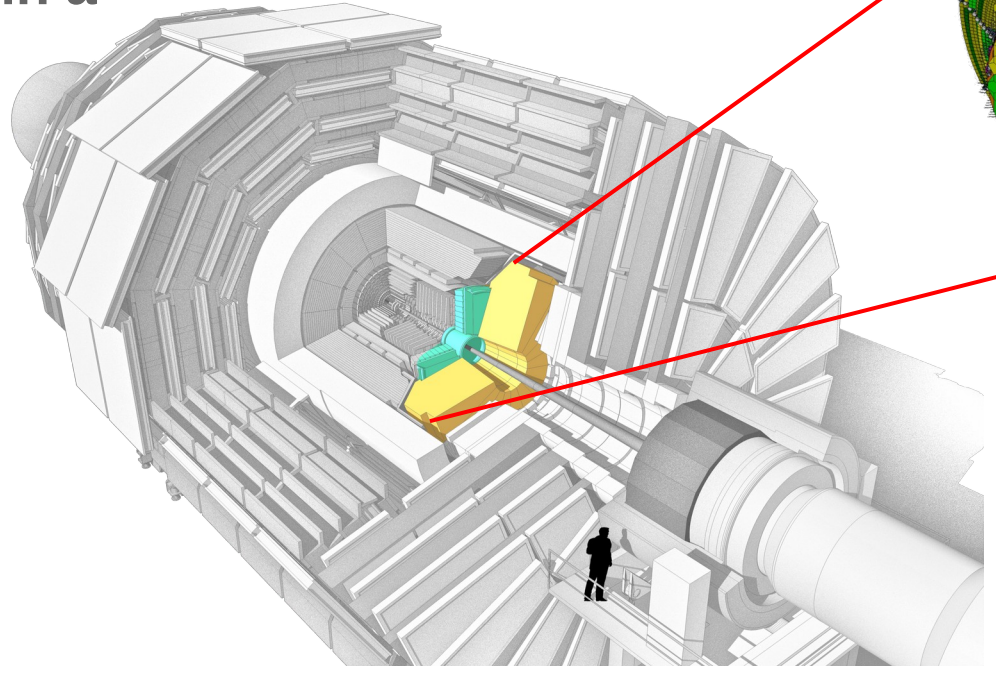

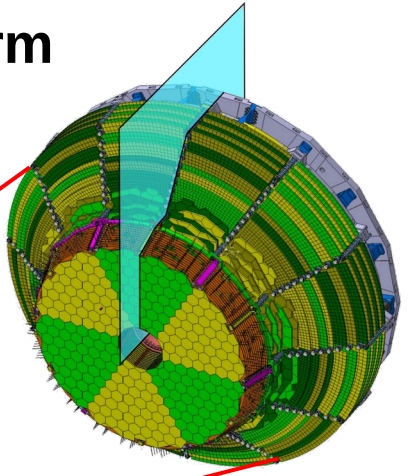

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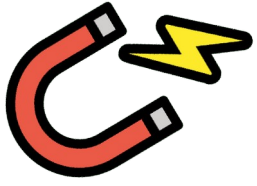
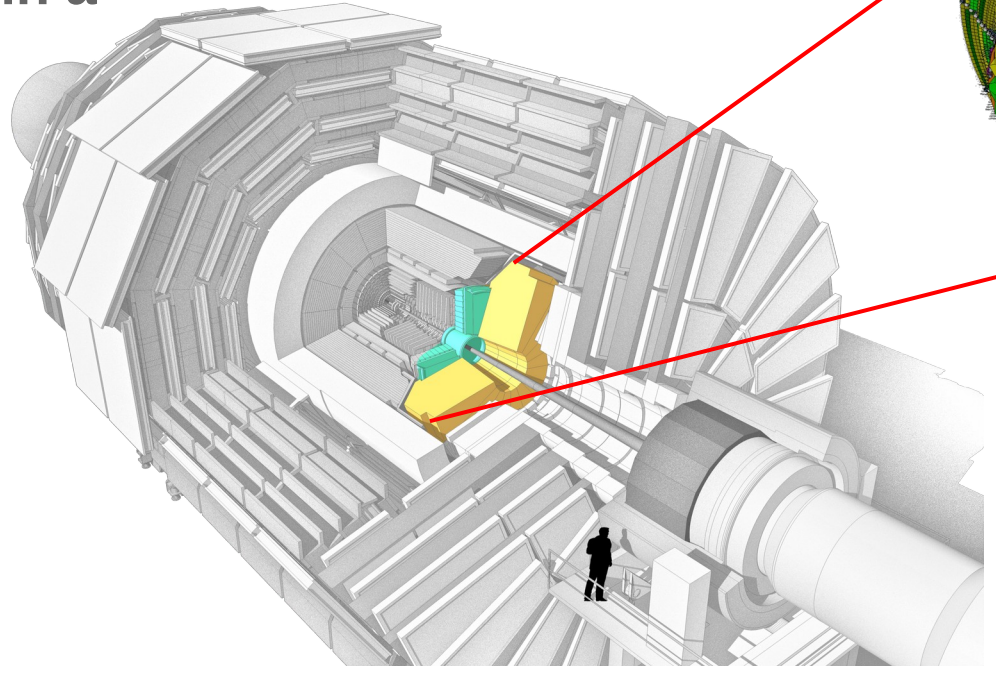
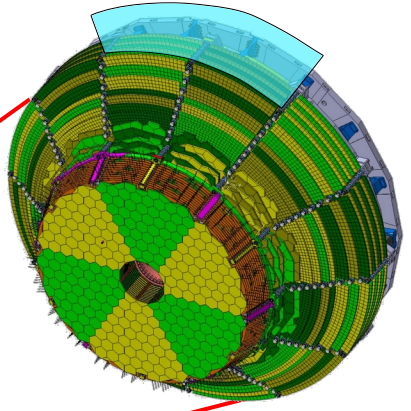




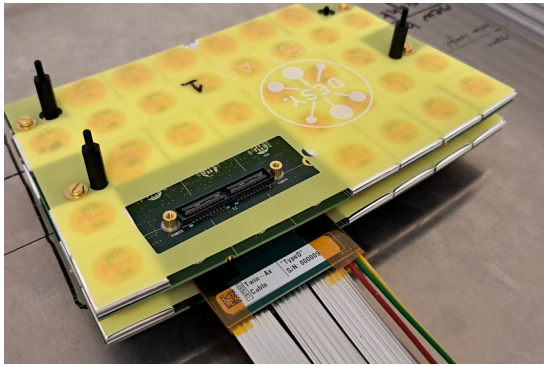


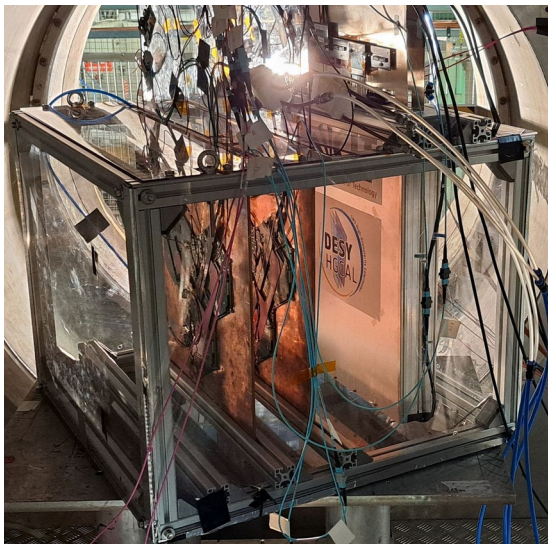
Do the layers work as a system?

Highlight #1: Beam test @ SPS H2

What did we test?

- Summer 2024 @ SPS north area
- Two tile modules in the complete readout chain
- In the 3T superconducting magnet at the H2 beam line, SPS north area at CERN
- Measurements with 120 – 200 GeV electrons and muons
- Beam time together with Silicon sensor group





Highlight #1: Beam test @ SPS H2

What did we *learn*? – Outcome & Impact

- First time the full SiPM-on-Tile readout chain was used in a particle beam!
- Stable operation in 3T magnetic field
- Synchronous readout of two tile modules
- Readout of silicon and scintillator* modules with the same Serenity

Presented at TWEPP 2024:
F. Hummer on behalf of the CMS collaboration 2025 JINST 20 C01015

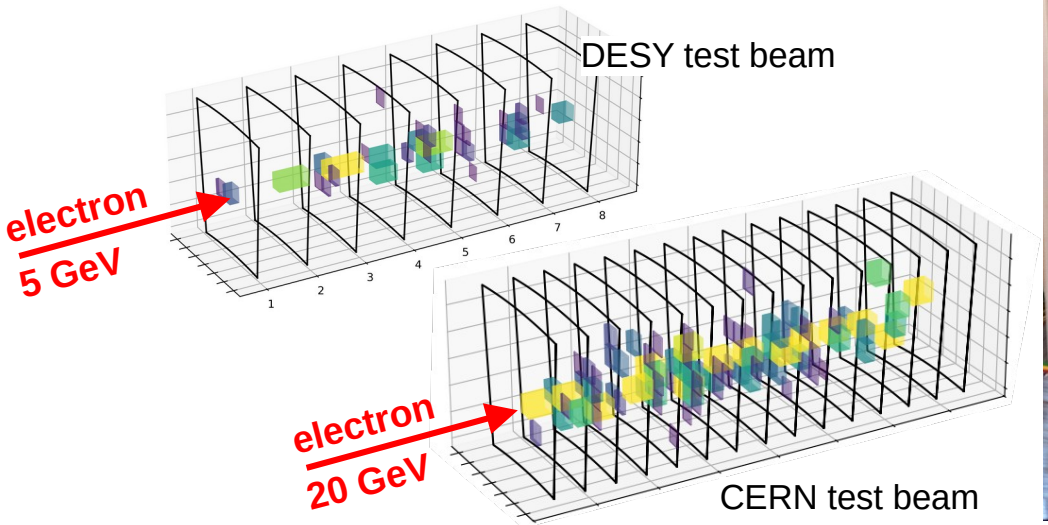
*trigger data stream only, for now...

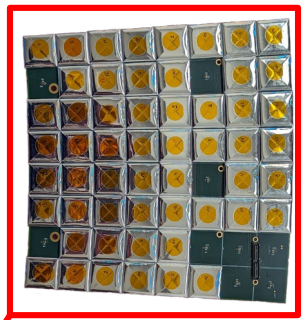
Highlight #2: Calorimeter Stack

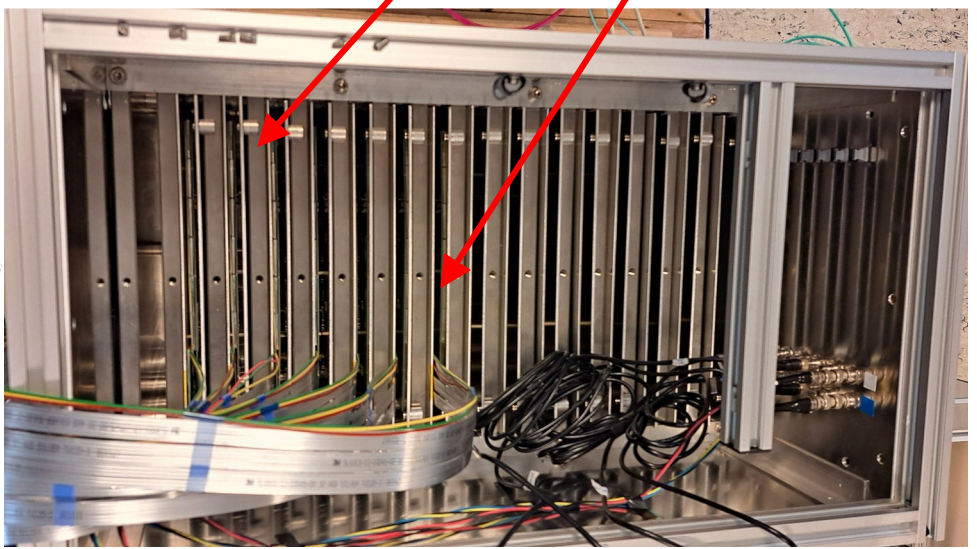
Karlsruhe Institute of Technology

What did we test?

- Verify the calorimetric performance of HGCAL's tile modules
- March 2025 @ DESY II: stack of 8 modules
- September 2025 @ CERN: stack of 15 modules
- 17 mm stainless steel absorbers







Highlight #2: Calorimeter Stack

What did we *learn*? – Outcome & Impact

- The Serenity-based readout system scales well for more tile modules
- First time tile modules were a „real“ calorimeter
- Measurement of time resolution, energy resolution (analysis ongoing)
- Compare with HGCAL simulations (ongoing)

Presented at *BTTB13*

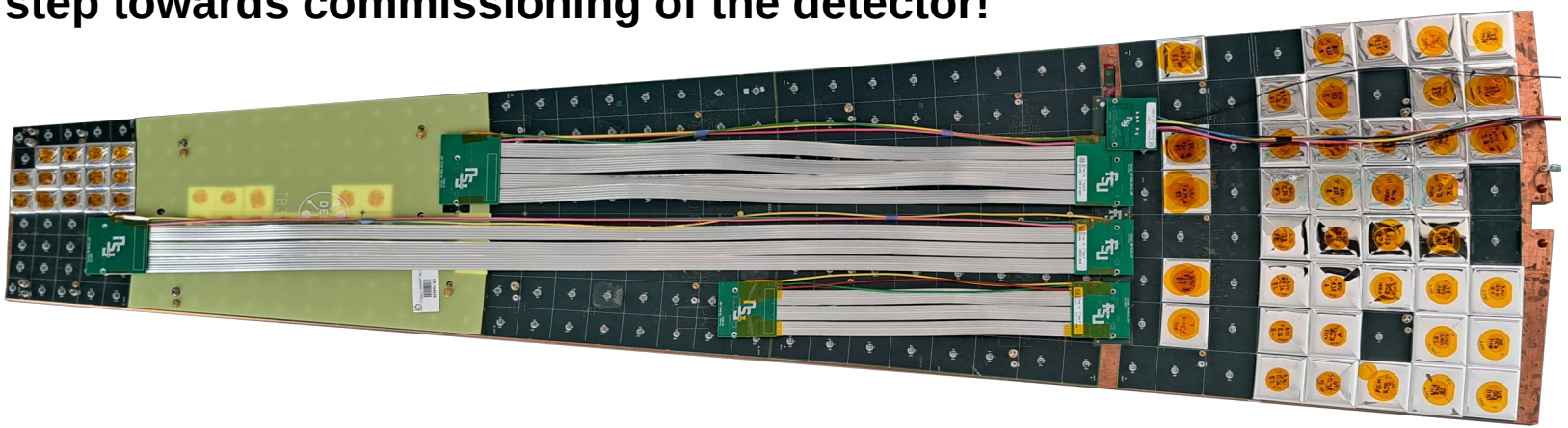
Highlight #3: Testing a slice of HGCAL

What did we test? – A slice of the HGCAL detector

- 5 pre-series tile modules from DESY → complete 10° sector
- Copper plate manuractured at KIT → realistic installation & grounding
- Pre-series motherboard with all data concentrators
- Prototype power supplies & realistic cable lengths

Poster presented at *TWEPP 2025*

Important step towards commissioning of the detector!



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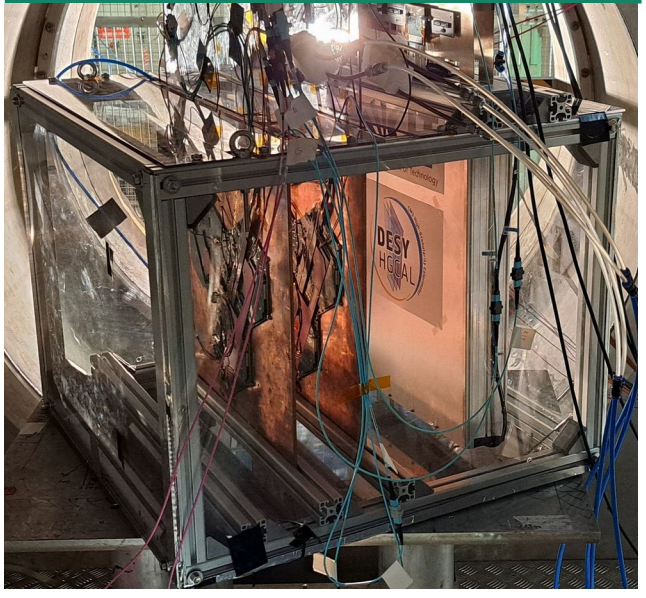
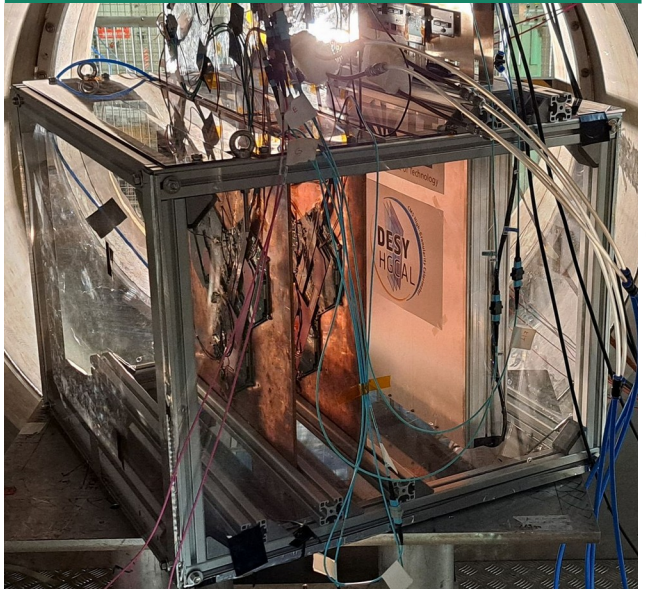


Beam tests at SPS H2
Full readout chain in the beam
Operation in magnetic field
Summer 2024

Highlight #1



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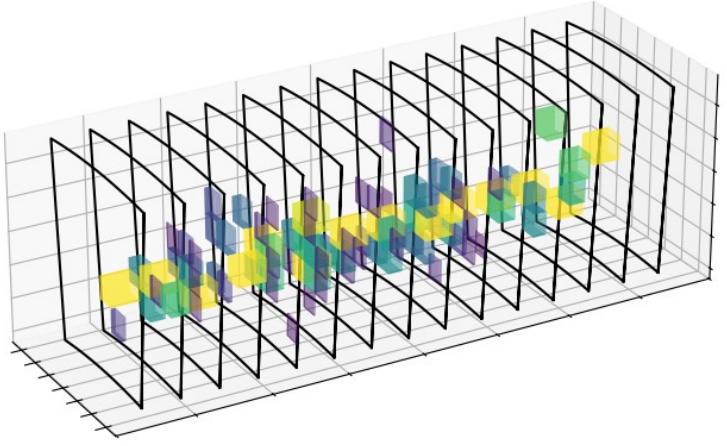
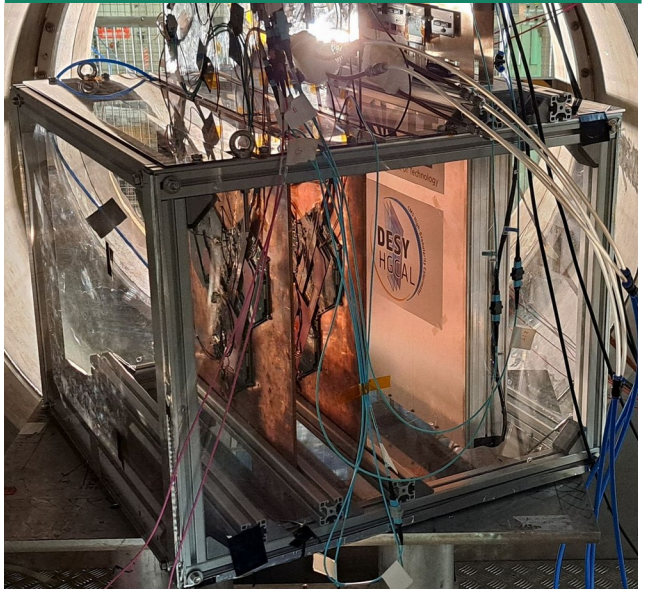


Stack beam tests
First time a „real“ calorimeter
March & September 2025

Highlight #1



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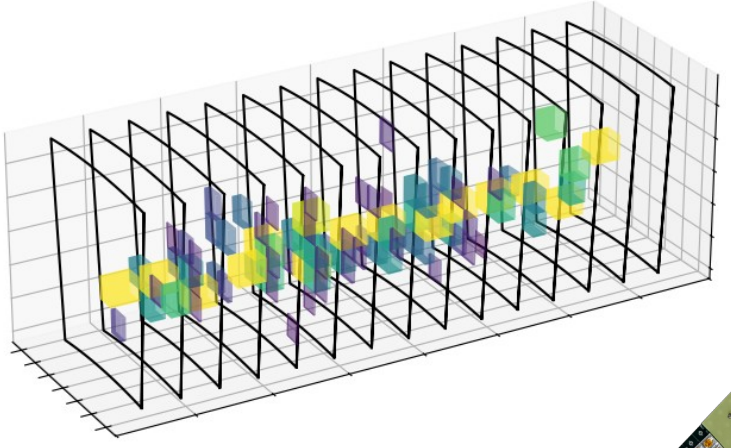
Highlight #2



Stack beam tests
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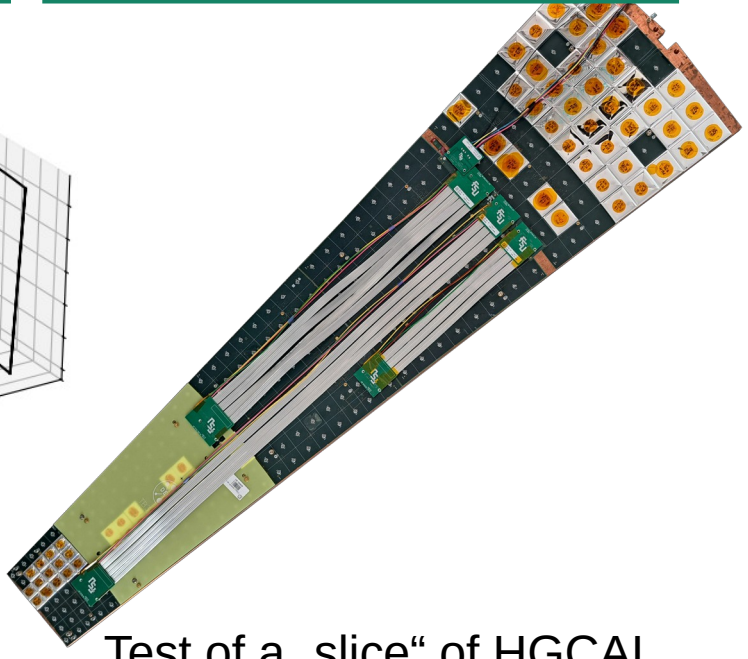
Highlight #3



Test of a „slice“ of HGCAL
System Validation
Summer 2025

Backup

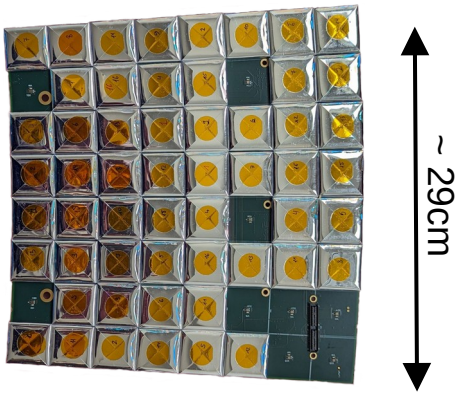
CERN Beam Test Summer 2024

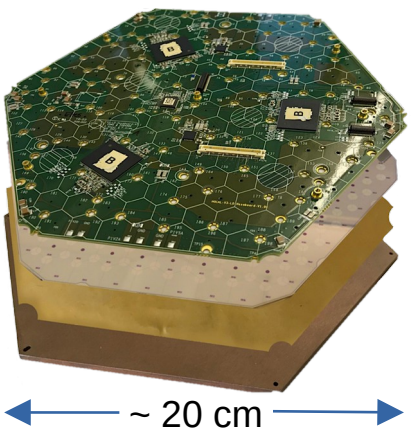
DESY Beam Test March 2025

CERN Beam Test March 2025

HGCAL's sensors in a nutshell

- Scintillator tile modules:
  - Plastic scintillator tiles read out by SiPMs
  - For lower-radiation environment
  - Sensor cell size 4 cm² … 30 cm²
  - 370 m² active area, 4k modules, 240k channels
- Silicon modules:
  - Silicon sensors wire-bonded to readout PCB („hexaboard“)
  - For high-radiation regions of HGCAL
  - Sensor cell size 0.5 cm² … 1 cm²
  - 620 m² active area, 26k modules, 6M readout channels

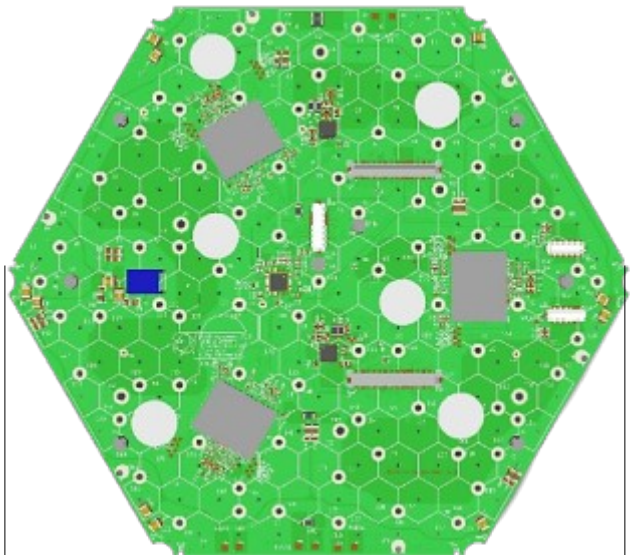




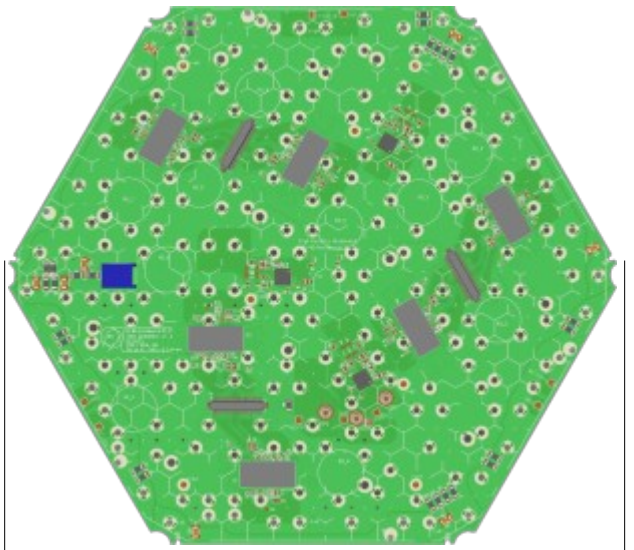
Silicon Modules – Hexaboards

- For areas with high radiation
- 620 m² of active area
- Front-end ASICS: HGCROC, LDO and RAFAEL
- Low density and high density version
- Wire bonded to Si sensor (8 inch wafer)
- Readout electronics: engines (VL+, ECONs) and wagons (passive)
- 30k boards, 6M channels

Low Density Hexaboards
3 x HGCROC
192 Si cells (1.1 cm²)

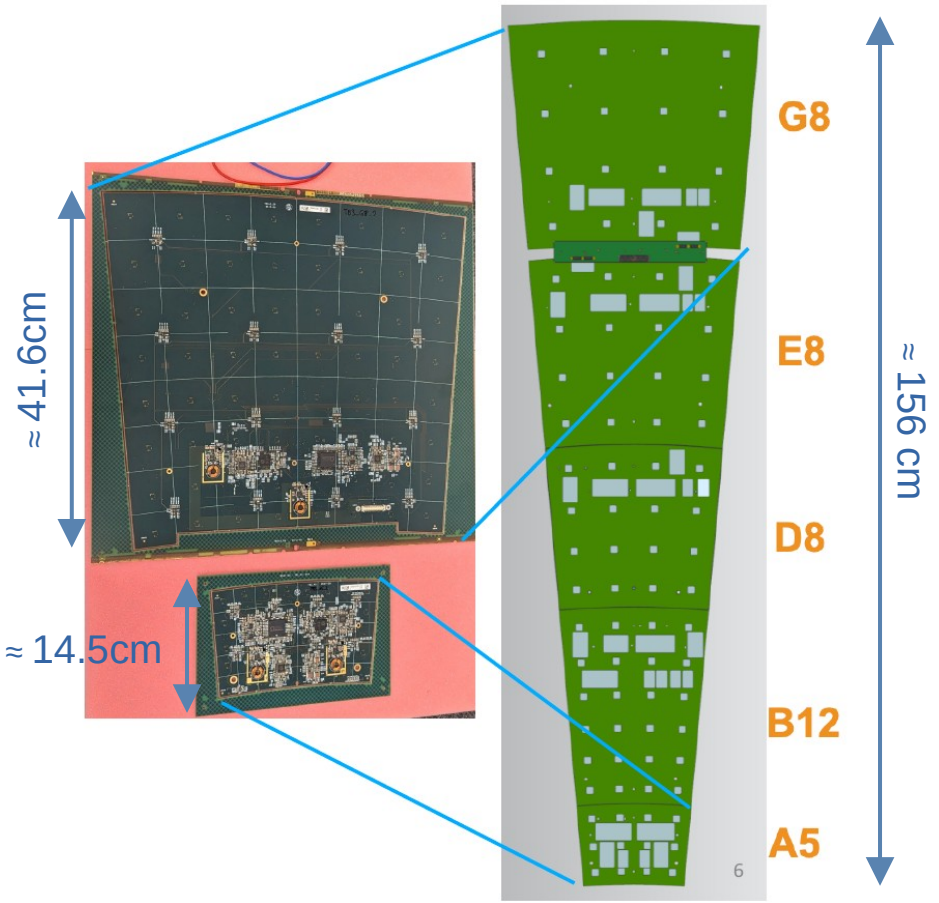


High Density Hexaboards
6 x HGCROC
432 Si cells (0.5 cm²)

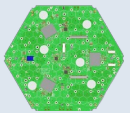


Tile Modules – Tileboards

- For areas with lower radiation
- 400 m² active area: scintillator + SiPM
- Front-end ASICS: 1-2 x HGCROC, GBT-SCA, 1-2 x ALDO
- Scintillator tiles placed directly on PCB, 4-30 cm² per tile
- LED system for calibration
- High density version with smaller tiles under consideration
- Readout electronics: Motherboard (VL+, ECONs, RAFAEL) and wingboards (passive)
- 4k boards, 240k channels

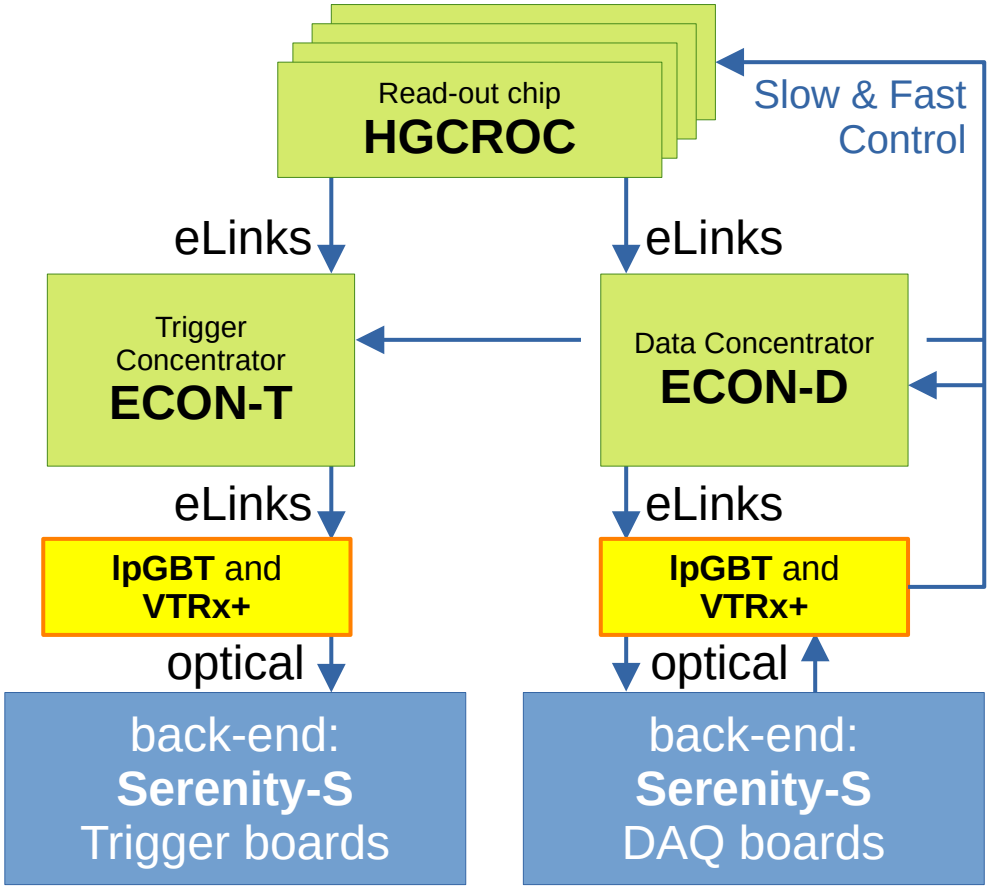


Silicon / SiPM-on-Tile FE Differences

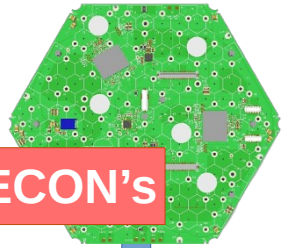
	LD Hexaboard 	HD Hexaboard	Tileboard / Motherboard / WB 
HGCROC	3 per LD Hexaboard	6 per HD Hexaboard	1 for most Geometries / 2 for B12 Tileboard
GBT-SCA	N/A	N/A	1 GBT-SCA per Tileboard
ECONs	ECON Mezzanine on the Hexaboard		2 ECON-T + 1 ECON-D on the Motherboard
RAFAEL	1 per Hexaboard		1 per Motherboard
lpGBT	3 per LD Engine	6 per HD Engine	2 per Motherboard (DAQ + Trigger)
VTRx+	1 per LD Engine	2 per HD Engine	1 per Motherboard
linPol12	Engine		Motherboard
LDO	Hexaboard and Engine		1 on Motherboard, 2 per Tileboard
bPol12	DCDC mezzanine on the Hexaboard		1 per Motherboard, 2 per Tileboard
ALDO	N/A	N/A	2 per Tileboard

The HGCAL Readout Chain

- Trigger data:
  - Sent for each bunch crossing
  - Reduced formats, e.g. sum of multiple sensor cells
- DAQ data:
  - Full event information (ADC/ToT + ToA)
  - Only sent on demand (L1 trigger accept)



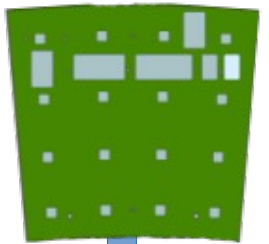
Core Feature: shared* Readout Chain



Wagon

ECON's

Engine



Wingboard

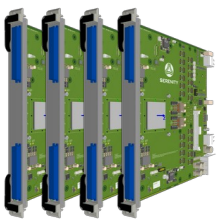
Motherboard

ECON's

Detector module
HGCROC (SiPM and Silicon version)

Passive connector board
different shapes → integration

Motherboard
Data to fiber optics (lpGBT, VTRx+)



Back-end
- Serenity S1

* with some specific parts to each

Serenity-S1 FPGA Card

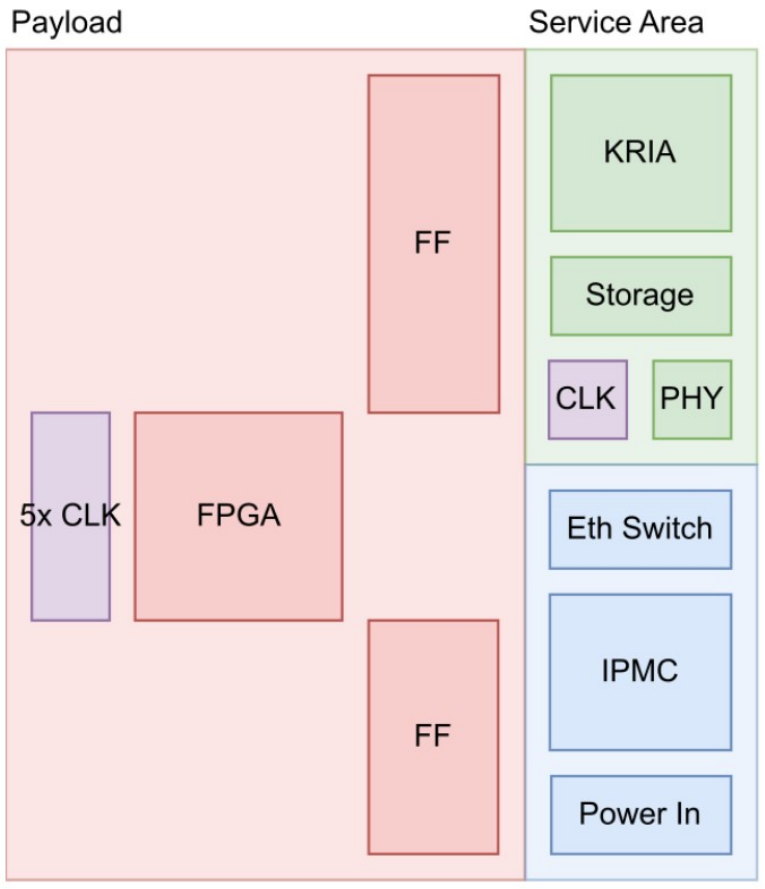


Figure by Torben Mehner

- Board Infrastructure
  - Xilinx KRIA SoM
  - Clock, power, PHY
  - SD, SSD
- ATCA Infrastructure
  - Backplane connectors
  - IPMC (OpenIPMC DIMM module)
  - Power input
  - Ethernet switch
- Payload
  - FireFly optical transceivers
  - VU13P FPGA
  - Clocks