14th MicroTCA Workshop for Industry and Research

2th - 4th December 2025

Deutsches Elektronen-Synchrotron DESY

Hamburg, Germany

Book of Abstracts

For more information please visit: https://mtcaws.desy.de

14th MicroTCA Workshop for Industry and Research

The workshop deals with MicroTCA.4 (Micro Telecommunications Computing Architecture) and brings together experts and beginners from industry and research.

In the past, MicroTCA.4 was largely driven by the particle accelerator community, but then expanded to photon science and plasma fusion facilities. More recently, astrophysics-observatories, gravitational wave detection, axion particle detection, and quantum computing plan to implement the standard.

We strive to make each workshop better than the last and welcome your suggestions for improvement – please do not hesitate to contact the local organization team.

The Workshop's main topics include:

- Applications in research facilities
- Applications in industry
- New Products
- New Technologies
- Future of standard and interoperability
- Software and firmware
- Industry Exhibition – presentation of modules and systems from industry and research

Chair and Advisory Committee:

Kay Rehlich (Chair)	DESY
Holger Schlarb (Chair)	DESY
Christian Ganninger	nVent - Schroff GmbH
Tobias Hoffmann	GSI
Timo Korhonen	ESS
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Rong Liu	Beijing DAQ Technology Co. Ltd
Alex Malcom	VadaTech Ltd
Paul Chu	Nanjing University
Alan Justice	Oak Ridge National Laboratory
Jan Marjanovic	Atom Computing
Fumihiko Tamura	J-PARC
Axel Winter	IPP

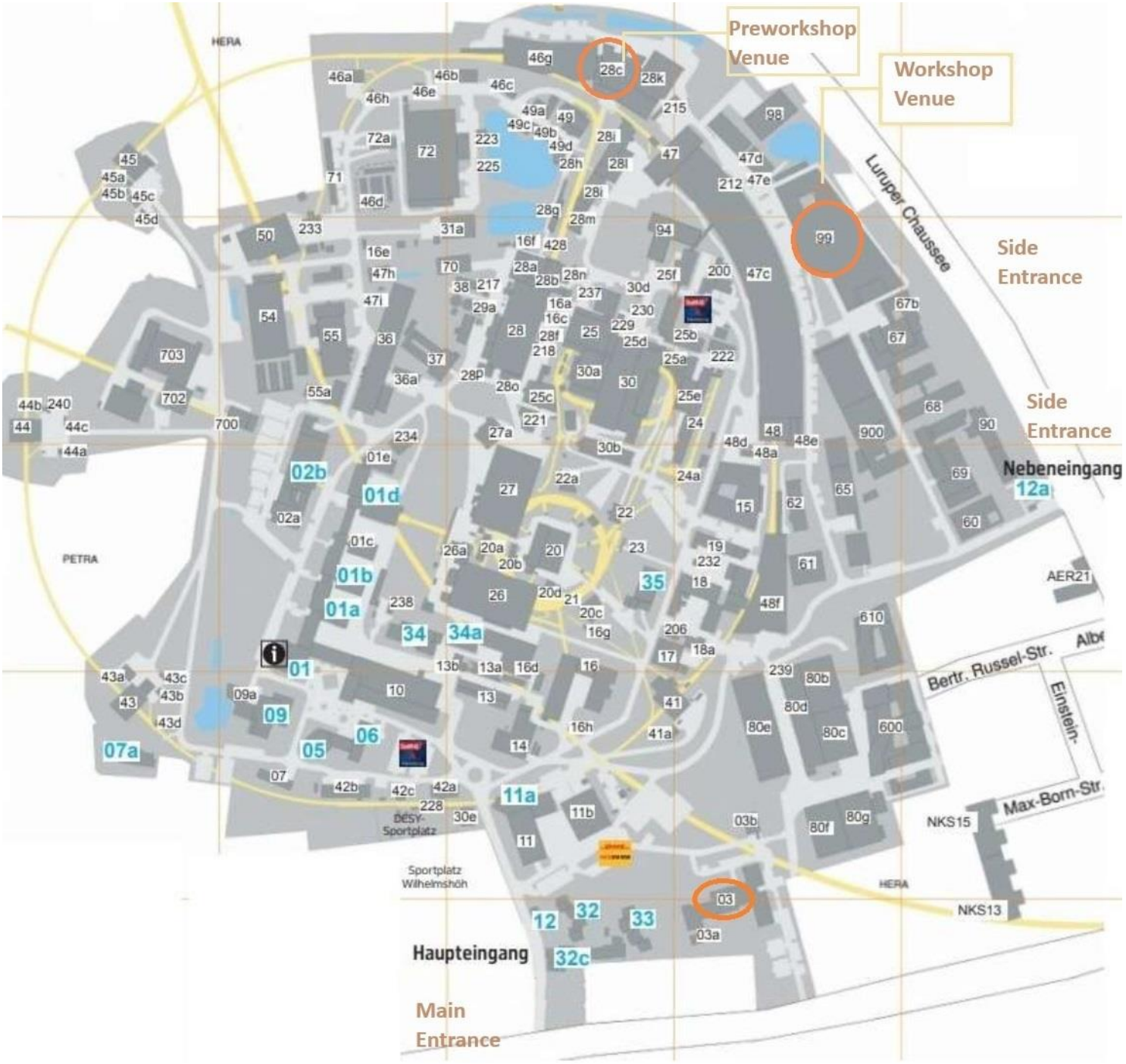
Local Organizing Committee:

Hanna Kunze	DESY

General Information

Venue	DESY CFEL, Building 99, Deutsches Elektronen-Synchrotron, Notkestraße 85, 22607 Hamburg
Preworkshop Venue	FLASH Meeting room (bulding 28c, 2nd floor)
W-LAN	WLAN name: **Science-Hotspot** The guest WLAN does not require user registration. Users only have to accept the usage regulations on the portal website of the WLAN network.
Registration	2th Dec., 09:00-13:00 Venue Location
Meals	A small lunch, coffee breaks, tea and coffee will be offered during the workshop in the CFEL building.

Workshop Venue at DESY



Hamburg Harbour Tour via MS HAMMONIA

with Workshop Dinner

The workshop dinner will take place on the MS HAMMONIA. We will take dinner while cruising in Hamburg's famous harbour. The ship departs from Überseebrücke at 19.30 and returns at 22.30.

We provide shuttle busses starting at 18:15 in front of the CFEL. The shuttle busses will return to DESY after the dinner at 23:00.
If you are not taking the bus shuttle, please make sure to be at Überseebrücke at 19:00

Public transport information: Leave DESY at the side entrance. Take bus line 3 from "Luruper Chaussee (DESY)" to "U Feldstraße", then U3 to "Baumwall".
The trip takes about 35 minutes.

DESY tours

We offer two DESY tours, organized by the MSK group of DESY.

Tour 1: 2th December, 12:30 – 13:30

Tour 2: 3th December, 12:30 – 13:30

Meeting point for the tours: Registration desk in the CFEL foyer.

Workshop Program

Tuesday, December 2, 2025

MTCA Tutorial: Basics (9:00-10:30)

Time	Title	Speaker
9:00-9:05	Introduction	Kay Rehlich
9:05-9:35	MicroTCA Basics	Ralf Waldt (Schroff GmbH)
9:35-10:05	MicroTCA Management	Heiko Koerte (N.A.T.)
10:05-10:30	Communication links, clocks and triggers	Kay Rehlich

MTCA Tutorial: MicroTCA Hardware Design (9:00 -10:30)

Time	Title	Speaker
9:00-10:00	Hardware Design in MicroTCA	Behzad Boghrati (DESY)
10:00-10:30	EMI consideration for precision analogue electronics in MicroTCA	Frank Ludwig (DESY)
10:30-11:00	Coffee Break	

MTCA Tutorial: Timing session (11:00 -12:30)

Time	Title	Speaker
11:00-11:30	The MRF Timing System	Jukka Pietarinen (Micro-Research Finland Oy)
11:30-12:00	The White Rabbit based Timing System	Dietrich Beck (GSI)
12:00-12:30	The DESY x2 and x3 Timing Systems	Victor Andrei (DESY)

MTCA Tutorial: Firmware and Software Frameworks, FWK and ChimeraTK (11:00 -12:30)

Time	Title	Speaker
11:00-11:45	FWK Firmware Framework	Cagil Guemues, Gianmarco Ricci (DESY)
11:45-12:30	Rapid hardware integration with the ChimeraTK software framework	Martin Hierholzer (DESY)
12:30-14:00	Lunch	

Session 1 (14:00-15:30) Chair: Holger Schlarb (DESY)

Time	Title	Speaker
14:00-14:15	Welcome to DESY	Edgar Weckert (DESY)
14:15-14:30	Introduction to workshop	Holger Schlarb (DESY)
14:30-14:45	Deployment and Development of MicroTCA at ESS	Faye Chicken (ESS)
14:45-15:00	Status of MicroTCA at the Spallation Neutron Source	Thomas Justice (ORNL)
15:00-15:15	Summary of MTCA Workshop in Japan 2025 and Status of MTCA at J-PARC in 2025	Fumihiko Tamura (J-PARC)
15:15-15:30	RF Beam Noise Feedback System for the High-Luminosity LHC Crab Cavities	Dimitar Hristov Marinov (CERN)
15:30-15:45	Discussion	
15:45-16:15	Coffee break	

Session 2 (16:15-18:00) Chair: Tobias Hoffmann (Helmholtzzentrum für Schwerionenforschung)

Time	Title	Speaker
16:15-16:30	New FPGA, CPU and ADC/DAC products	Karl Judex (EMCOMO Solutions AG)
16:30-16:45	Overview of DMCS Projects and MicroTCA.4 Developments	Dariusz Makowski (Lodz University of Technology)
16:45-17:00	Engineering Challenges in Scaling MicroTCA for High-Power Double Full-Size AMC Configurations	Christian Ganninger (nVent SCHROFF)
17:00-17:15	New building blocks and uplink solutions with the NAT-MCH	Heiko Körte (N.A.T.)
17:15-17:30	Vadatech: Accelerating Your Development (DAQ ToolSuite)	Alex Annis (VadaTech Ltd)
17:30-17:45	Libera Brilliance X: MTCA.4 Readout Electronics for Electron Synchrotrons.	Peter Paglovec (Instrumentation Technologies)
17:45-18:00	Discussion	

Wednesday, December 3, 2025

Session 3 (9:00 - 10:30) Chair: Thomas Holzapfel (powerBridge)

Time	Title	Speaker
9:00-9:30	**Keynote: Systematic Approaches for Accelerator Controls**	Chungming (Paul) Chu (Nanjing University)
9:30-9:45	An “industrial server” made of MicroTCA building blocks (& something else)	Herbert Erd (N.A.T)
9:45-10:00	Smart Infrastructure Around MTCA Crates	Udo Weiss (nVent)
10:00 -10:15	VITA 93 QMC - Expanding Modularity and Performance: Unlocking New Potential for MTCA Platforms	Tim Tews (Tews)
10:15-10:30	Discussion	
10:30-11:00	Coffee break	

Session 4 (11:00 -12:30) Chair: Dariusz Makowski (Lodz University of Technology)

Time	Title	Speaker
11:00-11:15	Experimental point-to-multipoint distribution of WR-Based clock and PPS signals through µTCA Backplane	Juan Fernández, Javier Benavides Caro (Safran)
11:15-11:30	DAMC-X3TIMER: Status Update on Hardware, Firmware, and Timing Infrastructure for PETRA IV	Hendrik Lippek (DESY)
11:30-11:45	Precision Timing & Advanced RF Solutions for Particle Accelerators	Jiaoni Bai (KVG)
11:45-12:00	NGCII Detector Controller synchronization using White Rabbit	Matthias Seidel (ESO)
12:00-12:15	Micro Hertz Temperature and Phase Stability of a LISA Phasemeter based on MicroTCA as ground-support equipment	Christian Darsow-Fromm (UniHH)
12:15-12:30	Discussion	
12:30-14:00	Lunch	

Session 5 (14:00-15:30) Chair: Timo Korhonen (European Spallation Source ERIC)

Time	Title	Speaker
14:00-14:15	First results of CW diagnostics for future accelerator	Olaf Hensler (DESY)
14:15-14:30	Custom data acquisition using FMCs and MicroTCA	René Geißler (GSI)
14:30-14:45	First Major Release of 'fwk'	Cagil Guemues (DESY)
14:45-15:00	Machine control and beam diagnostics prospects for the DALI project	Klaus Zenker (HZDR)
15:00-15:15	Progress of MTCA Platform and Applications in Large-scale scientific facilities	Hongrui Cao (ASIPP)
15:15 -15:30	Discussion	
15:30-16:00	Coffee break	

Session 6 (16:00 -17:45) Chair: Heiko Körte (N.A.T.)

Time	Title	Speaker
16:00-16:15	Integration of prototyping and cost-effective XILINX-AMD SoC/FPGA platforms in the DESY Firmware Framework	Alejandro Piñas (Uni Madrid)
16:15-16:30	Flashless, Network-Based Booting of MicroTCA AMCs	Patrick Huesmann (DESY)
16:30 -16:45	Actually utilizing the standardization – Applying (C)OTS software for monitoring and controlling MTCA installations	Simon Fischer (MPI-IPP)
16:45-17:00	AMD Versal ACAP Devices for low latency and high compute applications	Jens Michaelsen (Avent)
17:00-17:15	ESS Linux: Yocto based linux on MicroTCA CPUs	Gabriel Fedel (ESS)
17:15-17:30	MicroTCA Development for PIP-II Beam Instrumentation at Fermilab	Robert Turner White (FNAL)
17:30-17:45	Discussion	
19:30-22:30	Dinner	

Thursday, December 4, 2025

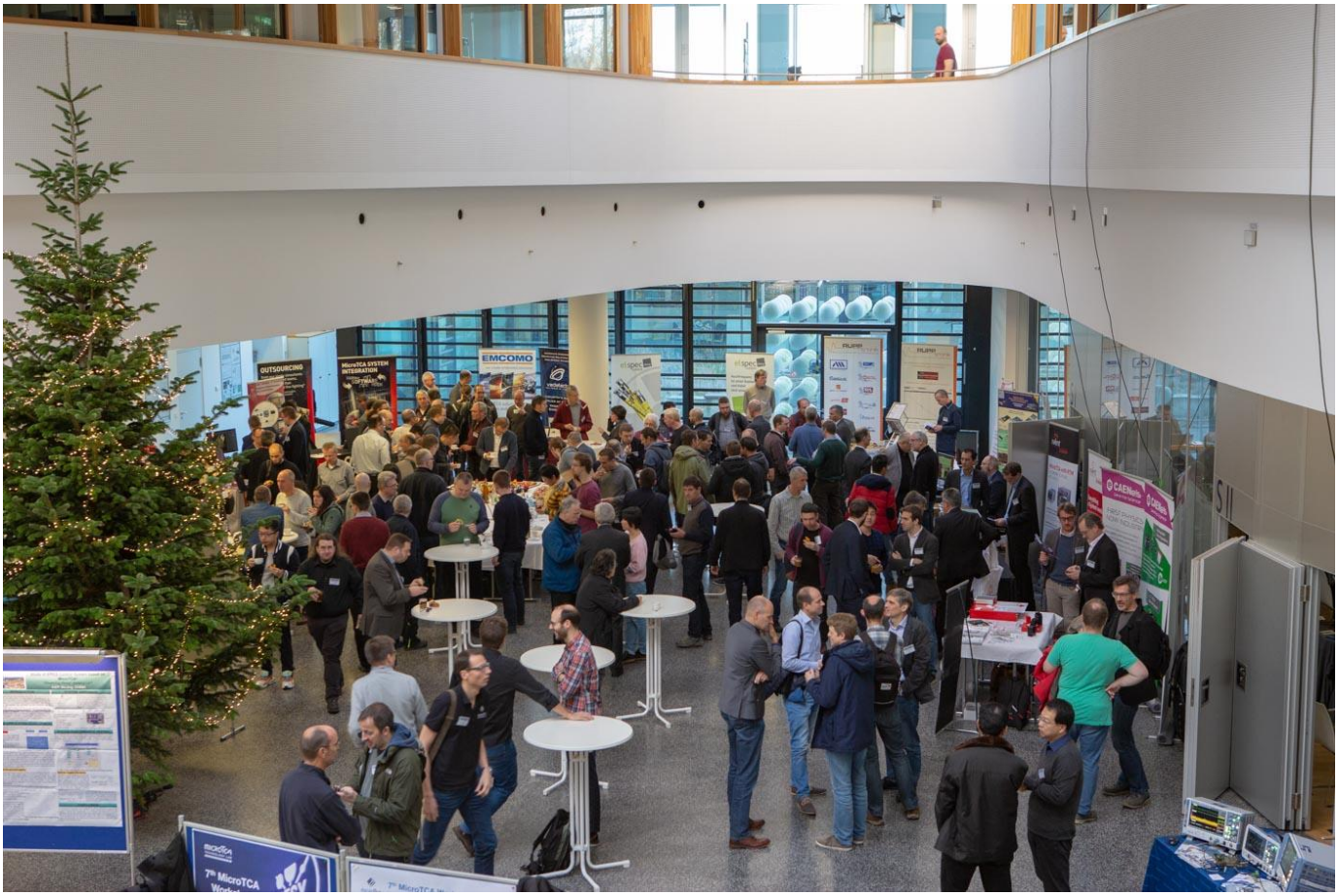
Session 7 (9:00 -10:30) Chair: Axel Winter (IPP)

Time	Title	Speaker
9:00-9:15	Summary of the 2025 MicroTCA workshop in China	Junqiang Zhang (CQU)
9:15-9:30	Update on the development and deployment of the MicroTCA based detector controller, NGCII	Mathias Richerzhagen (ESO)
9:30-9:45	The DAMC-DS5014DR: A High-Speed, High-Performance RFSoC-Based Digitizer Utilizing AMD Zynq UltraScale+ Technology in a MicroTCA.4 Form Factor for Diverse Scientific Applications	Behzad Boghrati (DESY)
9:45-10:00	2025 Status Report — MYRRHA/MINERVA LLRF System	Andrea Bellandi (SCK CEN)
10:00-10:15	Status Update on the Open-Source Synchronous Multi-Axis Motion Controller Solution for Large-Scale Experimental Physics Projects	Michael Randall (DESY)
10:15-10:30	Discussion	
10:30-11:00	Coffee break	

Session 8 (11:00 -12:30) Chair: Alan Justice (ORNL)

Time	Title	Speaker
11:00-11:15	Advancing Optical Interlock System with Custom MicroTCA RTM Solution for MYRRHA	Krisztian Ferencz (SCK CEN)
11:15-11:30	High channel count Simultaneous Analog IO to MTCA.4	John McLean (D-TACQ Solutions Ltd)
11:30-11:45	Bringing an AMC into operation with ChimeraTK	Martin Killenberg (DESY)
11:45-12:00	MicroTCA for photon beamlines - on-the-fly scans with spec	Martin Tolkiehn (DESY)
12:00-12:30	Discussion	
12:30-12:45	Closeout	Holger Schlarb (DESY)

Industrial Exhibition



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Session 1

Deployment and Development of MicroTCA at ESS

Faye Chicken

European Spallation Source ERIC

At the European Spallation Source, a range of control systems have been deployed using MicroTCA and PLCs. MicroTCA has become the standard platform for the fast controls needed to operate various sub-systems, such as LLRF, Machine Protection Systems, Timing Distribution and Beam Instrumentation applications.

The talk will give an overview of the current status of MicroTCA at ESS and upcoming new projects.

Status of MicroTCA at the Spallation Neutron Source

Thomas Justice, Brad Webb, Brian Shepetofsky, Kay Kasemir, Marnelli Martinez, Miljko Bobrek

Oak Ridge National Laboratory - Spallation Neutron Source

As part of a modernization initiative, the Spallation Neutron Source (SNS) has adopted MicroTCA technology to replace legacy systems, primarily those based on VME architecture. Currently, more than 60 MicroTCA systems are in production, supporting a range of applications including the Machine Protection System (MPS), Low-Level RF (LLRF), Pulsed Magnet Power Supplies, and the Personnel Protection System (PPS).

Building on the success of these deployments, SNS aims to perform one to two major system upgrades annually. Ongoing upgrades include the High Power RF (HPRF) systems, Extraction Kicker Power Supplies, the Timing Master and additional LLRF components.

In parallel, SNS and Oak Ridge National Laboratory (ORNL) are actively promoting wider adoption of MicroTCA technology across the North American accelerator community. This outreach is being carried out primarily through the Experimental Physics and Industrial Control System (EPICS) collaboration meetings, where SNS personnel lead workshops and introductory tutorials on MicroTCA integration and best practices.

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Summary of MicroTCA Workshop in Japan 2025 and Status of MicroTCA at J-PARC in 2025

Fumihiko Tamura

J-PARC Center, Japan Atomic Energy Agency

The MicroTCA workshop in Japan 2025 (MTCAWS in Japan 2025) was held from August 27 to 29 at KEK in person, while the last Japanese workshop in 2021 was held in a virtual format under COVID-19 conditions. The goal of this workshop is to boost the application of MicroTCA in Japan by exchanging the information and experiences. We welcomed the lecturer from DESY, who gave us a tutorial lecture on FPGA programming for MicroTCA platforms. We had a keynote talk and 16 orals. The workshop was very successful with 70 registered participants. The summary of the workshop and outlook are presented. The LLRF systems based on MTCA.4 in Japan Proton Accelerator Research Complex (J-PARC) are working stably and reliably. They support the stable beam delivery from RCS and MR to the experiments at very high beam power. Recently, we achieved the design output beam power of RCS and MR. There are new MTCA applications projects at J-PARC. The status and future plans of the MTCA applications at J-PARC are presented.

RF Beam Noise Feedback System for the High-Luminosity LHC Crab Cavities

Dimitar Hristov Marinov, Ben Woolley, Daniel Valuch

CERN

The High-Luminosity Large Hadron Collider (HL-LHC) project at CERN is set to introduce a series of major upgrades across the LHC complex, including the implementation of crab cavities, applied for the first time in a hadron machine. These cavities are designed to increase beam luminosity by compensating for the geometric luminosity reduction caused by the crossing angle at the interaction points.

However, the crab cavity controller and RF power stage introduce additional phase noise into the system, which can lead to beam emittance growth if not properly mitigated. A new solution, known as the beam noise feedback system, is therefore being developed to suppress the impact of this noise.

This presentation will outline the main challenges of the project and introduce a potential mitigation strategy based on AMD RFSoC technology.

Session 2

New FPGA, CPU and ADC/DAC products

Karl Judex

EMCOMO Solutions AG

Short introduction on EMCOMO Solutions and Vadatech, new AMC modules and MicroTCA crates, furher strategy on new FPGAs, CPUs and ADC/DACs.

Overview of DMCS Projects and MicroTCA.4 Developments

Dariusz Makowski

Lodz University of Technology

The Lodz University of Technology, Department of Microelectronics and Computer Science is involved in the development of MicroTCA.4, MicroTCA.4.1 and the future standards from 2007 onwards. Since that time, we have developed various MicroTCA.4 components including Intelligent Platform Management, Advanced Mezzanine Cards (AMCs), Rear Transition Modules (RTMs) for data acquisition and processing systems used in numerous accelerators and fusion projects.

The presentation discusses selected projects currently performed at our department based on the MicroTCA.4 technology.

Engineering Challenges in Scaling MicroTCA forHigh-Power Double Full-Size AMC Configurations

Christian Ganninger

nVent SCHROFF

Several companies engaged in the development and construction of quantum computers have adopted MicroTCA as the platform for their control systems, taking advantage of the proven architecture and ecosystem established within the MTCA.4 community. A significant number of these implementations utilize the Double Full-Size AMC form factor to provide increased front panel area and to enable the use of larger heat sinks for adequate thermal management.

The integration of up to twelve Double Full-Size AMCs, two MCHs, and a minimum of two Power Modules within a single MTCA crate introduces substantial mechanical, electrical, and thermal design challenges for crate manufacturers. This presentation discusses the current system-level constraints and outlines possible solutions, including new crate designs optimized for Double FullSize AMC configurations.

New building blocks and uplink solutions with the NAT-MCH

Heiko Körte

N.A.T. GmbH

The NAT-MCH is successfully serving MicroTCA applications and appliances around the world for more than 19 years now.

However, today's demands from the markets are very diverse as they do not only include request for simplified and easy-to-work-with solutions. The requirements also include fast and low-latency interconnects as well as increased connectivity to systems beyond the MicroTCA environment.

The current generation of MTCA.0 Rev 3 compliant MCHs from N.A.T. addresses these demands by a flexible combination of user-selectable building blocks for low-end and high-end switching and timing. The building blocks include switches for Ethernet and PCIexpress and timing based on IEEE1588/SyncE or GPS but also cover custom rquirements by its Protocol Agnostic Fabric (PAF) switch and programmable PLLs and clocking multiplexers.

The presentation will briefly introduce the building blocks before demonstrating how MicroTCA systems can be connected to the other MicroTCA and non-MicroTCA systems using low and highspeed system interconnects for Ethernet and PCIe.

The presentation by Herbert Erd on "An "industrial server"made of MicroTCA building blocks (& something else)"will then demonstrate the use of these system interconnects in real applications.

Vadatech: Accelerating Your Development (DAQ ToolSuite)

Alex Annis

VadaTech Ltd

Introduction to Vadatech DAQ Toolsuite, new DAQ software services available to accelerate your development cycle using Vadatech FPGA and FMC's.

Libera Brilliance X: MTCA.4 Readout Electronics for Electron Synchrotrons

Peter Paglovec

Instrumentation Technologies

Within the PETRA IV project at DESY, a new high-resolution Beam Position Monitor (BPM) system based on MicroTCA.4 technology is being developed to meet the stringent requirements of the low-emittance lattice. Building on the successful prototype phase, the system has now been introduced under the commercial name Libera Brilliance X, a new member of Instrumentation Technologies' Libera family. The name emphasizes continuity with the widely adopted Libera Brilliance+, while extending the concept into the modular MicroTCA.4 platform.

The Libera Brilliance X system relies on two key application modules developed for the PETRA IV project: the DAMC-UNIZUP AMC card, designed at DESY and licensed by Instrumentation Technologies, and the Libera 2BPMRTM front-end and digitizer, developed at Instrumentation Technologies. Leveraging the modularity of the platform, these boards can be integrated into various chassis, including compact form factors suitable for laboratory and test-bench applications.

In this contribution, we present the current development status and the first test results obtained with the instrument in the laboratory and at Brookhaven National Laboratory on the NSLS-II machine.

Session 3

Keynote: Systematic Approaches for Accelerator Controls

Paul Chu

Nanjing University

Modern accelerator-based user facilities are taking advantage of recent artificial intelligence (AI) boom. Regardless a newly planned facility or an existing one, all should implement a well-suited control system to support advanced tasks with AI technologies. This talk illustrates an architecture design to cover as much possible future application supports at reasonable cost. The talk will first give background introduction for AI and potential issues. A realistic design with possible applications utilizing latest technologies is presented. Additionally, a complete data infrastructure for supporting applications is also shown.

An “industrial server” made of MicroTCA building blocks (& something else)

Herbert Erd

N.A.T GmbH

The demands from the markets these days are very diverse as they do not only include request for simplified solutions but also clear requirements for new interconnect and interface options, high precision timing and flexible processing power.

Using MicroTCA building blocks such as MTCA.0 rev3 compliant components and existing as well as new 1U 19” enclosures, N.A.T. has developed a new server type family of products. These solutions can be considered as a true industrial server with AMC/RTM extension slots on the one hand, but as a ready-to-deploy MicroTCA.4 system on the other hand.

The new architecture can be a door opener for AMCs to enter markets still being dominated by other formfactors. By the features embedded into the solution, system designers can benefit from the value of MicroTCA for high-end, reliable systems.

Another part of this new MicroTCA system concept is a new system-level approach to AMC design and testing which at the same time delivers the world’s first full-featured one-slot MicroTCA system.

For the first time an AMC designer can develop, test and deploy an AMC completely separated from any MicroTCA infrastructure. The solution eases the AMC design process as it significantly reduces the must-have knowledge requirement on MicroTCA and thus allows hardware and software developers to focus on the AMC design.

This presentation will high-light the system architectures with all default and application specific options. A live demonstration will also be available.

Smart Infrastructure around MicroTCA Crates

Udo Weiss

nVent SCHROFF

Increasing power dissipation and computational demands have made the supporting infrastructure of MicroTCA systems a key factor for reliable and efficient operation. System architects must address challenges in thermal management, power distribution, monitoring, and electromagnetic compatibility (EMC) to maintain stable performance. A controlled thermal environment— achieved through air-to-water heat exchangers—is essential for ensuring the long-term integrity of sensitive electronics. Intelligent power distribution units (IPDUs) further enhance reliability by enabling remote sensor monitoring, fault detection, and targeted power cycling when required. In addition, robust EMC shielding of the enclosures that host the MTCA crates is critical to minimizing interference and preserving signal integrity in high-density environments. This presentation explores how integrating such smart infrastructure components around MicroTCA crates enhances operational stability, supports predictive maintenance, and enables scalable, future-proof system designs.

VITA 93 QMC - Expanding Modularity and Performance: Unlocking New Potential for MTCA Platforms

Tim Tews, Jan Zimmermann

TEWS Technologies GmbH

The recently ratified VITA 93 QMC standard introduces an unprecedented level of modularity, flexibility, and scalability. Building on lessons learned from previous standards, QMC blends their proven strengths with new capabilities designed for the future. This presentation provides an overview of the key features and advantages of the QMC standard, including support for next-generation interfaces such as PCIe Gen6 and the possibility to integrate the latest FPGA technologies. Furthermore, it explores how MicroTCA can serve as an ideal platform for QMC integration, highlighting the concept of a QMC carrier for MTCA.4 that combines the flexibility of QMC with the reliability, management, and ecosystem maturity of the MicroTCA architecture.

Session 4

Experimental point-to-multipoint distribution of WR-Based clock and PPS signals through MicroTCA Backplane

Juan Fernández, Javier Benavides Caro, Adrián Martínez Múnera, Antonio Miguel López Antequera, Gabriel Ramírez Escalona, Pilar Gil Jaldo

Safran Electronic & Defense Spain

This work presents an experimental implementation of a clock and PPS distribution system using the MicroTCA backplane to achieve synchronized operation of multiple AMC modules. The point-to-multipoint lines of the backplane allow a single master AMC, connected to a White Rabbit (WR) network link, to share its reference clock and PPS signals with all slave AMCs in the chassis. This enables the generation of synchronous signals across all modules using only one fiber connection to the WR network, simplifying the hardware and improving scalability.

The study was carried out within the framework of a WR-based trigger generation system, demonstrating that the number of synchronized triggers can be increased without adding new WR links. Jitter measurements of both the clock and trigger signals at the master and slave AMCs confirmed excellent timing stability and negligible degradation, validating the feasibility of this approach for deterministic, high-precision synchronization in complex distributed control systems.

DAMC-X3TIMER: Status Update on Hardware, Firmware, and Timing Infrastructure for PETRA IV

Hendrik Lippek

DESY

The DAMC-X3TIMER, a dedicated MTCA.4 AMC module, serves as the central component of the Timing and RF-Distribution System for the PETRA IV accelerator. Initial hardware prototypes have been produced, with the next revision now in production.

This presentation outlines the planned timing system infrastructure, emphasizing the DAMCX3TIMER's role in the PETRA IV accelerator complex. It also covers key insights from the hardware bring-up phase, including technical challenges and solutions, as well as the current firmware development status and its integration with the hardware.

Precision Timing & Advanced RF Solutions for Particle Accelerators

Jiaoni Bai

KVG Quartz Crystal Technology GmbH

KVG Quartz Crystal Technology GmbH is a professional frequency control products manufacturer, focusing on research, development, production and sales. High-end crystal oscillators are our specialty. We cooperate with DESY for the production and test of the Master Oscillator (MO) module, the Local Oscillator Generation (DeRTM-LOG) module and X-Band middleware. The MO provides 1.3 GHz reference for modern accelerators with excellent phase noise, sub-fs jitter and high-power output. The DeRTM-LOG module is a critical component in LLRF systems generating local oscillator, RF reference and clock signals for the MicroTCA.4 standard. Currently the DeRTM-LOG 1.3GHz and 1.5GHz are available. X-Band middleware, including X-band Local Oscillator Generation Module (XLOGM) and X-band Downconverter Module and Upconverter (XDWCM_UPC), are employed to convert between the S-band 3 GHz and X-band 12 GHz frequencies.

NGCII Detector Controller synchronization using White Rabbit

Matthias Seidel, Alexander Rüde, Mathias Richerzhagen

European Southern Observatory (ESO)

Accurate synchronization between detector controllers is important for low-noise readout in focal-plane arrays used for astronomical observations. ESO's MicroTCA based detector controller (NGCII) uses White Rabbit to enable sub-nanosecond timing and timestamp distribution in a PTP environment. This allows us to accurately synchronize the main sequencer clock from which all detector control signal timing is derived. In this presentation, we describe the method used to integrate White Rabbit into the NGCII architecture and show first lab results.

Micro Hertz Temperature and Phase Stability of a LISA Phasemeter based on MicroTCA as ground-support equipment

Christian Darsow-Fromm[1], Arnold Walker[1], Johannes Zink[2], Gianmarco Ricci[2], Holger Schlarb[2], Oliver Gerberding[1]

Uni Hamburg Institut fuer Experimentalphysik[1], DESY[2]

The University of Hamburg, in collaboration with DESY, is developing an electrical ground-support equipment phasemeter, or phasemeter simulator, based on the MicroTCA.4.1 standard, for the space-based gravitational-wave detector LISA, funded by the German Aerospace Agency (DLR).

The main task of the phasemeter is to extract the phase of various laser interferometer beat note signals with microcycle precision at frequencies between 0.1 mHz and 1 Hz, with a phase stability requirement of 6 µrad/√Hz. Additional functions include the readout and generation of ranging and data communication sidebands, frequency control of the lasers, and signal acquisition. The development is conducted in parallel to, and in collaboration with, the development of the flight hardware phasemeter. The simulator will be made available to the partners within the LISA consortium for the assembly, integration, verification, and testing (AIVT) phase of the mission and for the technology development of payload items.

We present the system design, the phasemeter software for controlling and data acquisition, temperature and phase stability measurements of our custom ADC, and the status of our hardware development.

Session 5

First results of CW diagnostics for future accelerator

Olaf Hensler, Timmy-Jan Lensch

DESY

Continuous Wave (CW) mode is becoming increasingly relevant for FELs, in contrast to a pulsed operation mode as it is currently done at the EuXFEL accelerator. This transition requires a new approach to timing and data readout concepts. One potential solution involves using double-buffered memory in the firmware, with buffer swapping controlled by a timing system trigger. Initial developments using this approach have been carried out with a laser pulse energy measurement setup at the KALDERA facility at DESY.

The implementation is based on Struck SIS8300-KU ADC hardware, the DESY Firmware Framework, and ChimeraTK software. Integration with the DOOCS control system via the DOOCSDeviceAccess library will be presented.

Custom data acquisition using FMCs and MicroTCA

René Geißler

GSI

GSI is a particle physics research institute located in Darmstadt, Germany. At the same location, a new accelerator facility called FAIR (Facility for Antiproton and Ion Research) is currently under construction.

Our beam instrumentation department is using MicroTCA systems for measuring beam parameters like position, intensity and profile, for accurate timing control, for measuring voltages and for control applications.

The focus of the presentation will lie on the different FPGA Mezzanine Cards (FMCs) (Open Hardware, commercial and self-developed), that we use together with AMC FMC carriers in our custom data acquisition and control systems.

First Major Release of ’fwk’

Cagil Guemues

DESY

Managing large-scale, long-lifecycle FPGA projects at scientific facilities demands a framework that is both flexible and stable. To meet this challenge, the MSK group at DESY has developed ‘fwk’, an open-source FPGA framework. While its initial implementation dates back to before 2015, ‘fwk’ has since evolved into a collaborative tool used by various scientific national labs and companies across Europe.

‘fwk’ provides a stable, EDA-tool-agnostic abstraction layer, enabling the seamless integration of IP modules. It can generate, implement, and perform verification targeting SoC FPGAs, including Yocto support.

This presentation will highlight the framework’s key features, recent progress, and the significant milestone of the 1.0 release for the open-source scientific community.

Machine control and beam diagnostics prospects for the DALI project

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The Dresden Advanced Light Infrastructure (DALI) going to be build at HZDR is a accelerator driven light source. It combines intense THz radiation, infrared beams, positrons and ultra-fast electron diffraction to a unique source for cutting-edge science.

In this presentation, the DALI machine concept will be introduced. It is used to derive requirements for the machine control and beam diagnostics. Special emphasis is given to MicroTCA based subsystems and how we plan to integrate existing solutions. In that regard, different aspects related to MicroTCA based systems, like software, firmware and board selection, will be discussed.

Progress of MicroTCA Platform and Applications in Large-scale scientific facilities

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As an open-standard-compliant carrier platform, the Micro Telecommunications Computing Architecture (MTCA) chassis plays a key role in high-end computing and communication systems, and serves as a critical foundation for the technological upgrading of large-scale scientific facilities. In terms of platform development, the complete MTCA chassis components conforming to the MTCA.4 specification have achieved independent R&D and mass production. Constructed from high-strength aluminum alloy, the chassis is compatible with 19-inch standard racks and supports both 2U (6-slot) and 10U (12-slot) configurations to adapt to different scenarios. The chassis backplane, combined with a self-developed MCH, supports a differential data rate of 10.3125 Gbps, enabling a high-speed data exchange center. Together with the Hygon CPU, it realizes local/remote communication between AMC modules and processors, ensuring full domestic compatibility. Internally, a 2000W secondary power conversion module, a Power Management module and a domestic chip-based management module work together to ensure stable operation. Meanwhile, a high-performance Advanced Integrated Mezzanine Carrier (AIMC) board, centered on a Zynq processor and supporting scalable deployment and AI model integration, has also been developed synchronously as a supporting component of the platform.

In the aspect of application in large-scale scientific facilities, a high-speed digital Data Acquisition and Processing (DAQP) system has been developed based on the MTCA architecture. This system integrates a real-time pulse signal processing algorithm developed via FPGA technology, and has been successfully applied to neutron energy spectrum measurement in the EAST experiment, achieving a data transmission rate of 1.6 GB/s. This application not only validates the reliability and high performance of the domestically produced MTCA platform, but also provides effective technical solutions for nuclear fusion diagnostic and control system design, as well as high-precision data acquisition and processing in other large scientific facilities.

Keywords: MTCA.4; MCH; AMC; Nuclear Fusion; NES Neutron Energy Spectrum System

Session 6

Integration of prototyping and cost-effective XILINX-AMD SoC/FPGA platforms in the DESY Firmware Framework

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Developing SoC and FPGA-based applications for MicroTCA AMC involves significant hardware costs. It requires a complete hardware ecosystem with a Chassis, an MCH, and one or several AMCs, presenting a steep learning curve for new developers.

This contribution presents the integration of two different cost-effective boards into DESY's FPGA Firmware Framework (FWK). The goal is to provide a low-cost, and accessible platform that facilitates rapid application development and serves as an effective gateway to the framework.

The first integrated board is the AMD/Xilinx Kria KR260 Robotics Starter Kit, a powerful platform based on the Zynq UltraScale+ SoC with a rich variety of I/O elements.

The second board is the TEWS Technologies TMPE627, a compact mini-PCIe card hosted on a desktop computer. Based on an AMD/Xilinx Artix 7, it provides 4-channel AD/DA converters and 14 digital I/O lines.

The contribution focuses on the development cycle used and the implementation of different solutions.

This work was supported by Grant PID2022-137680OB-C33 funded by MCIN/AEI/ 10.13039/501100011033 and by "ERDF A way of making Europe"

Flashless, Network-Based Booting of MicroTCA AMCs

Patrick Huesmann, Michael Fenner

DESY

In particle accelerator facilities, on-board flash memory is exposed to radiation that can cause bit corruption over time, making it preferable to load applications over the network rather than store them locally. This talk presents a method for flashless, network-based booting of MicroTCA Advanced Mezzanine Cards (AMCs) using U-Boot and standard network protocols. By loading the entire application stack - including the kernel, device tree, root filesystem, and FPGA bitstream - over NFS or TFTP, systems can achieve stateless operation and simplified fleet management.

The talk will outline key implementation details, including MicroTCA backplane Ethernet quirks, required U-Boot patches, and NFS server adjustments.

Finally, integration with MMC mailbox data can enable boards to request configuration-specific software automatically. This allows an entire fleet of AMCs to boot from a single, generic setup - streamlining maintenance and making system management more robust and scalable.

Actually utilizing the standardization –Applying (C)OTS software for monitoring and controlling MicroTCA installations

Simon Fischer[1], E. Lovrič[2], J. Klavžer[2], M. Železnik[2]

Max Planck Institute for Plasma Physics[1], Cosylab[2]

This talk gives an overview of the first steps into using the widely used IT infrastructure monitoring application Zabbix to remotely monitor and even maintain/control larger installations of MicroTCA (and PC/server) based hardware. The goal of this project is to utilize the standardized IPMI interface of the MicroTCA products in combination with the open source Zabbix software to build dashboards as well as detailed views of the health status of W7-X overall DAQ systems consisting of many MicroTCA chassis, AMCs, CPUs and also including PCs/servers and other DAQ hardware –without specific coding or hard to maintain, homegrown scripts & applications.

AMD Versal ACAP Devices for low latency and high compute applications

Jens Michaelsen

Avnet Silica

The modern system on chip that can support your project via:

- integrated ADC and DAC for control and data acquisition
- array of massive compute DSP engines
- high speed data links and network on chip

ESS Linux: Yocto based linux on MicroTCA CPUs

Gabriel Fedel

European Spallation Source

The European Spallation Source will be the most powerful accelerator-based neutron source, and the standard chosen for the ESS Linear accelerator fast data acquisition systems is MicroTCA. The ESS accelerator has a big set of different MicroTCA based systems: Machine Protection, Low Level RF, Beam Diagnostics, Motion systems based on Ethercat and more. Besides that, different models of CPUs are in use on ESS MicroTCAs : Concurrent AMC90x and AMG6x (x86) and IOxOS IFC1410 (PowerPC).

To access the most of our CPUs and support all requirements from the different applications we choose to use Yocto as the base of our OS: the ESS Linux. Even though the OS name may not be the most original, the performance and improvements we achieve with ESS Linux are quite remarkable.

On this presentation we will go through the basics of Yocto and ESS Linux, the challenges, our migration process from CentOS 7, biggest achievements and future plans.

MicroTCA Development for PIP-II Beam Instrumentation at Fermilab

Robert Turner White

FNAL

Session 7

Summary of the 2025 MicroTCA workshop in China

Junqiang Zhang

Shanghai Advanced Research Institute,CAS

The “2025 MicroTCA/ATCA International Workshop for Large Scientific Facility Control”was held by Chongqing University (CQU), in Chongqing, China, on September 15-17 2025. The workshop was held on-site and online at the same time. More than 90 participants from 18 institutes and 13 companies joined the workshop. 41 talks were presented, which included hardware, firmware and applications in research facilities and industry, etc. The presentation will give a summary of the workshop and highlight some of the key presentations of the workshop.

Update on the development and deployment of the MicroTCA based detector controller, NGCII

Mathias Richerzhagen, Alexander Rüde, Matthias Seidel, Max Engelhardt

European Southern Observatory (ESO)

In the time since the last MicoTCA workshop we have achieved laboratory first-light with the final two detector families to be supported by our MicroTCA.4 based general detector controller, NGCII. Besides CCDs, the workhorse detector for ground-based astronomy, we have also brought up Geosnap, a fully digital detector transmitting its pixel data through high-speed digital signals.

Meanwhile, we are in the process of preparing CMOS detector systems for large scale deployment. We are developing test tooling for post-production testing, estimating the need for, and starting the procurement of spare parts, and are in the process of performing final environmental tests for CMOS detector specific systems.

The DAMC-DS5014DR: A High-Speed, High-Performance RFSoC-Based Digitizer Utilizing AMD Zynq UltraScale+ Technology in a MicroTCA.4 Form Factor for Diverse Scientific Applications

Behzad Boghrati, Cagil Guemues, Michael Fenner, Stanislav Chystiakov, Szymon Jablonski

DESY

This talk reviews the DESY MicroTCA card, DAMC-DS5014DR, designed for high-speed multichannel data acquisition and signal generators. Based on the AMD Zynq Ultrascale RFSoC ZU47DR, it features eight 14-bit, 5 GSPS ADCs, eight 14-bit, 8.92 GSPS DACs, extensive programmable logic (PL) resources, and an ARM-processing system (PS). In this AMC card, the AC or DC coupling options precondition the input signals and feed them to the ADCs, leaving enough room for the user to perform custom signal conditioning at the RTM side. The interface between DAMC-DS5014DR and RTM follows the MicroTCA.4 concept. The board offers a QSFP28+ interface that supports 100Gb Ethernet or optical PCIe Gen.4 x4 (16 Gbps/lane) data streaming, while the second set of PCIe Gen.4.0 x8 available on the card provides data transfer to the MicroTCA.4 backplane. Eight independent timing/trigger inputs can be used to capture event-coincident data.

To support highthroughput applications, the card incorporates three 16-GByte, 64-bit DDR4 memory banks, ideal for managing and processing fast data streams. A high-frequency clock synthesizer generates synchronized clocks for the ADCs, DACs, and PL, with inputs selectable from the backplane, front panel, or a local precision oscillator. The board is designed to be compatible with the CERN White Rabbit protocol, allowing receipt of White Rabbit trigger signals via the QSFP module. Supported by AMD's comprehensive toolchain (Vivado, HLS, Yocto, PetaLinux, SDSoC, SDAccel), the DAMCDS5014DR integrates a powerful FPGA, high-performance ADCs/DACs, and a capable CPU, delivering an advanced platform for high-speed digitization and real-time processing while minimizing development time.

2025 Status Report —MYRRHA/MINERVA LLRF System

Andrea Bellandi, Florian Frank, Wouter De Cock, Erik Verhagen, Jan Geerts, Koen Geerts

SCK-CEN

At SCK CEN in Belgium, the MYRRHA project aims to build the world's first Accelerator-Driven Subcritical reactor (ADS). The initial phase centers on implementing a 100MeV, 4mA CW superconducting linear proton accelerator –with the unique technical challenge: the maximum allowable beam trip duration is less than 3 seconds. The accelerating field stability requirement is ≤0.1% and ≤0.1 degrees to avoid excessive beam loss. The SRF cavities operate at a high loaded quality factor (QL=2.3e6) and close to the beam optimal value to minimize power consumption. The beam current can be modulated at 250Hz.

This contribution presents the past work and the strategy used to achieve the project's objectives. Recognizing DESY's world-leading expertise in building and operating LLRF systems, a collaboration was established to share particle accelerator-related firmware and software modules. Leveraging DESY's Framework (FWK) capability to integrate multiple board support packages (BSPs) within a single project, the team developed its LLRF system using the RealDigital RFSoC4x2 prototype board. This parallel development path allows for rapid prototyping while the MTCA.4 AMC design, the DAMC-DS5014DR, is finalized.

Status Update on the Open-Source Synchronous Multi-Axis Motion Controller Solution for Large-Scale Experimental Physics Projects

Michael Randall, Cagil Guemues, Jens Georg, Martin Killenberg, Martin Tolkiehn, Michael Fenner, Patrick Huesmann, Stanislav Chystiakov

DESY

Synchronous multi-axis motion control systems integrated with diagnostic and data acquisition subsystems are critical components in large experimental physics projects. To meet these specific requirements, DESY has developed an open-source motion control solution based on the DAMCMOTCTRL board. Designed for projects like PETRA IV, this system enables synchronized control of up to 48 stepper motors on a single AMC board, interfacing with established control systems such as DOOCS, EPICS, and TANGO, or through a direct ASCII interface.

Since last year's status update, significant progress has been achieved in the firmware development. The internal motor-control architecture has been redesigned around the CANopen CiA402 profile, which defines an industry-standard framework for motion control. As part of this redesign, closed-loop operation with incremental encoders has been added, along with other essential motion-control features. This standardization provided the basis for implementing the first native TANGO interface for the controller.

This presentation will provide an overview of the hardware and firmware architecture, introduce the latest features, and outline the roadmap for the MicroTCA-based motion controller.

Session 8

Advancing Optical Interlock System with Custom MicroTCA RTM Solution for MYRRHA

Krisztian Ferencz

SCK CEN

For the implementation of the first 100 MeV stage of the superconducting, high power proton linac for MYRRHA at SCK CEN (Belgium) an optical Interlock Rear Transition Module (RTM) and its companion daughterboard were developed to provide a modular, high-speed solution for optical signal transmission in MicroTCA-based control systems. Designed for reliability and low latency, the system ensures robust isolation and immunity to electrical noise in safety-critical applications.

A simplified Spartan-7 FPGA reference design complements the RTM, implementing key functionalities to interface primary system devices. This presentation outlines the architecture, design choices, and validation results of the RTM and reference design, emphasizing lessons learned from collaboration with DESY and potential extensions toward future accelerator system integration.

High channel count Simultaneous Analog IO to MTCA.4

John McLean

D-TACQ Solutions Ltd

The DESY DAMC-FMC1Z7IO is a cost-optimized IO controller and processing board in AMC formfactor with a front panel site for FMC modules. The module features a ZYNQ-7000 SOC that makes the AMC a networked computer node with extensive application capability.

Now manufactured under license by D-TACQ Solutions, DAMC-FMC1Z7IO also supports an MTCA.4 RTM with Z3 D1.0 signaling. This allows the AMC module to be used with the D-TACQ ACQ400-MTCA-RTM2, a two-site module carrier allowing access to a wide range of modules from D-TACQ Solutions. This combined with new and existing D-TACQ Simultaneous Analog and Digital I/O modules gives a powerful and flexible data acquisition solution.

Here we show some available configurations and real-world examples.

Bringing an AMC into operation with ChimeraTK

Martin Killenberg

DESY

Getting a new type of AMC up and running usually has a significant entry barrier.

Especially for unfamiliar boards it is important to have a reliable tool chain ready to have a smooth start. The ChimeraTK framework provides libraries and tools that cover the whole range from first communication and configuration of the board to full application development with integration to DOOCS, EPICS, TANGO or OPC UA based control systems. Even more advanced features like handshakes with AMD interrupt controllers have a ready to use implementation, particularly but not exclusively when using firmware provided by the DESY FPGA firmware framework (FWK). This significantly speeds up the whole device integration and application development process.

In this presentation we give an overview of ChimeraTK and report on recent improvements and new features.

MicroTCA for photon beamlines - on-the-fly scans with spec

Martin Tolkiehn

DESY

DESY is currently planning to upgrade the third generation synchrotron light source PETRA III to a state of the art diffraction limited storage ring. The new machine PETRA IV will make use of MTCA not only for the accelerator itself but also for the photon science experiments.

In my presentation I will show possible applications of MTCA for experiment control and data acquisition at photon beamlines. One of the most important applications is motion control and on-the-fly or continuous scanning.

I will present a very efficient implementation of on-the-fly scanning based solely on MicroTCA hardware and the well-known software package spec realized at beamline P24 at PETRA III.