Tutorial
MicroTCA Management

"How to become a MicroTCA expert – this year: within 25 minutes"

14th MicroTCA Workshop for Research and Industry

DESY, Hamburg

December 2nd – 4th, 2025

UNCLASSIFIED

Agenda

- About N.A.T.
- From ATCA to MTCA - two well-connected standards
- Why do we need management?
- What is behind the management?
- How does it work?
- What can you do?

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About N.A.T. – key facts

- Founded in 1990
- Privately owned and owner lead business
- Based in greater Cologne area in Germany (City of Bonn)
- Focus on innovation in communication
- Equipment for reliable operation with longevity commitment, including life-cycle management and upgrade/migration
  - comprehensive standard product line based on modular open standards
  - custom solutions designed to customer defined specification
- Quality „made in Germany“ since more than 35 years

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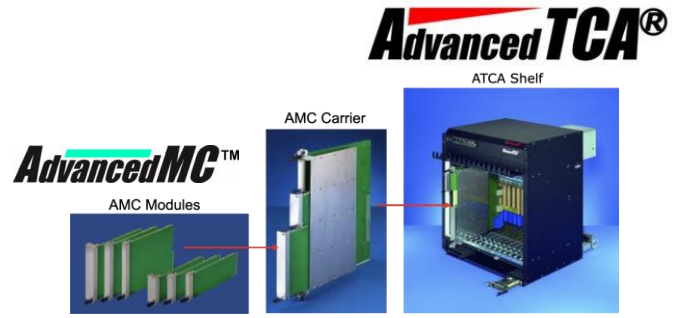
Where MicroTCA came from

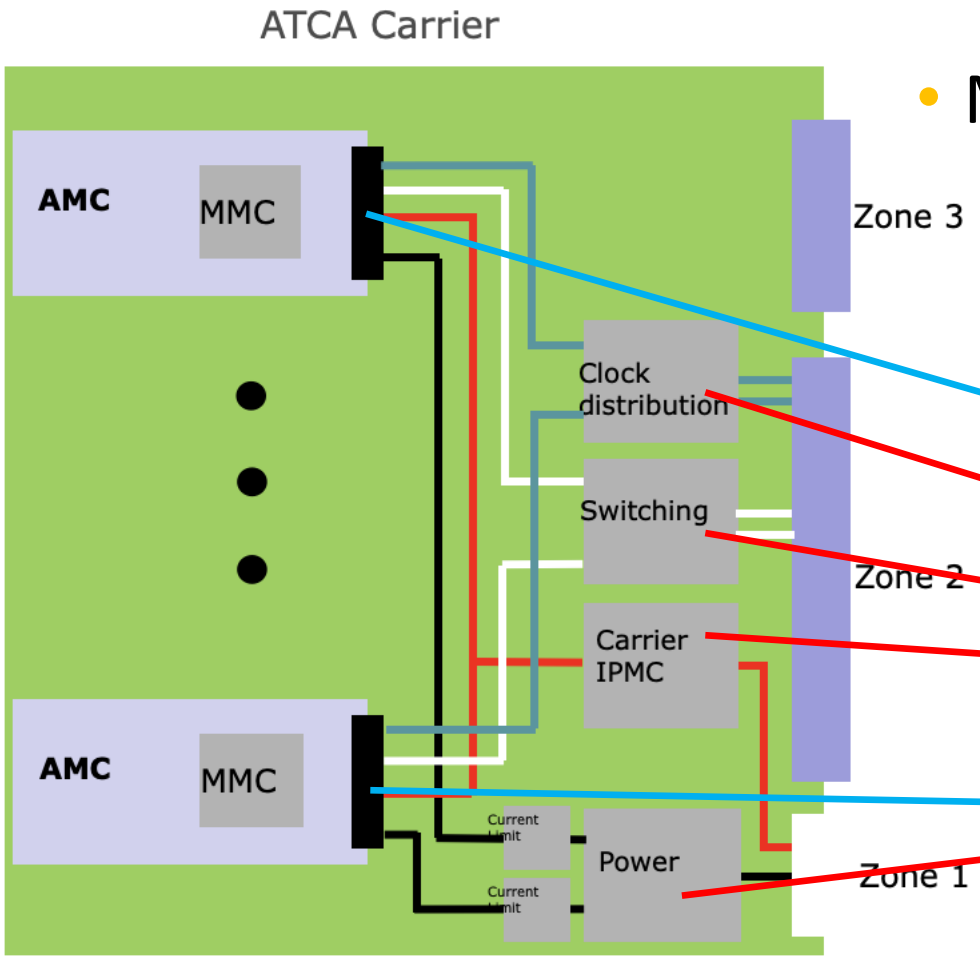
- 2002: **A**dvanced **T**elecom **C**omputing **A**rchitecture (ATCA)
  - Telecom carrier grade communication equipment
  - Switched MOSA using serial communication
  - New mezzanine standard: **A**dvanced **M**ezzanine **C**ard (AMC)



- 2006: **M**icro **T**elecom **C**omputing **A**rchitecture (MicroTCA, MTCA)
  - Derived from **A**dvance **T**elecom **C**omputing **A**rchitecture (ATCA)
    => common system management and re-use of Advanced Mezzanine Cards (AMCs)
  - Targeting at any telecom application ATCA would be an overkill for
  - Switched MOSA using serial communication

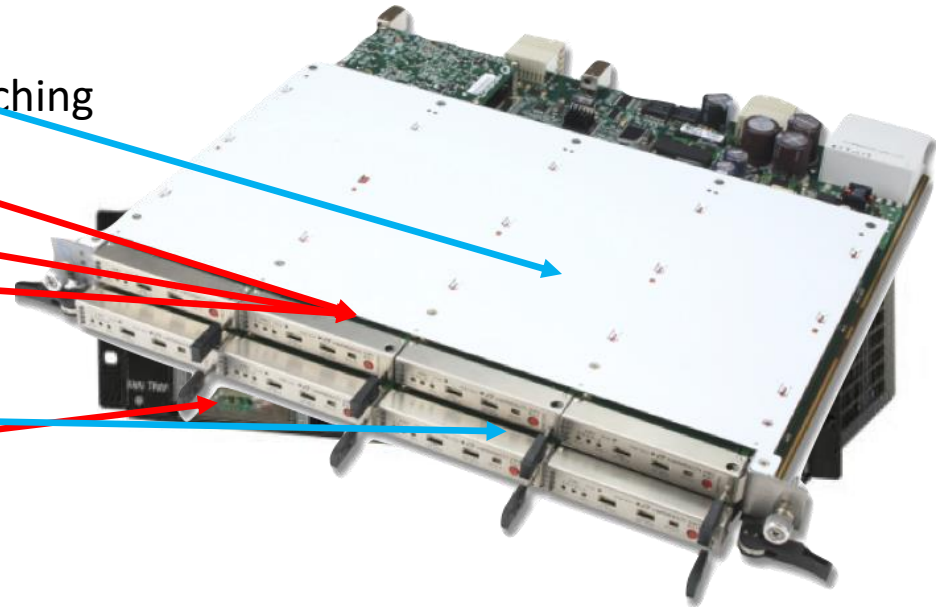
AdvancedTCA® ⟷ AdvancedMC™ ⟷ µTCA®

From ATCA to MicroTCA – creating the living environment for AMCs



- MTCA: AMC directly plugged into backplane

  => ATCA carrier is “virtualized” regarding
  - Power
  - Management
  - CLK,
  - Switching

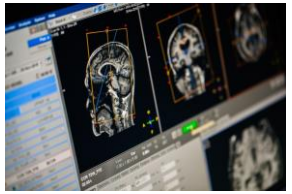


Where MicroTCA is being used today

- Today **M**icro**TCA** (MTCA) is being used in almost any vertical market:


Quantum Computer

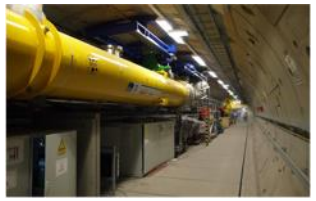

Vision and AI


Medical


(Tele-) Communication


Military


Traffic


Research


Industrial Control


Test & Measurement

???

… any many more ….

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Management Why do we need it?

- “Who” is in my system?
  - i.e. list of devices (aka “FRU” for **F**ield **R**eplaceable **U**nit)
- What capabilities does the FRU have?
  - i.e. active connections (AMCs) or RPMs (CUs)
- How healthy is my system?
  - i.e. sensors for current, voltage, temperature
  - i.e. events
- How can I talk to my FRUs?
  - i.e. manipulation of sensors
- How can I service my system?
  - i.e. hot-swap FRUs

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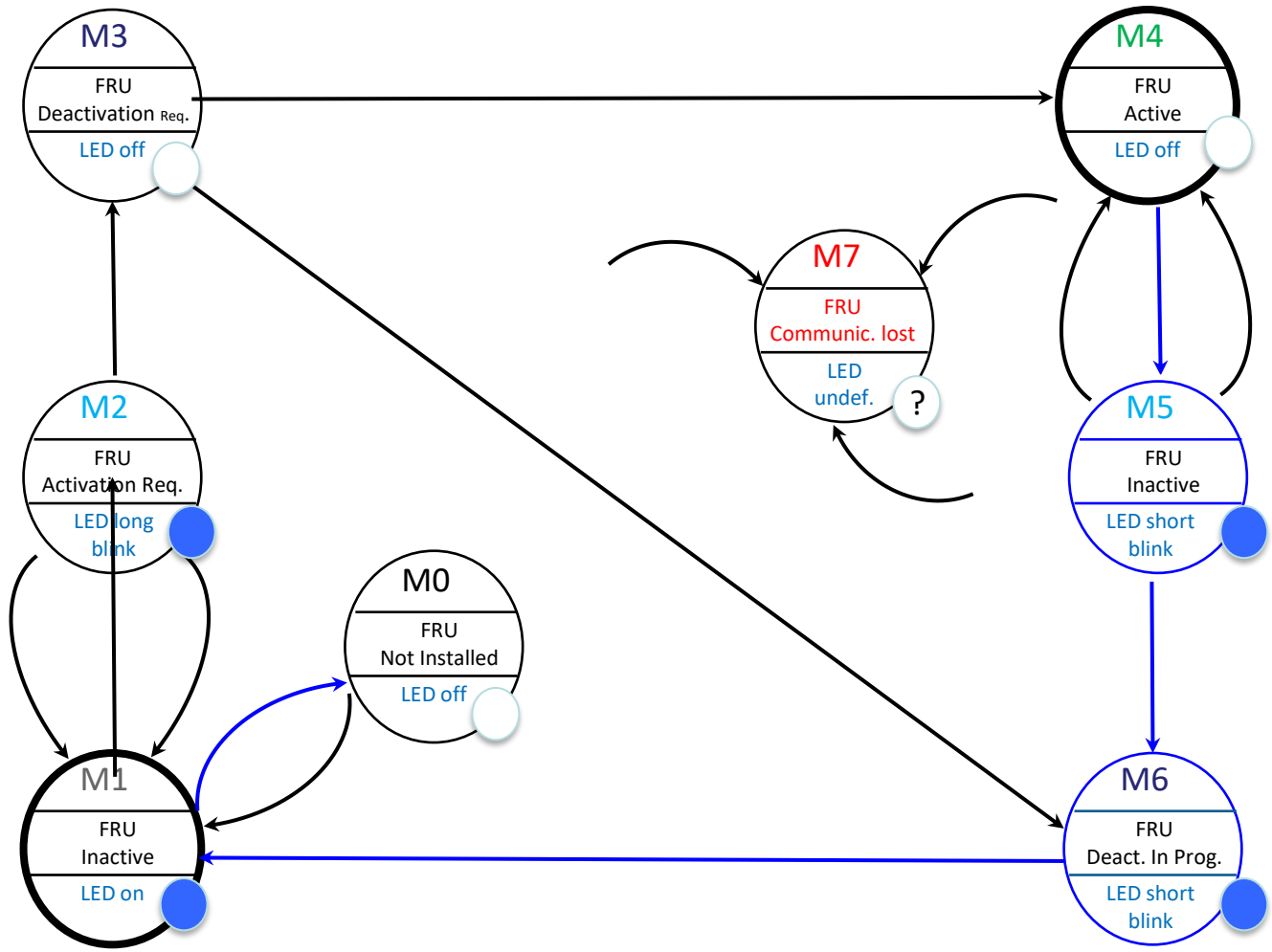
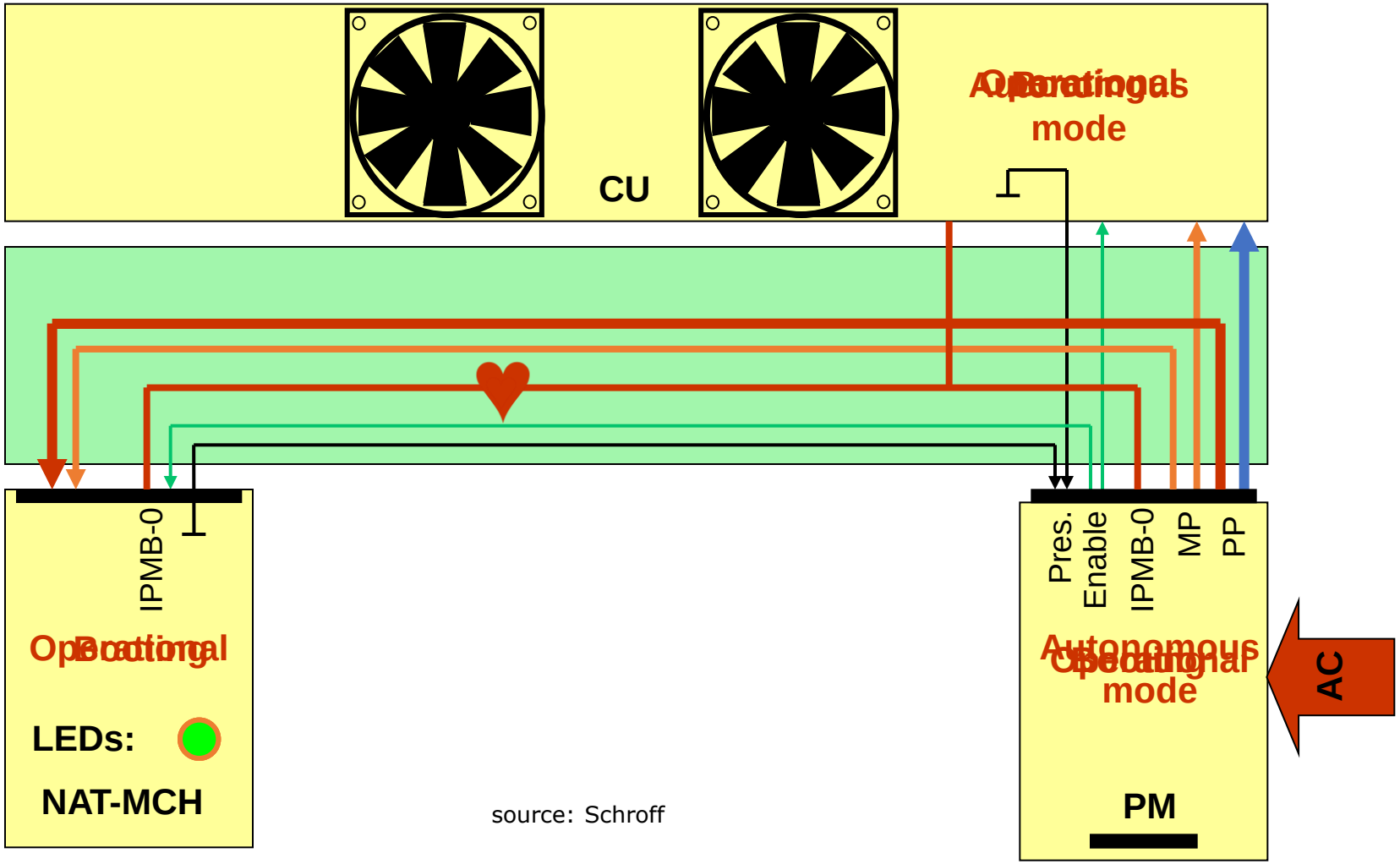
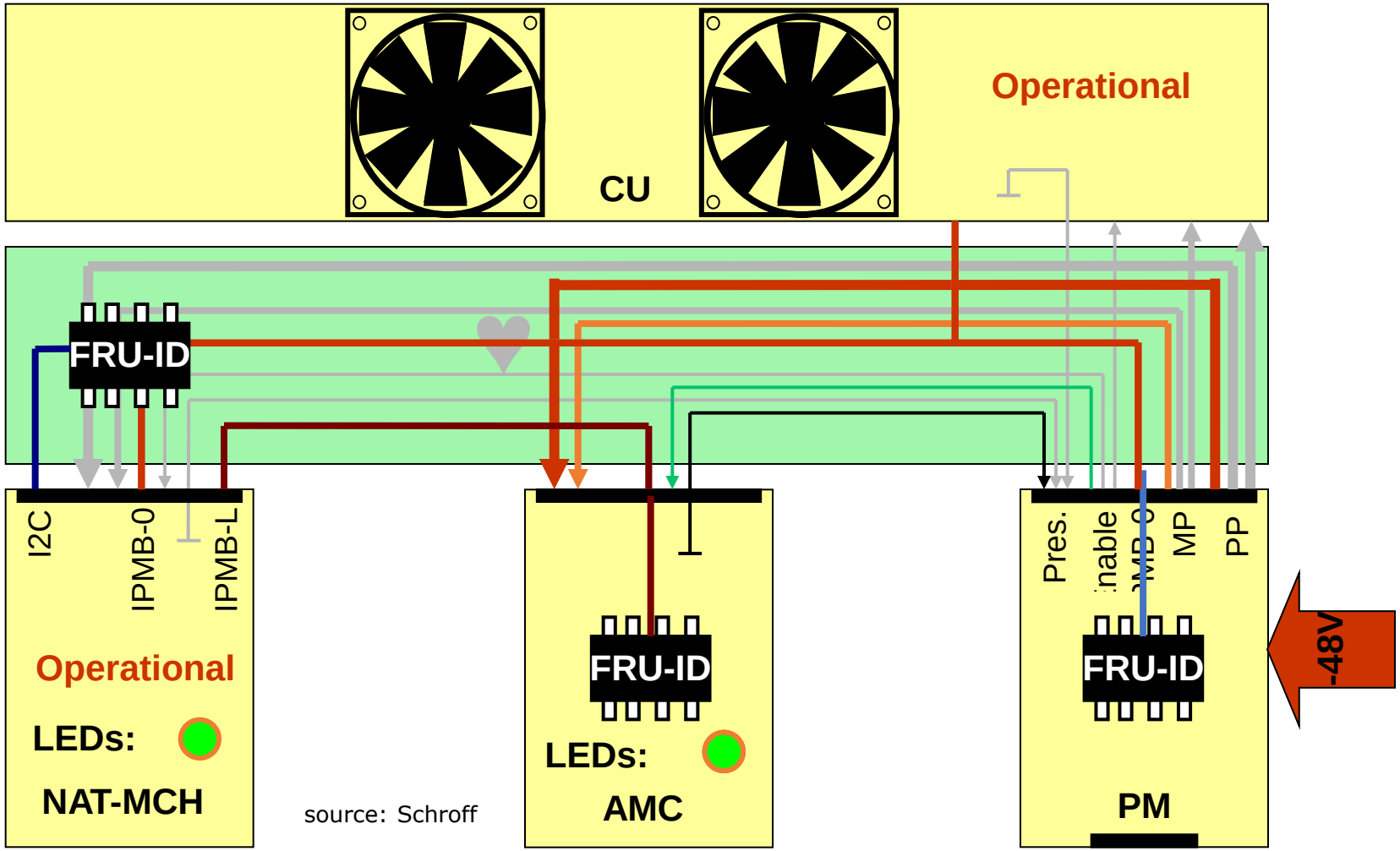
Management in MTCA FRU M states

- ATCA and AMC specs define FRU states, aka „M states“
  - Activation
    - FRU proceeds to state M4
  - Deactivation
    - FRU proceeds to state M1
  - Error (coms lost)
    - FRU moves to state M7
- MCH decides if and when module can reach M4
- MMC uses a state machine to control hot-plug/hot-swap





source: Schroff


Operational
CU
FRU-ID
I2C
IPMB-0
IPMB-L
Operational
LEDs:
NAT-MCH
source: Schroff
FRU-ID
LEDs:
AMC
Pres.
MP
PP
FRU-ID
-48V
PM

Useful CLI commands

NAT-MCH Gen3

- show_ekey
- show_fru
- show_fruinfo <fru_id>
- show_cu
- show_pm
- show_sensorinfo <fru_id>

NAT-MCH Gen4

- print ekey
- print fru
- print fruinfo <fru_id>
- print cu
- print pm
- print sensorinfo <fru_id>

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Management in xTCA What is behind

- Idea of management:
  - Hardware supervision by software (remote control and monitoring)
  - Intelligent handling of events and actions
  - Abstraction of hardware functionality
  - Operating system independent

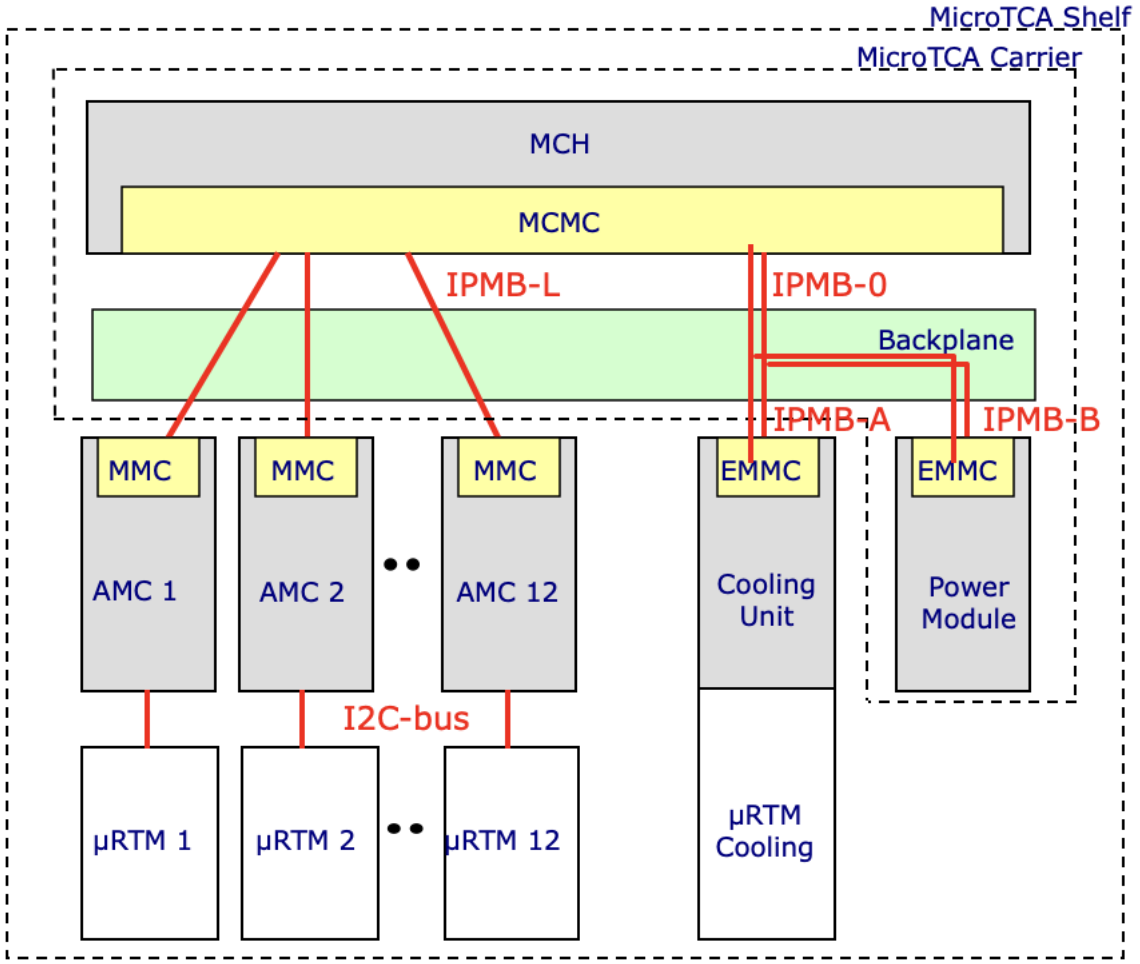
=> I^2C (**I**nter **I**ntegrated **C**ircuit): 2-wire, multi-master cabaple bus

=> IPMI (**I**ntelligent **P**latform **M**anagement **I**nterface) protocol

=> RMCP (**R**emote **M**anagement **C**ontrol **P**rotocol)

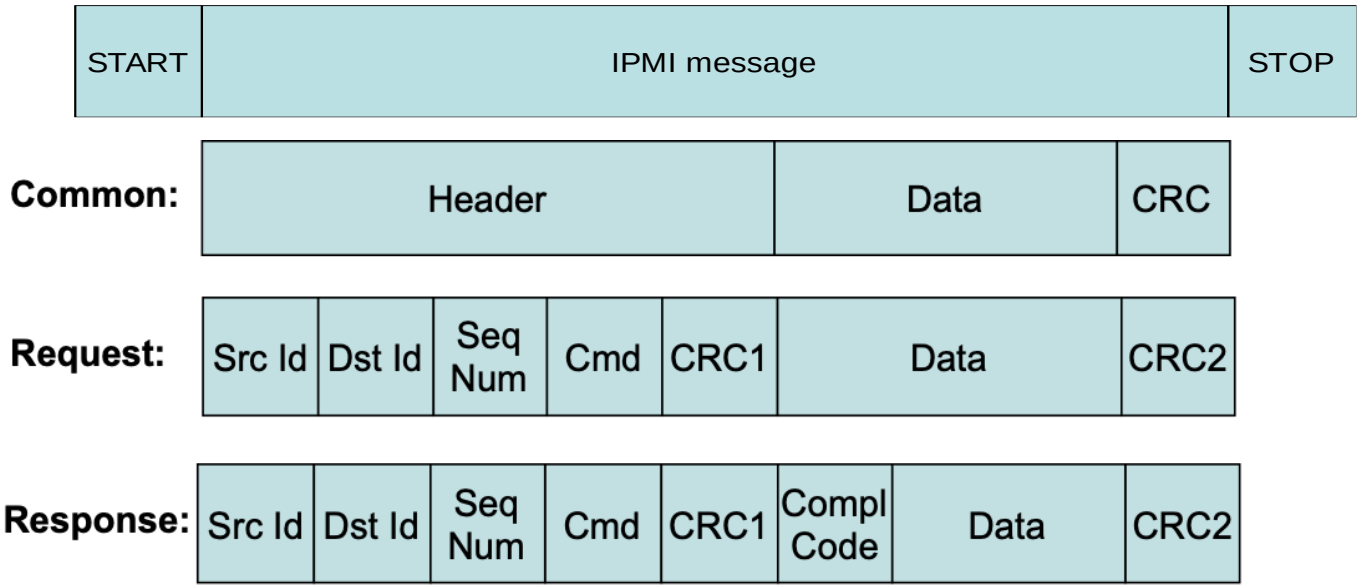
Management in MTCA Physical Connections And Controllers

- **IPMB-L**
  - connects the MCMC on the MCH to the MMC on the AMC Modules
  - radial architecture
- **IPMB-0 .1**
  - connects the MCMC on the MCH to the EMMC on the PMs and CUs
  - bussed architecture
- **I2C-bus**
  - connects the AMC to its µRTM
  - the µRTM is treated as managed FRU of the AMC

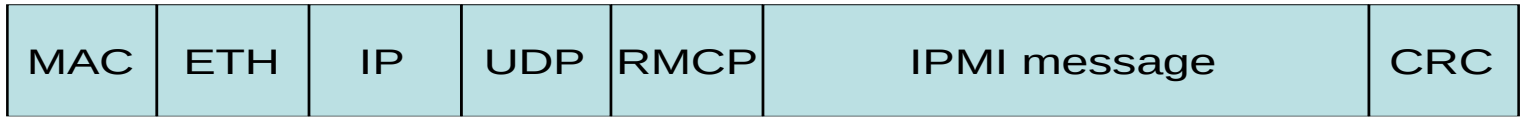


Management in xTCA IPMI

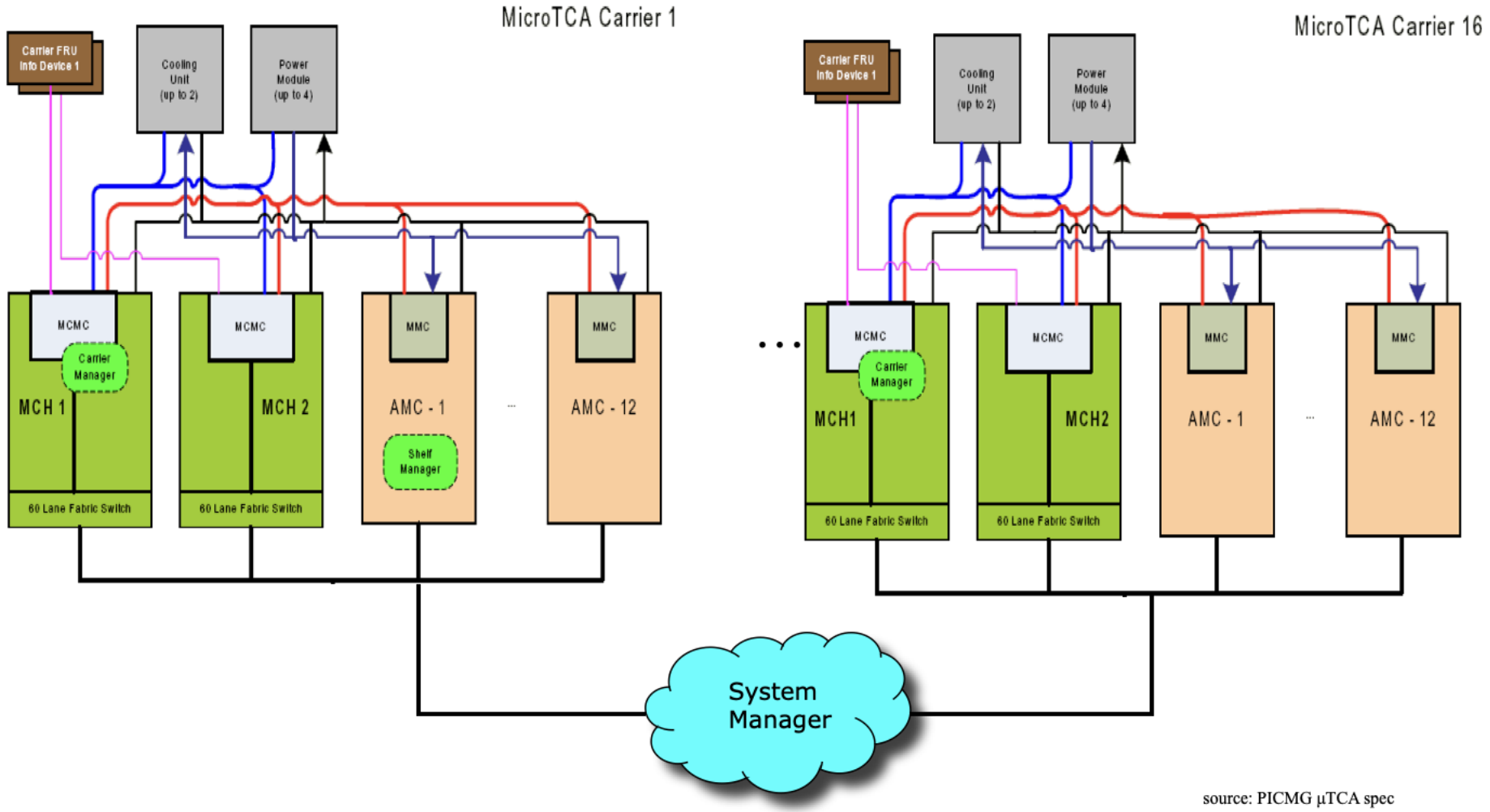
- IPMI protocol



- RMCP:

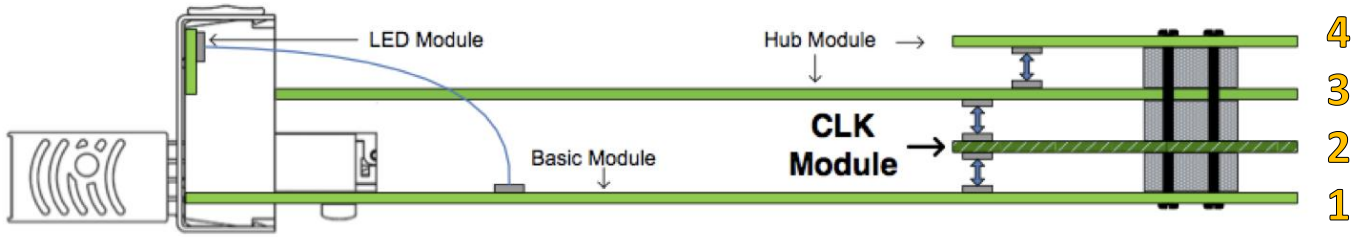


Management in MTCA Management Structure



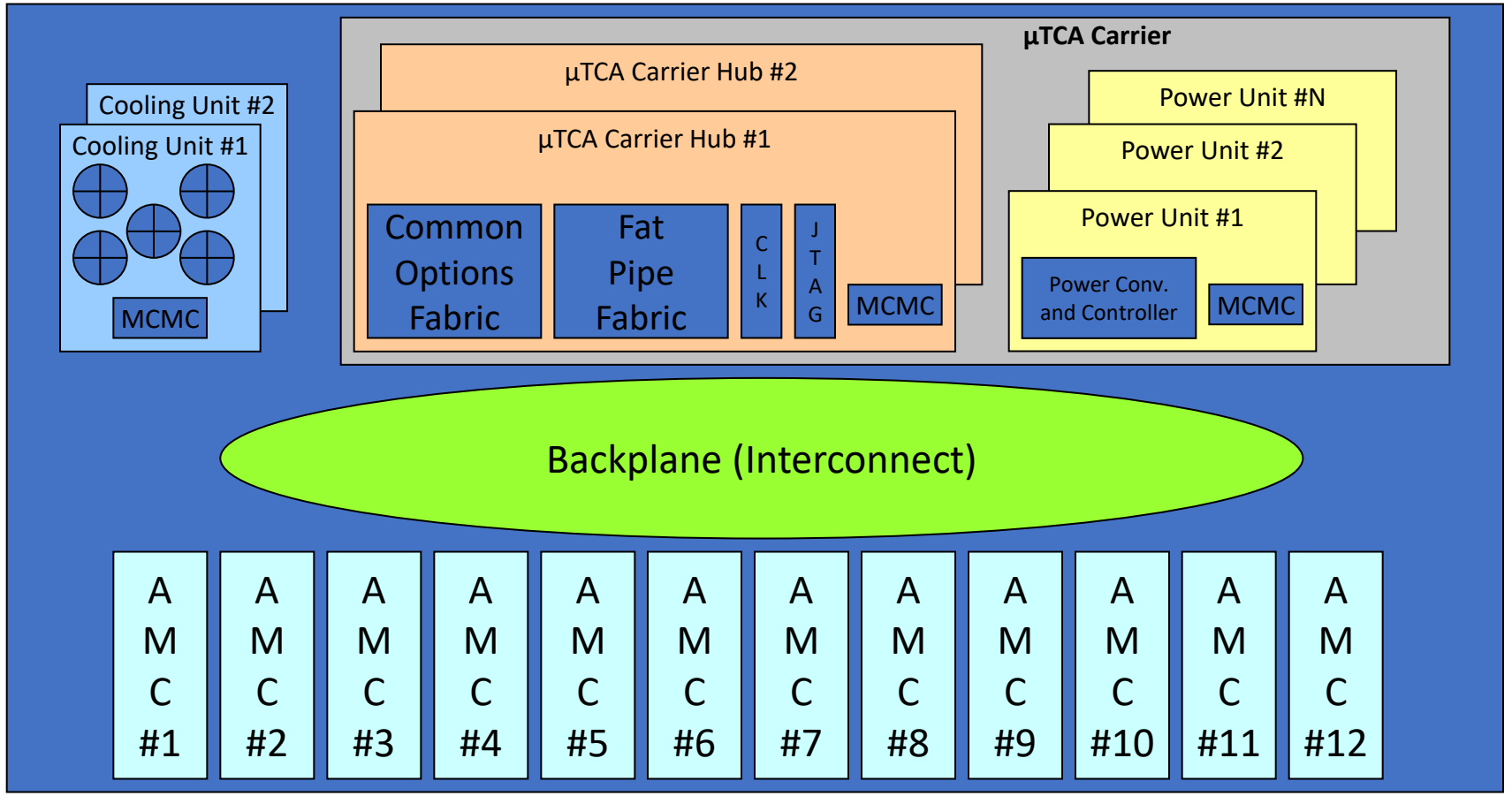
source: PICMG µTCA spec

MTCA Carrier Hub (MCH) Adaptable to application demands



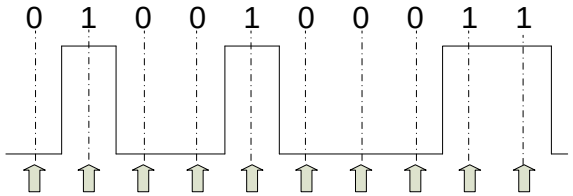
1. Base Module: base switch for all AMC slots and **management: carrier manager, shelf manager, system manager**
2. Clock Module for CLK #1-3 to all AMC slots
3. Fat Pipe Hub Module: fat pipe switch, signals to AMCs #1-6
4. Fat Pipe signals to AMCs #7-12

Excursus: fat pipes and clocks within a MicroTCA system

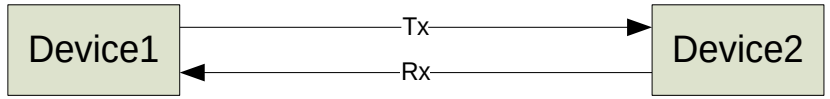


Excursus: fat pipes

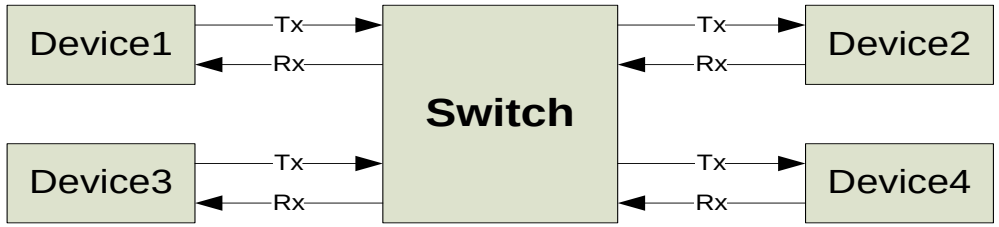
- Bits are transmitted one after the other over single data line
- **8B/10B Coding:** every data byte (8bit) is transformed to 10bit symbol that contains enough transitions



- Clock is recovered from serial stream
- Bidirectional transmission via dedicated Tx and Rx lines
  - One Tx/Rx pair is called "**Lane**"



- Multiple Devices interconnect by **switches**



Excursus: fat pipes within a MicroTCA system

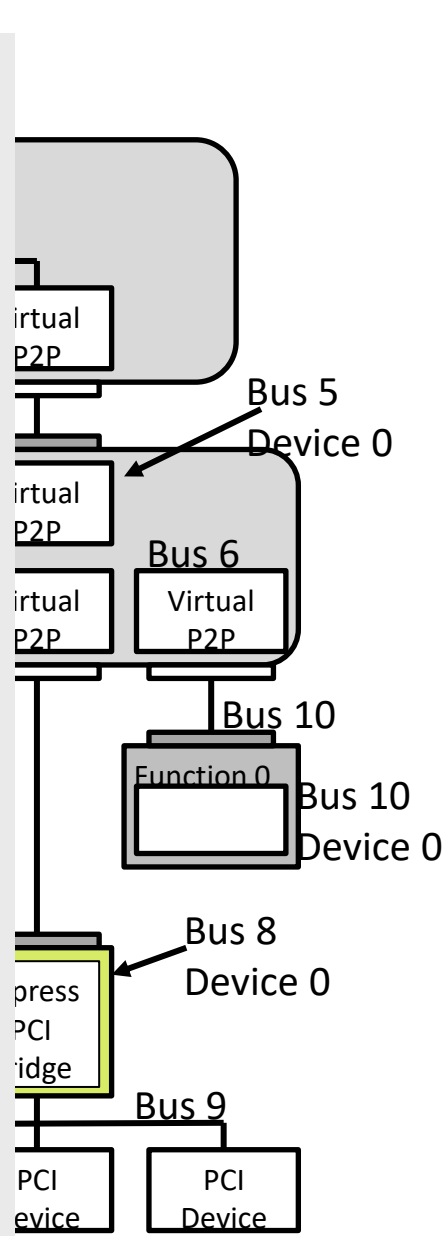
- Fat pipes aka fabrics
- Defined by PICMG AMC.x series
  - AMC.0 – Base Specification
  - AMC.1 – PCI Express (PCIe): gen 1, gen 2, gen 3 (gen 4)
  - AMC.2 – Ethernet: 1GbE, XAUI, 10GbE, 40GbE
  - AMC.3 – Storage (SAS)
  - AMC.4 – Serial RapidIO (SRIO)
- Link width: x1, x2, x4, lanes aka “ports”
- Compatibility between AMC and switch on MCH ensured by e-keying
- All signal levels are LVDS => incompatibility could not cause damage

Che

```
show_li
AMC  1
AMC  2
AMC  2
AMC  2
AMC  2
AMC  4
local R
   Ethe
   PCIe
```

lspci

00:00.0 Host bridge: Intel Corporation 2nd Generation Core Processor Family DRAM Controller (rev 09)
00:01.0 PCI bridge: Intel Corporation Xeon E3-1200/2nd Generation Core Processor Family PCI Express Root Port (rev 09)
00:01.1 PCI bridge: Intel Corporation Xeon E3-1200/2nd Generation Core Processor Family PCI Express Root Port (rev 09)
00:02.0 VGA compatible controller: Intel Corporation 2nd Generation Core Processor Family Integrated Graphics Controller (rev 09)
00:16.0 Communication controller: Intel Corporation 6 Series Chipset Family MEI Controller #1 (rev 04)
00:19.0 Ethernet controller: Intel Corporation 82579LM Gigabit Network Connection (rev 04)
00:1a.0 USB Controller: Intel Corporation 6 Series Chipset Family USB Enhanced Host Controller #2 (rev 04)
00:1c.0 PCI bridge: Intel Corporation 6 Series Chipset Family PCI Express Root Port 1 (rev b4)
00:1d.0 USB Controller: Intel Corporation 6 Series Chipset Family USB Enhanced Host Controller #1 (rev 04)
00:1f.0 ISA bridge: Intel **Corporation QM67 Express Chipset Family LPC Controller** (rev 04)
00:1f.2 IDE interface: Intel Corporation 6 Series Chipset Family 4 port **SATA** IDE Controller (rev 04)
00:1f.3 SMBus: Intel Corporation 6 Series Chipset Family SMBus Controller (rev 04)
00:1f.5 IDE interface: Intel Corporation 6 Series Chipset Family 2 port SATA IDE Controller (rev 04)
01:00.0 PCI bridge: Integrated Device Technology Inc. Device 808f
01:00.2 System peripheral: Integrated Device Technology Inc. Device 808f
02:08.0 PCI bridge: Integrated Device Technology Inc. Device 808f
03:00.0 PCI bridge: **PLX Technology Inc. Device 8748** (rev ba)
04:00.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:01.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:02.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:08.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:09.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:0a.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:0b.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:10.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:11.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:12.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
04:13.0 PCI bridge: PLX Technology Inc. Device 8748 (rev ba)
09:00.0 RAM memory: **Xilinx Corporation Device 0037**
0a:00.0 RAM memory: Xilinx Corporation Device 0037
10:00.0 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)
10:00.1 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)



Excursus: clocking within a MicroTCA system

- Defined by PICMG MTCA.0 and AMC.0
  - frequency limited to 100MHz by spec
  - from an MCH perspective: CLK1, CLK2, CL3
  - from an AMC perspective: TCLKx and FCLK
  - mapping between CLK1-2 and TCLKx/FLCK provided by the backplane
  - Compatibility between AMC and switch on MCH ensured by e-keying

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Thank you for your attention !

Heiko Körte
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