European XFEL and PETRA IV Timing Systems

Overview

Victor Andrei

DESY, MCS (Machine Control System)

[*on behalf of the MCS and PETRA IV WP 2.09 Timing and RF Synchronisation groups*]

MTCA Workshop, DESY, Hamburg, 02.12.2025

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

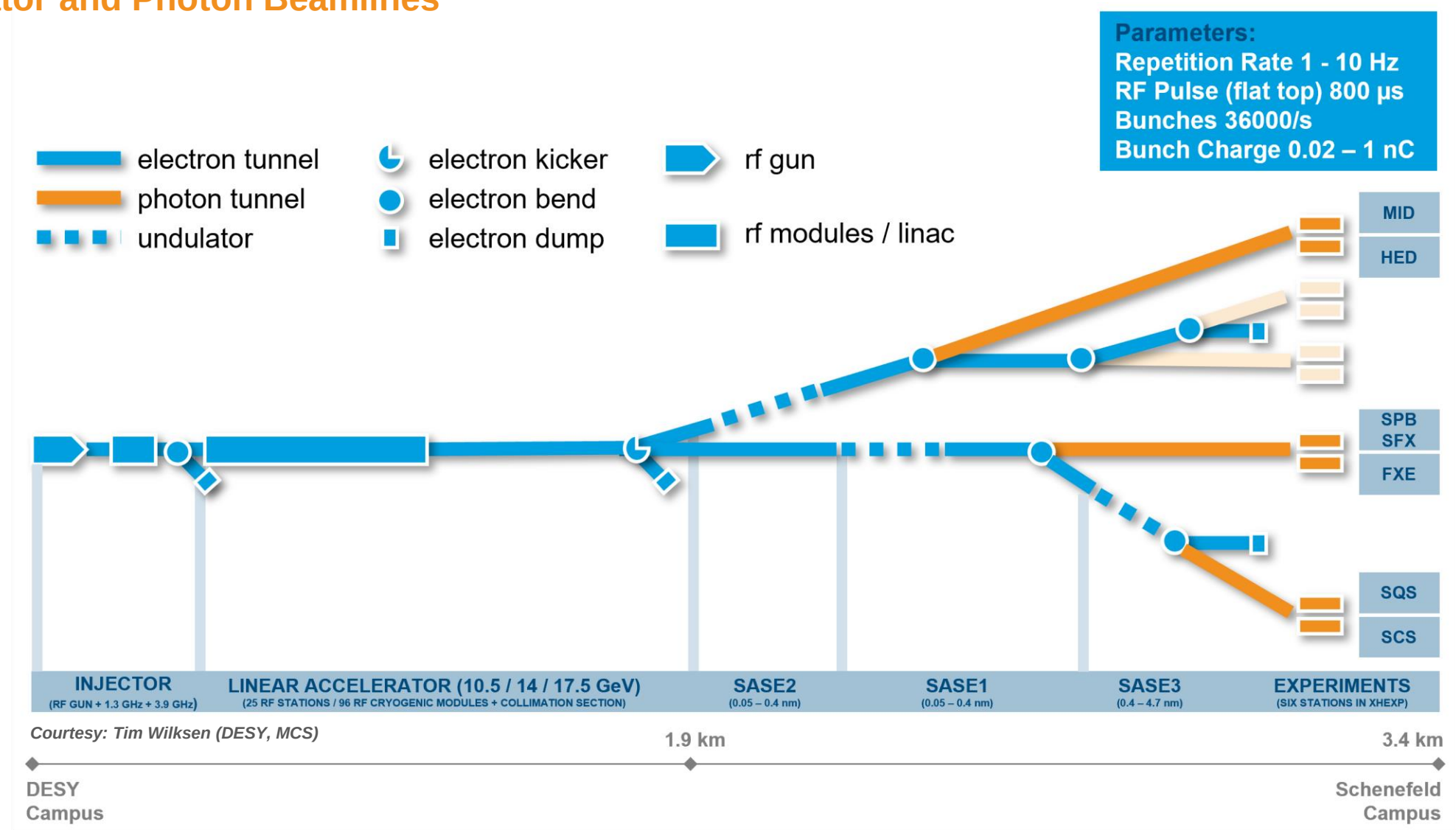
Outline

- **European XFEL / PETRA IV machine characteristics and requirements**
- **Timing System Concepts**
- **MTCA.4 Components of the Timing System**
- **Timing System Software**
- **Summary**

The EuXFEL Timing System

The European XFEL

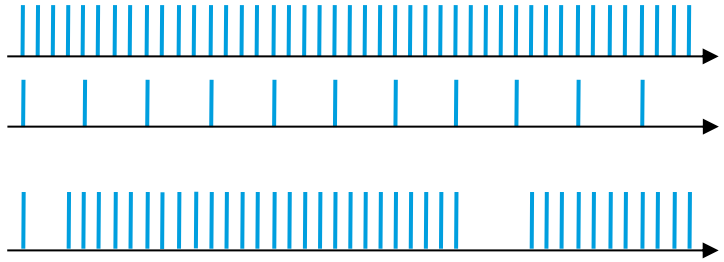
Accelerator and Photon Beamlines

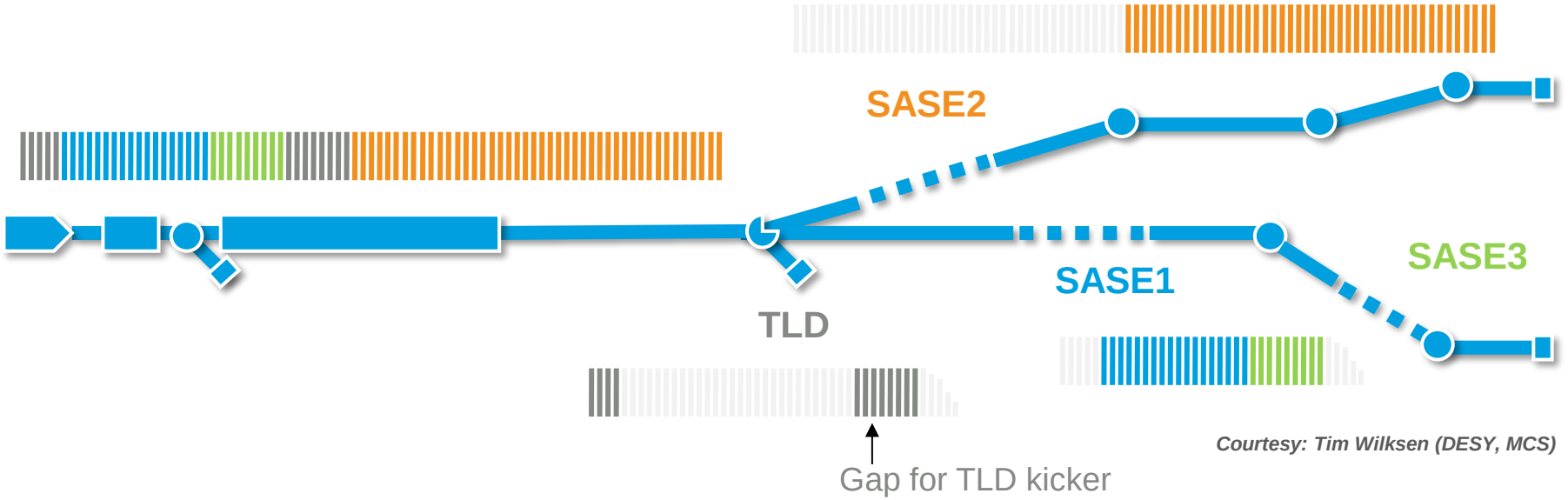


Timing System Concepts

Machine And Experiments Requirements – Pulsed Machine

- RF Reference 1.3 GHz
- Bunches up to 36000/s over 800 µs RF pulse
- Bunch spacing from 502 kHz [1992 ns] up to 4.5 MHz [222 ns] at 10 Hz repetition [9 MHz raster → 111 ns steps]
- Pre-bunches, intermediate gaps
- Beamline-specific and user-defined bunch patterns



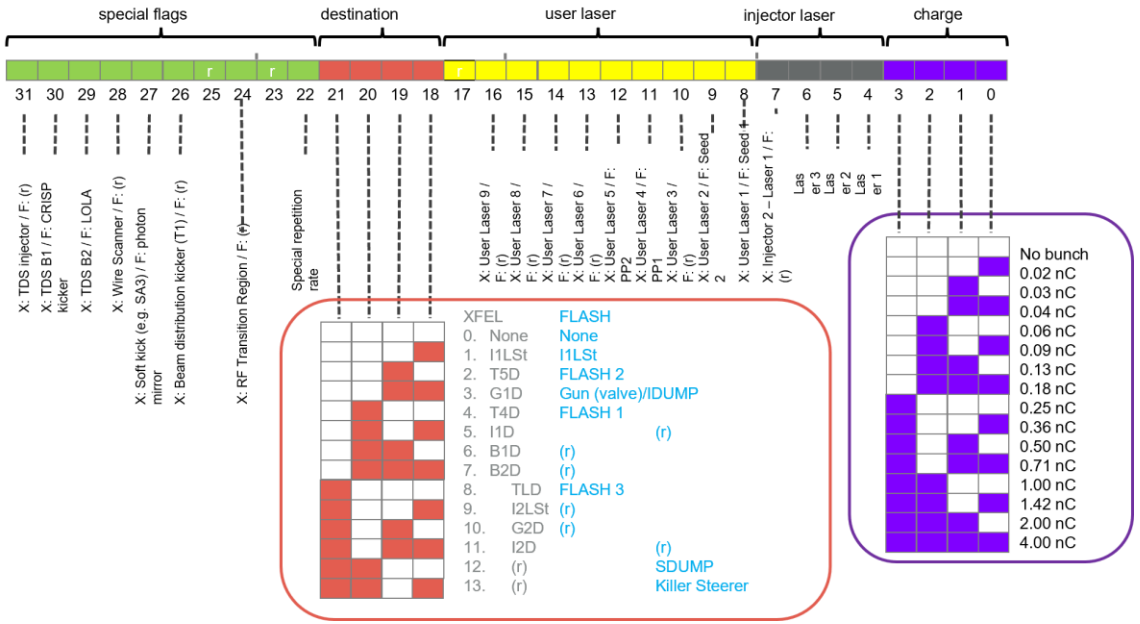


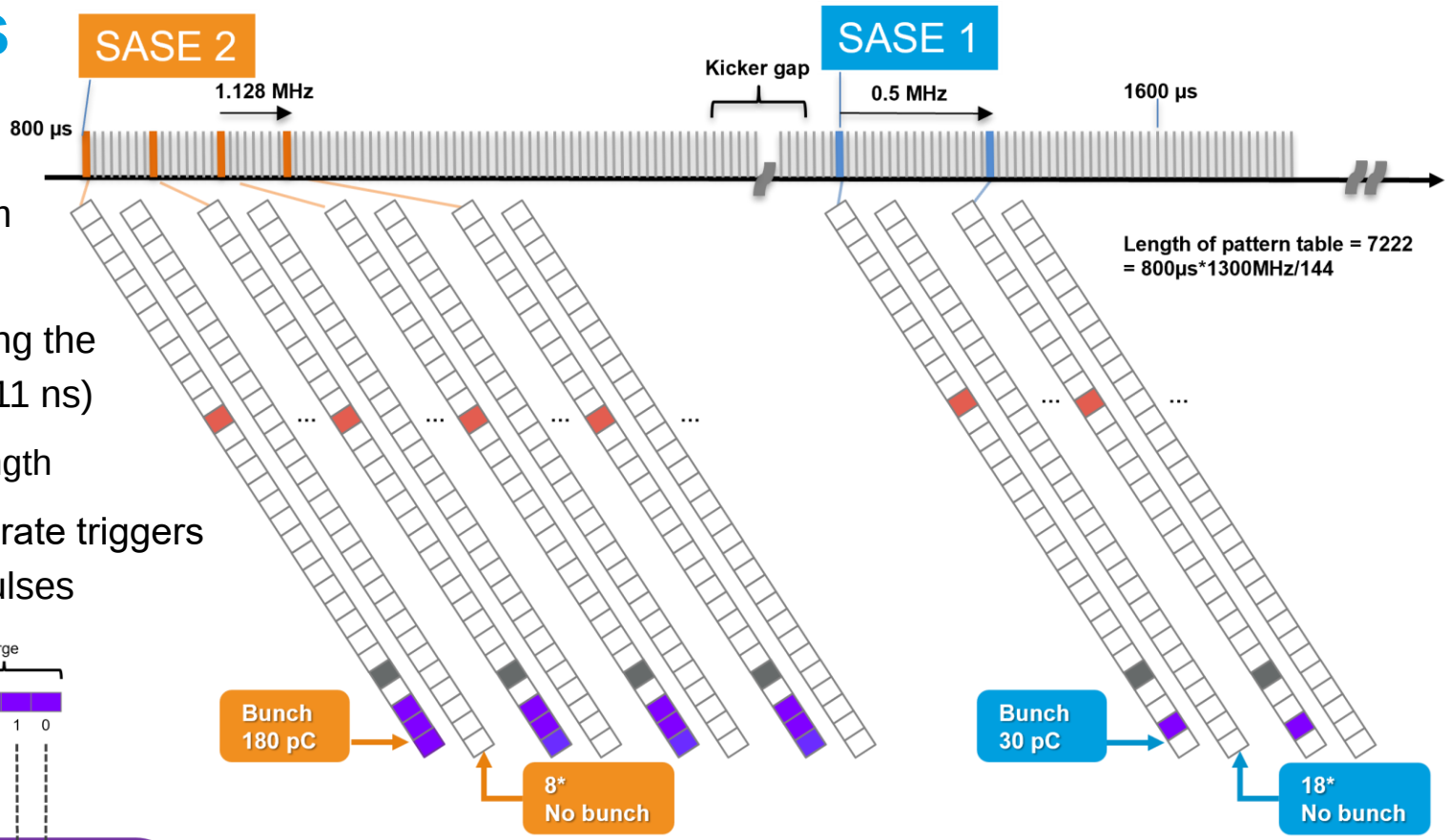
Courtesy: Tim Wilksen (DESY, MCS)

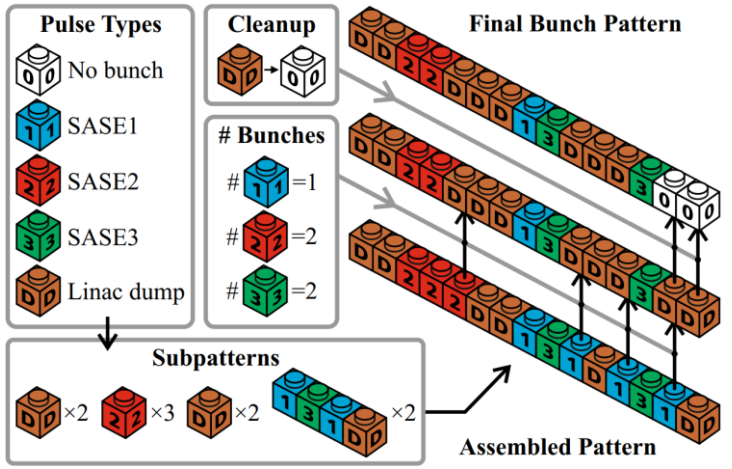
Timing System Concepts

The Timing (Bunch) Pattern

- Information block distributed by the timing system before each macro pulse or bunch train.
- *Table* of **8192 32-bit** *timing words*, each describing the bunch configuration at one 9 MHz raster point (111 ns)
  - **7222** timing words cover the **800 µs** RF pulse length
- Timing words → used by timing modules to generate triggers and by hard- and software to classify bunches/pulses







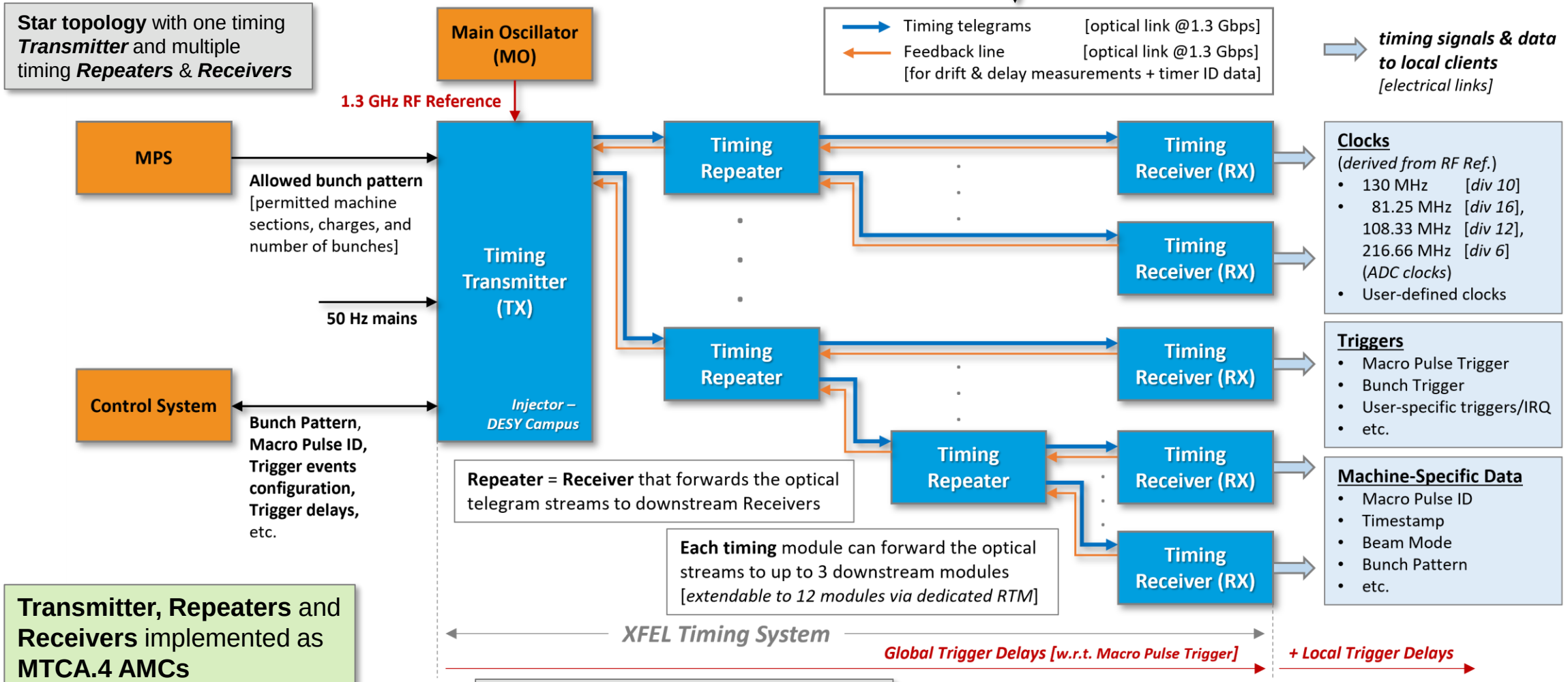
Courtesy: Lars Fröhlich (DESY, MCS)

Timing System Concepts

Layout, Topology & Distribution of Signals and Data

Telegrams contain: bunch pattern table, macro pulse trigger, trigger events configuration, commands, etc. **Routed back** to transmitting module to measure & compensate the drift.

Star topology with one timing ***Transmitter*** and multiple timing ***Repeaters*** & ***Receivers***



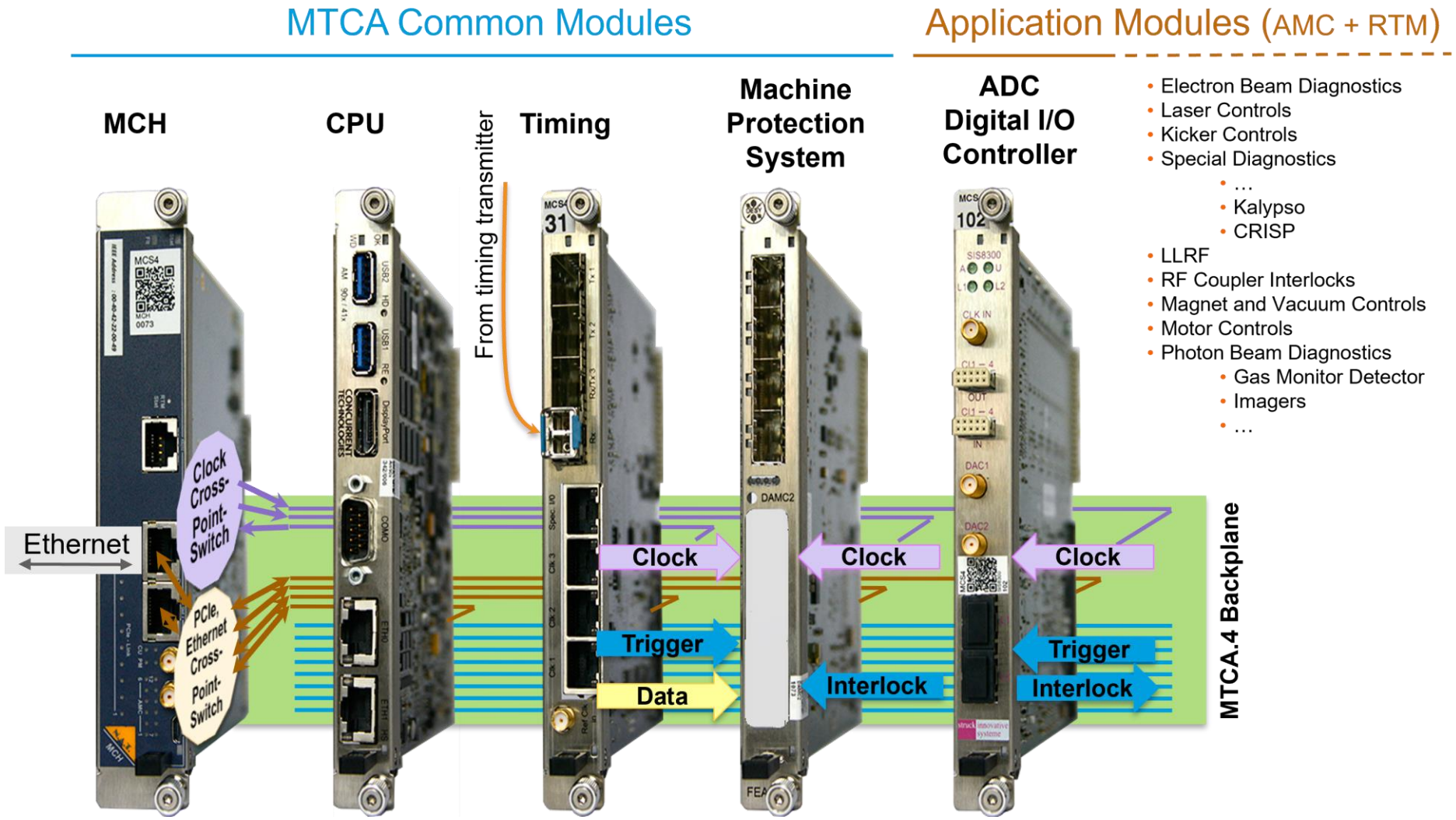
Transmitter, Repeaters and **Receivers** implemented as **MTCA.4 AMCs**

Repeaters & **Receivers** are distributed along the accelerator and photon beamlines

Each Repeater & Receiver
- recovers the **1.3 GHz RF Reference**
- decodes the **Telegram** data from the input optical stream.

MTCA.4 Timing System Components

Timing in a MTCA.4 Crate



MTCA.4 Timing System Components

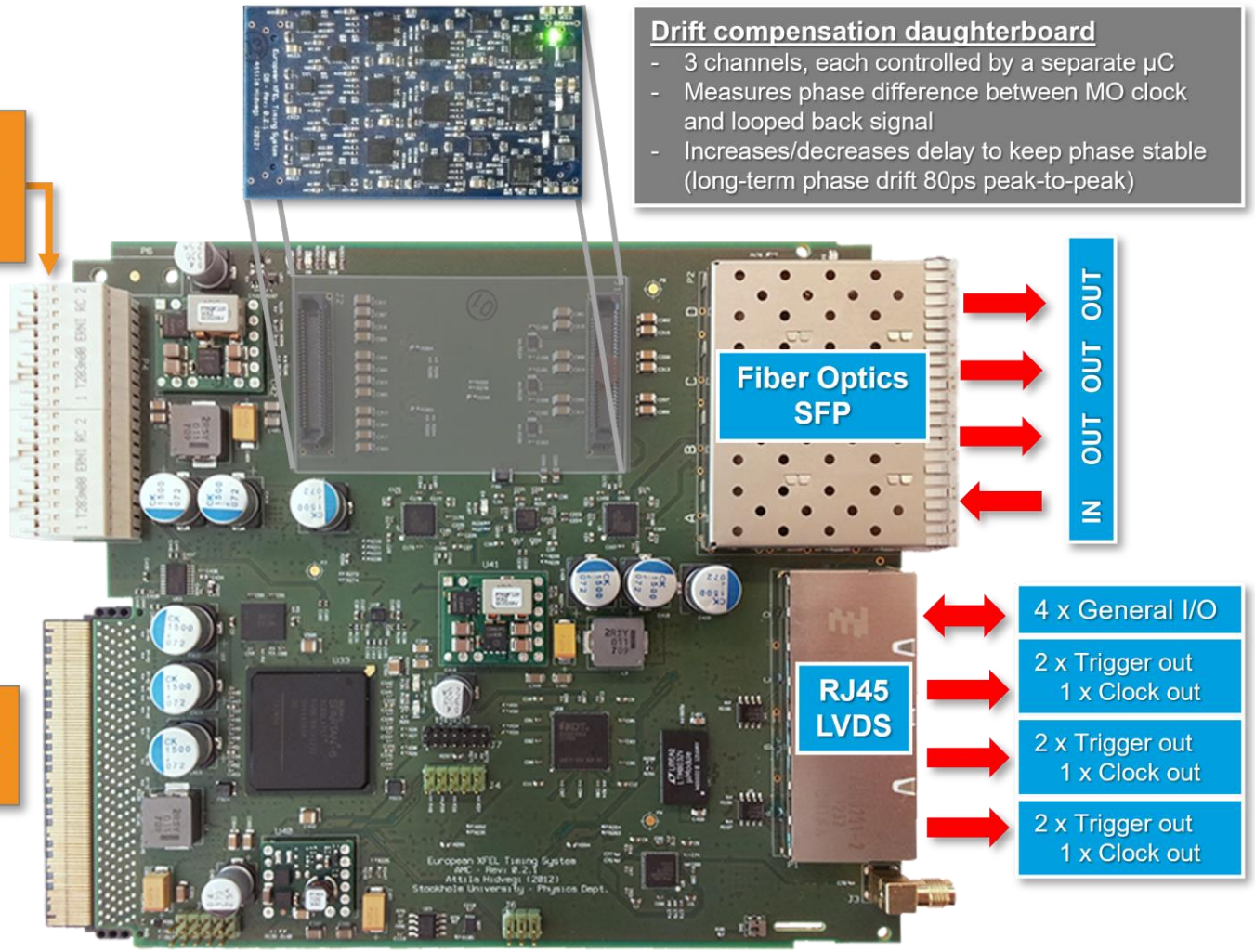
x2timer / NAMC-psTimer AMC

Double mid-size AMC (with optional RTM)

- May be operated as
  - **Transmitter, Repeater** or **Receiver**
  - Stand-alone w/ on-board PLL
- Optical Tx/Rx of 1.3 GHz telegram streams
- Low-jitter clock (5) and trigger (23) outputs
- Xilinx Spartan-6 FPGA (central logic unit)
- Software-accessible via PCIe
- Hot-swap capable
- Once configured it runs autonomously
  - No trigger/clock interruption if crate CPU is maintained/rebooted/replaced

Optional RTM:
9x optical-TX (SFP),
9x LVDS & TTL
(triggers or clocks)

MicroTCA backplane:
Clocks : TCLKA & TCLKB
Triggers : 8x M-LVDS



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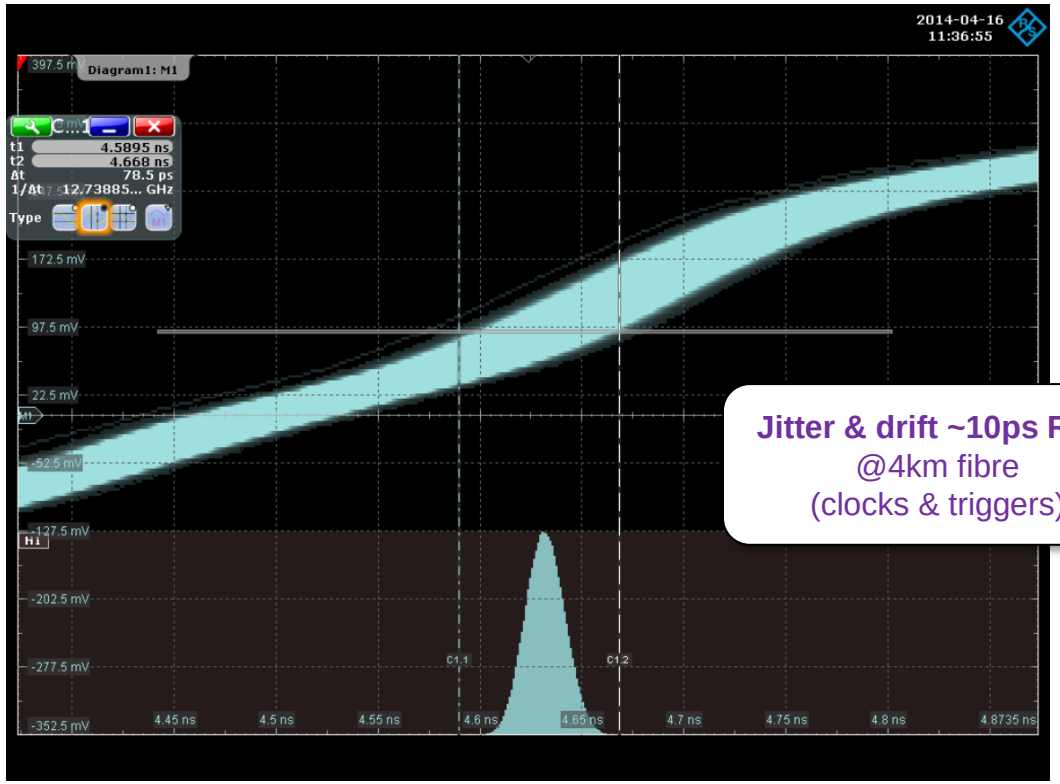
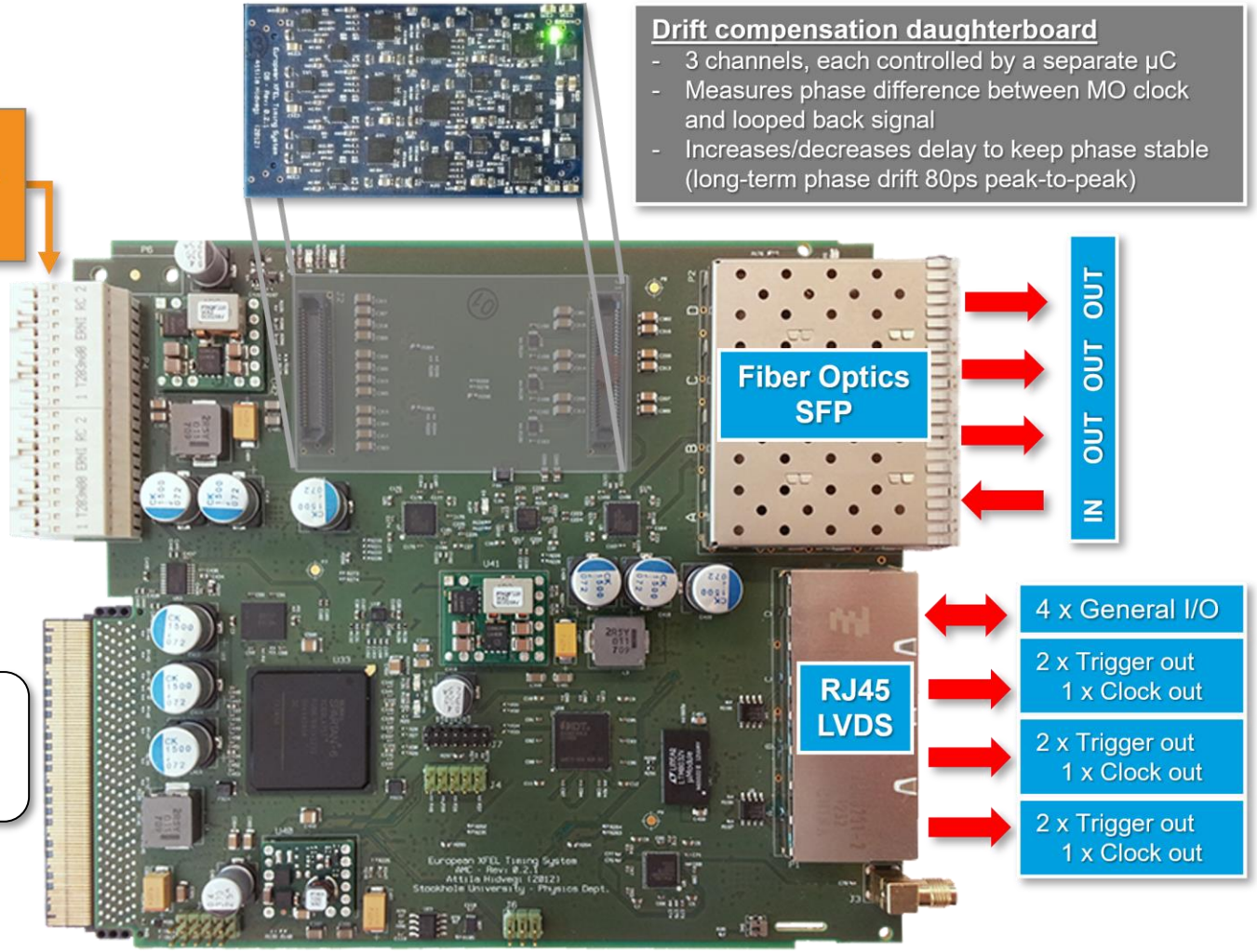


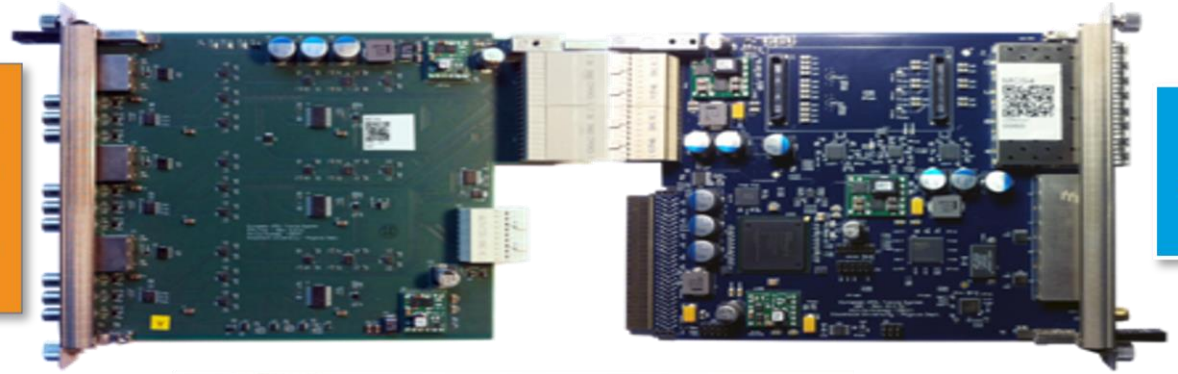
Jitter & drift ~10ps RMS
@4km fibre
(clocks & triggers)



MTCA.4 Timing System Components

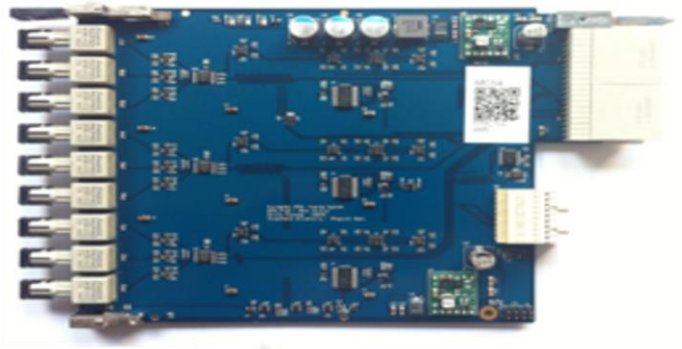
Timing RTMs (Rear Transition Modules)

RTM with **9 Lemo outputs** (50 Ohm) for trigger, clock and data distribution – 3 high-precision outputs (5ps steps)

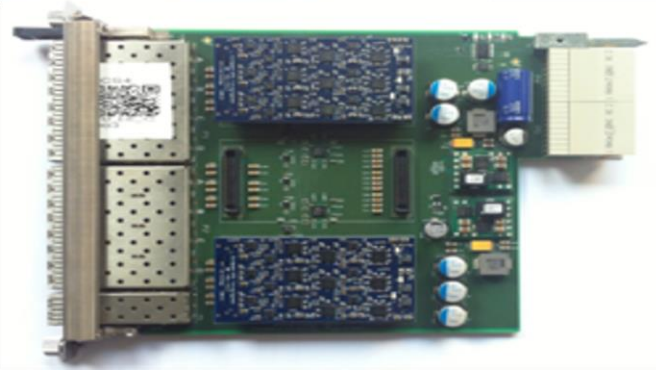


x2Timer / NAMC-psTimer Receiver-Transmitter MicroTCA.4 AMC

RTM **with 9 optical outputs** (ST connector) for trigger, clock and data distribution

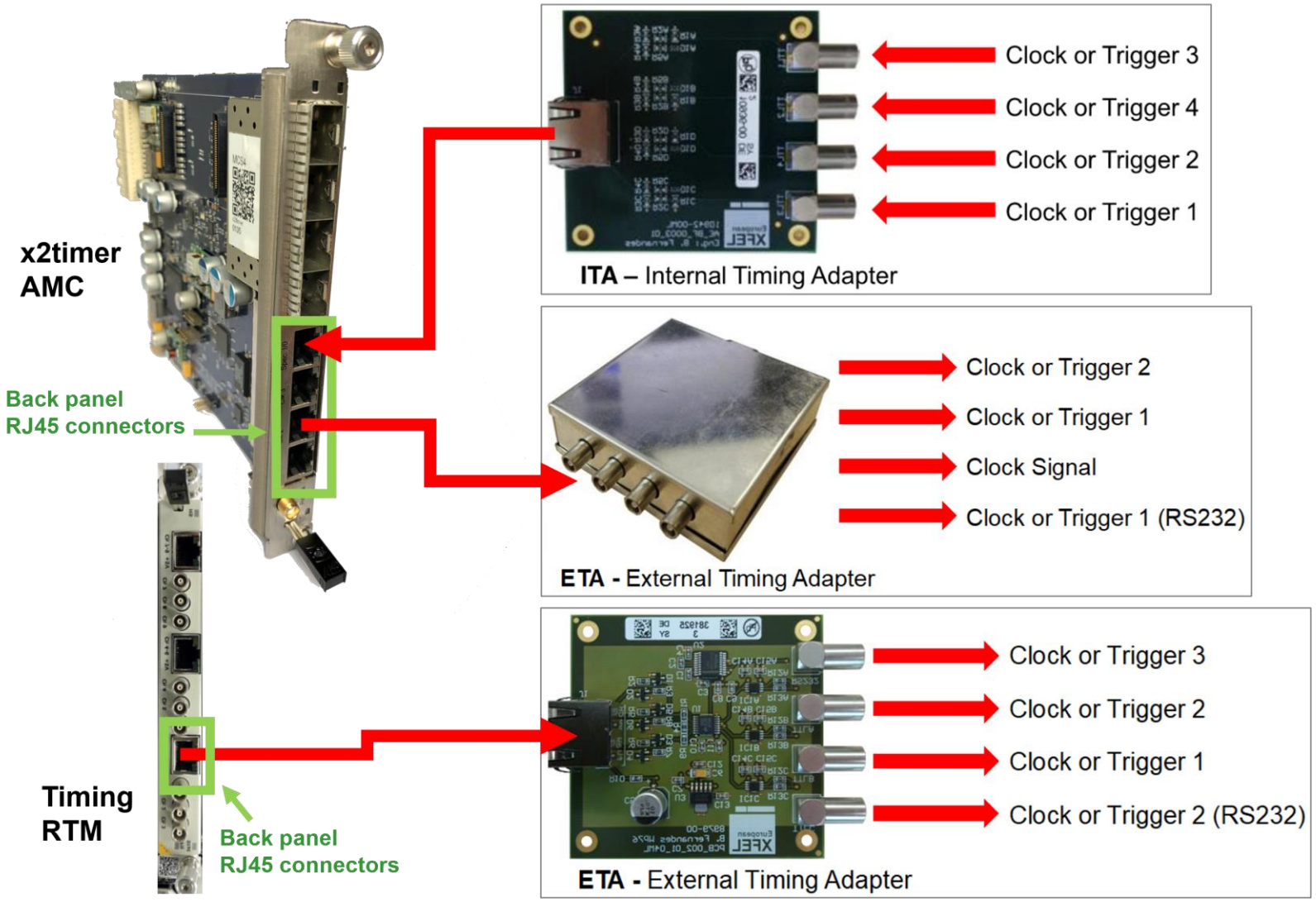


RTM with **9 optical SFP outputs –** length and drift compensated fiber links per channel



MTCA.4 Timing System Components

Adapters



- local clients → x2timer AMC
- TTL to LVDS conversion

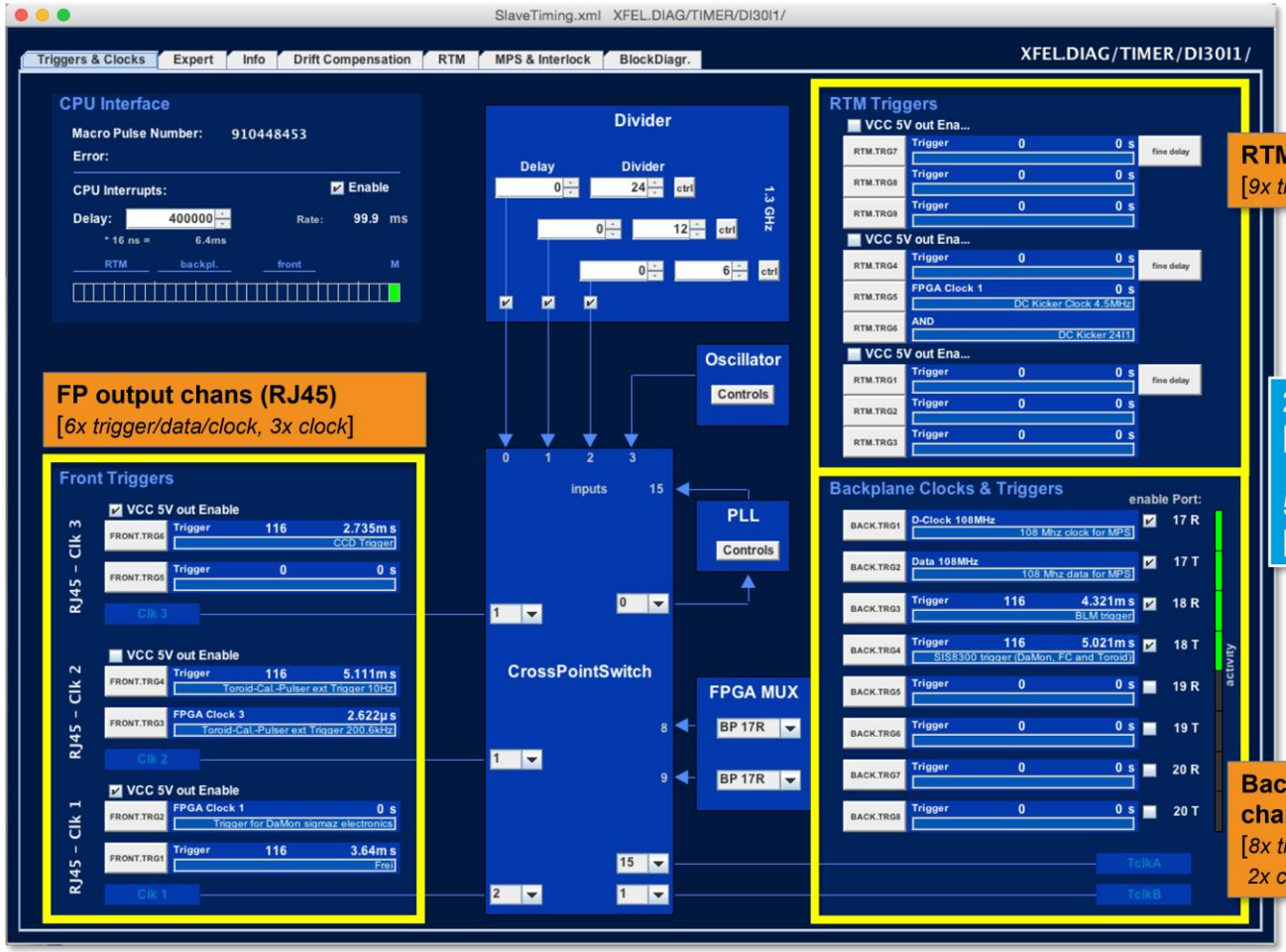
- x2timer AMC → local clients
- LVDS to TTL / RS232 conversion
- individually configurable interfaces

- x2timer RTM → local clients
- LVDS to TTL / RS232 conversion
- individually configurable interfaces

Timing System Software

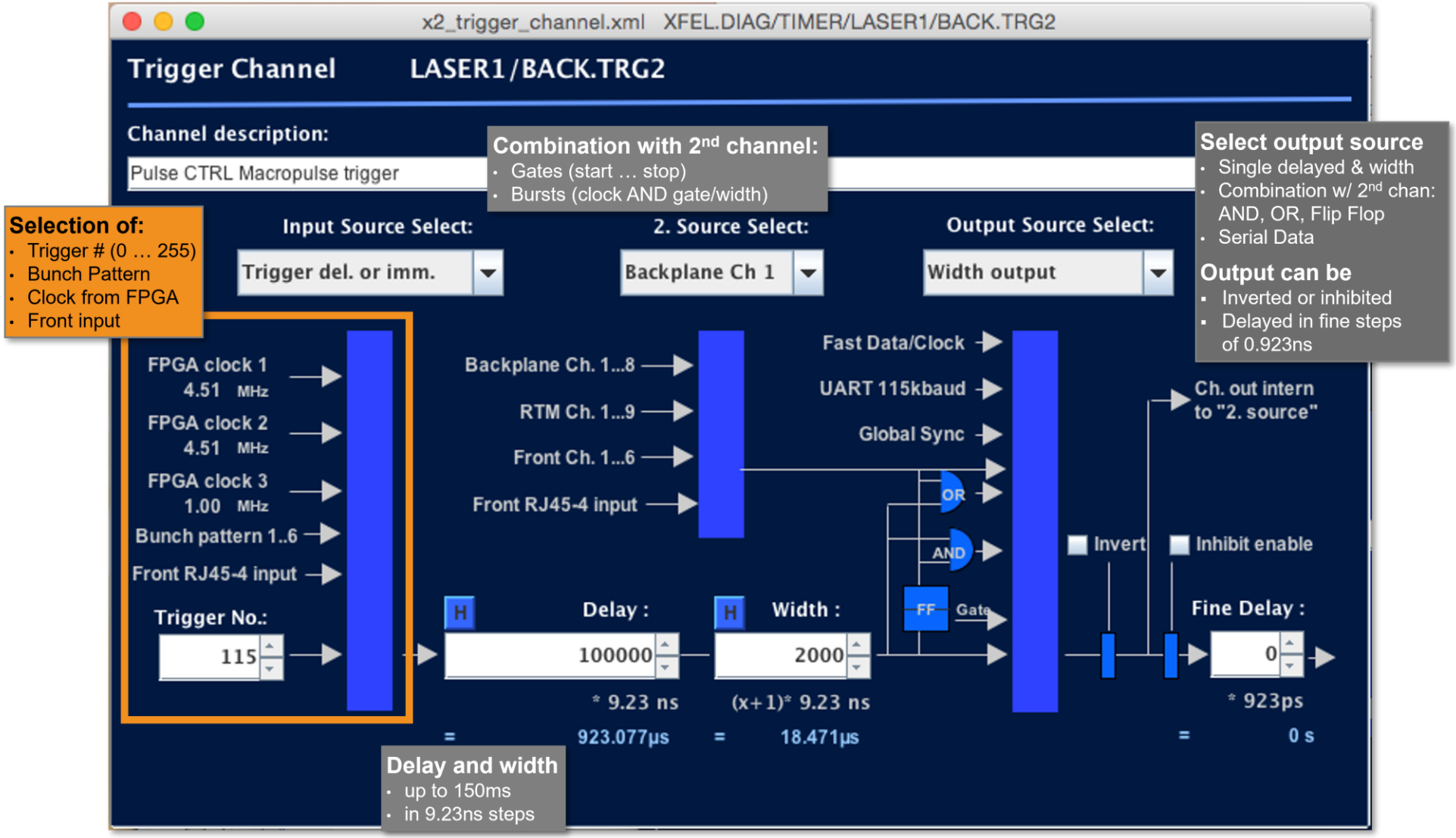
x2timer server & JDDD Configuration Panel

- **x2timer server** running on the crate CPU AMC
  - can manage several x2timer AMCs and RTMs in the crate via PCIe
- Configurable remotely over Ethernet with DOOCS and JDDD user interface



Timing System Software

One Trigger/Data/Clock Channel Configuration



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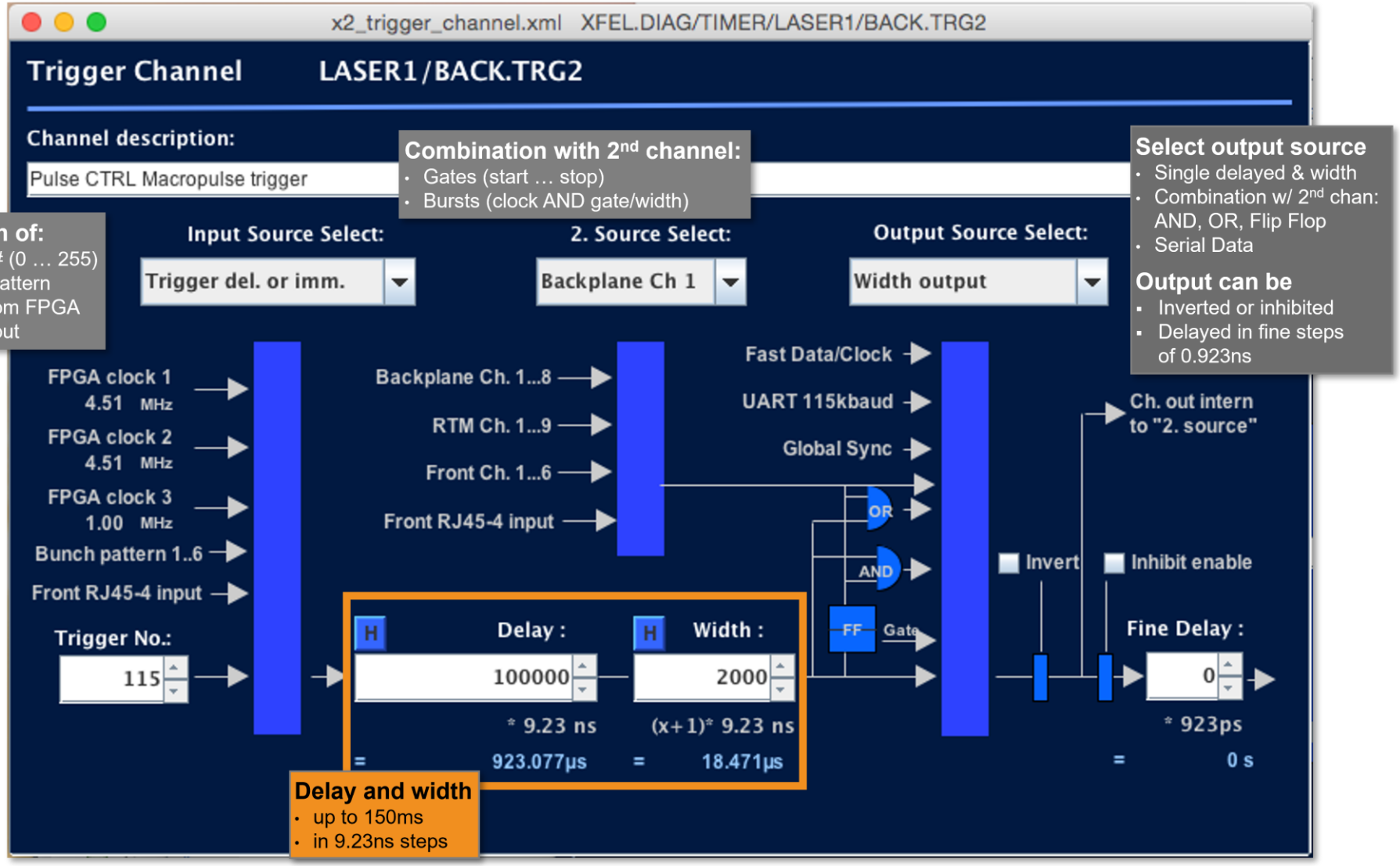

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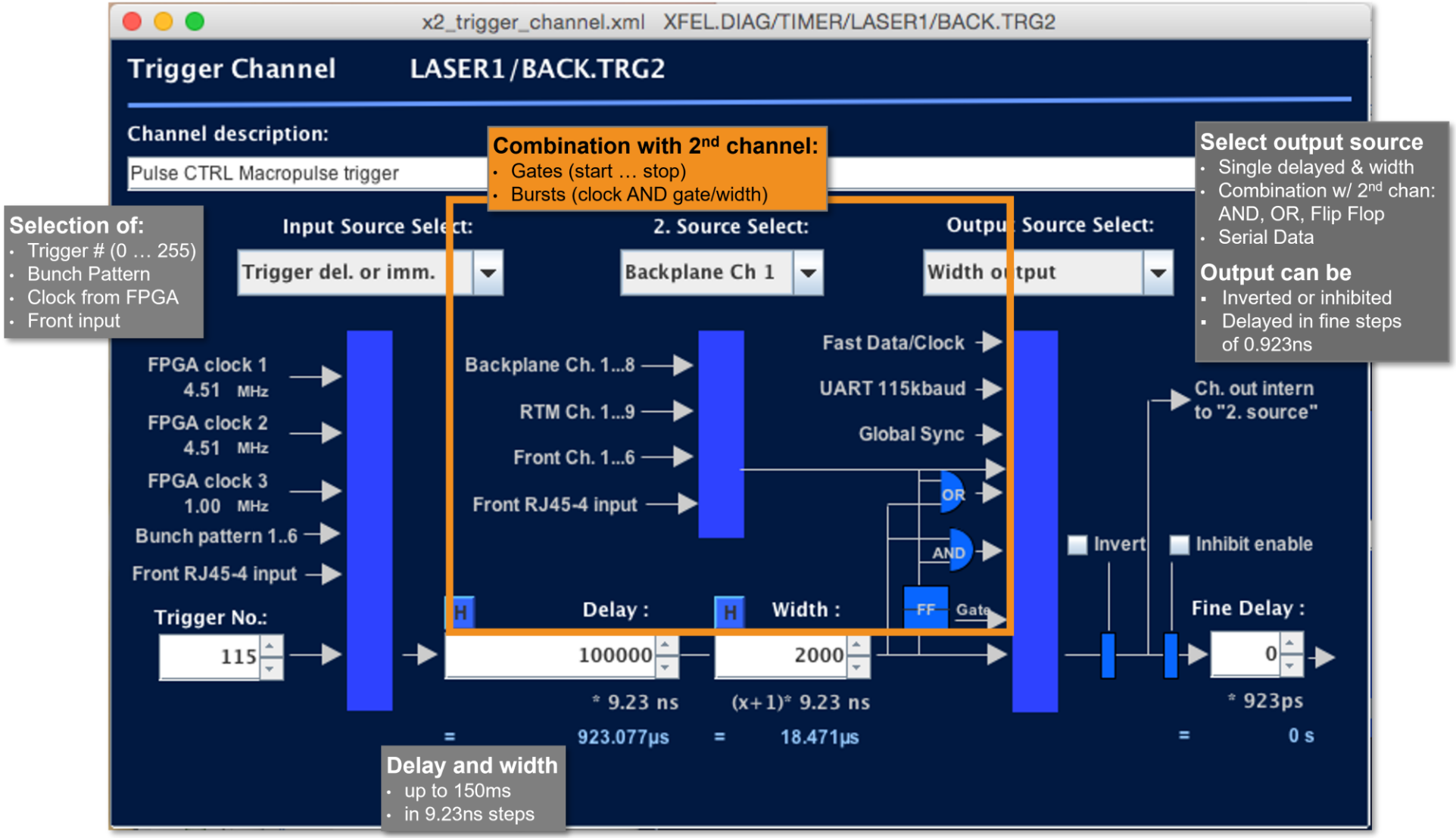

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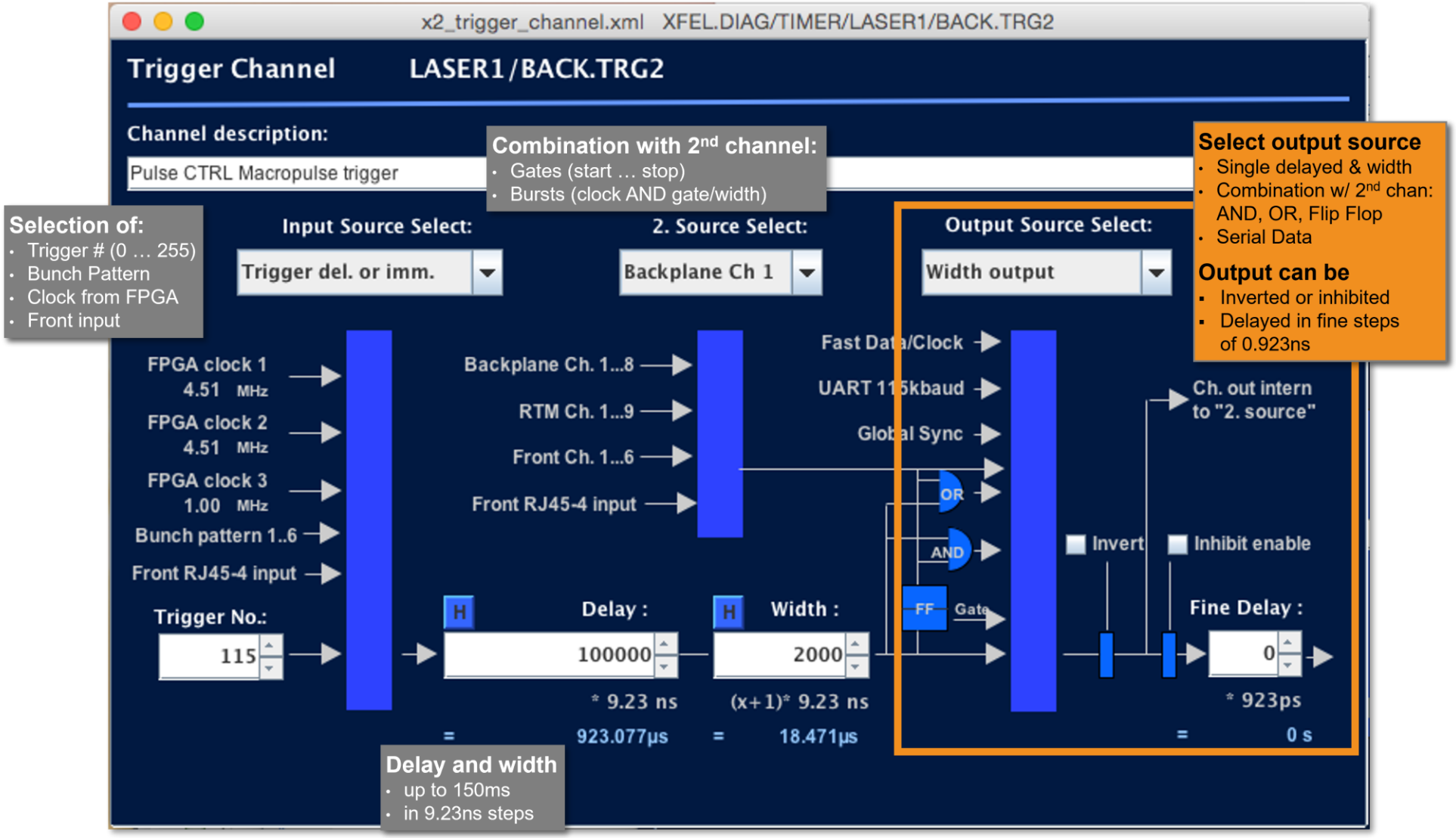
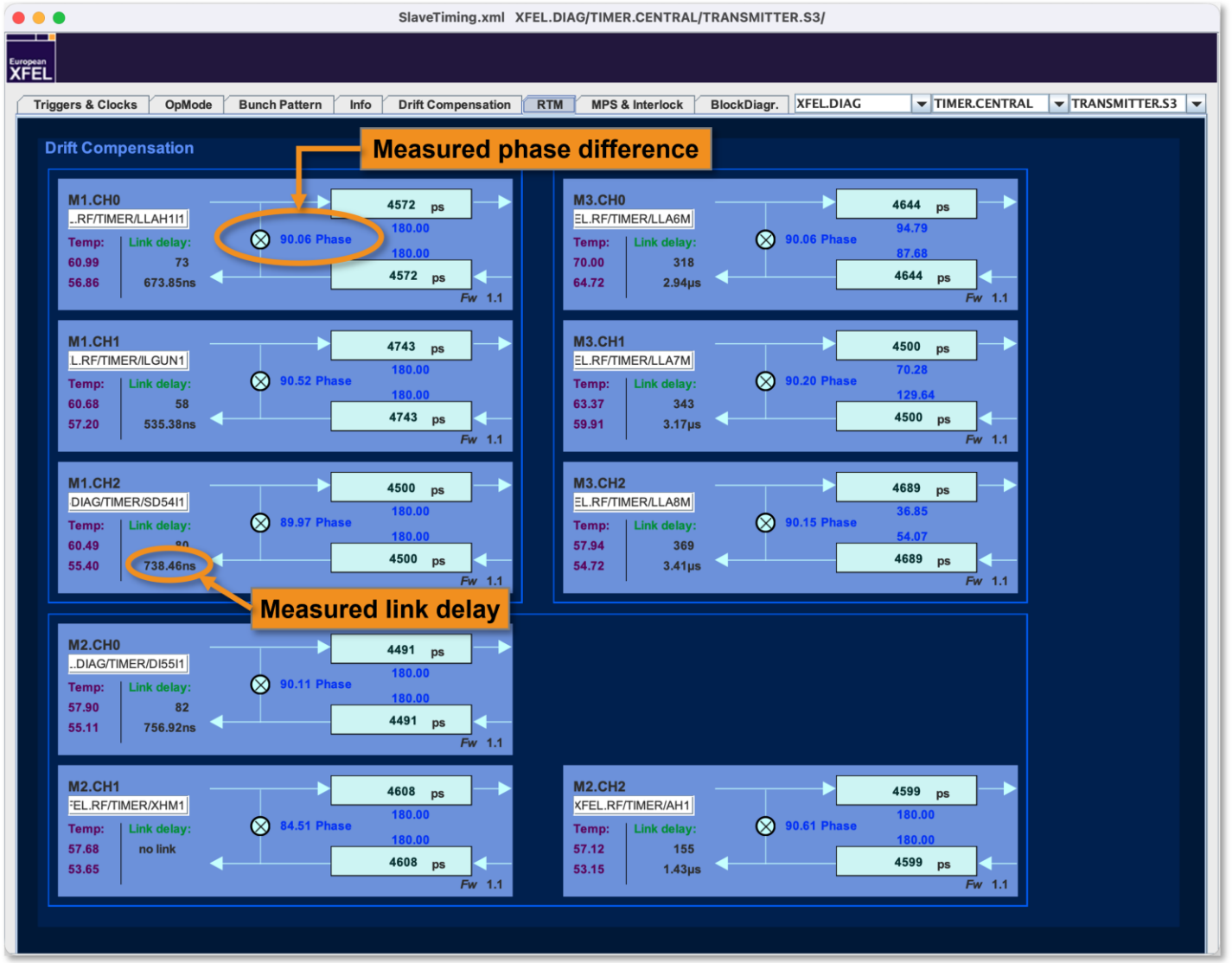


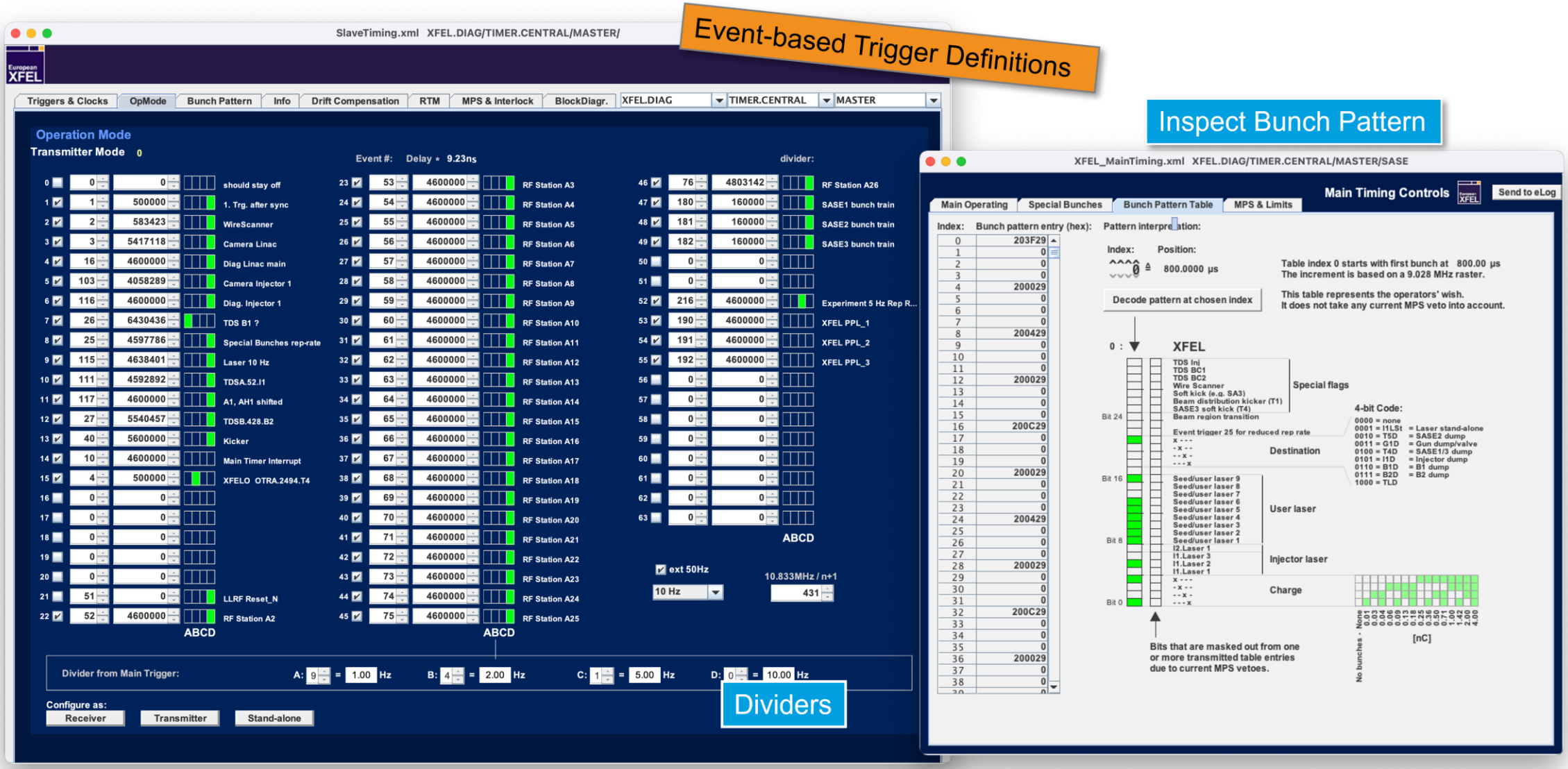
Timing System Software

Optical Links and Drift Compensation



Timing System Software

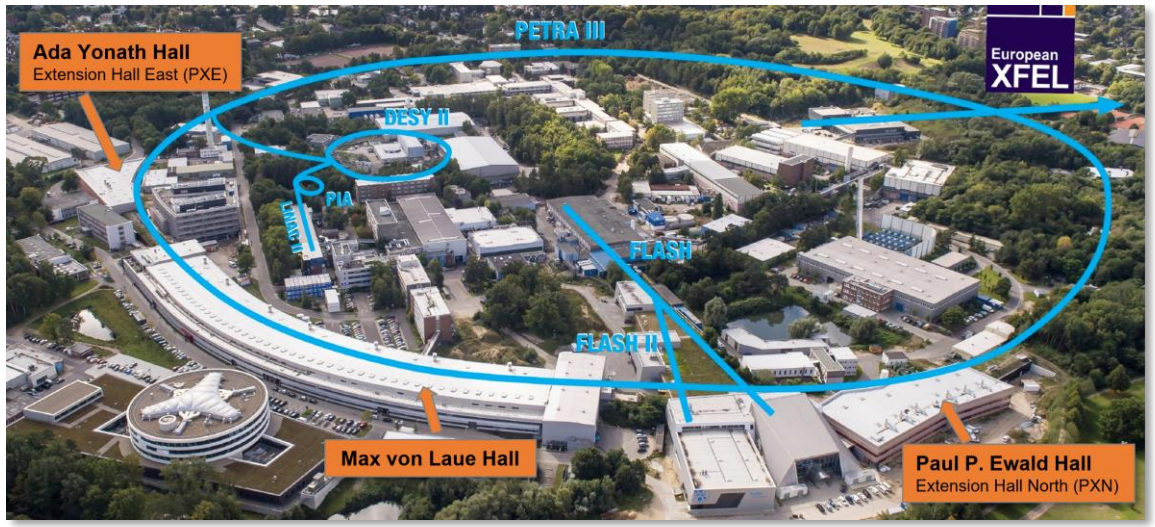
Main Timing – Operator Interface



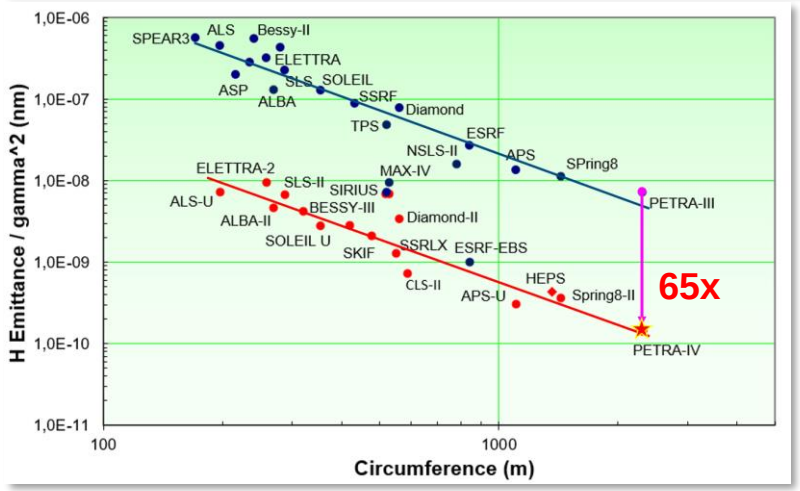
The PETRA IV Timing System

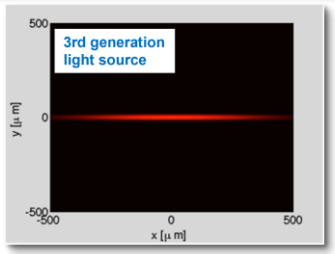
Upgrade of PETRA III to PETRA IV

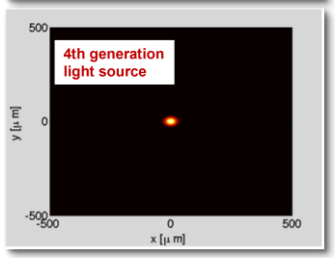
From the 3rd to the 4th-generation synchrotron radiation source



The new PETRA IV synchrotron will replace PETRA III with an ultra low emittance ring adding a new experimental hall with beamlines.

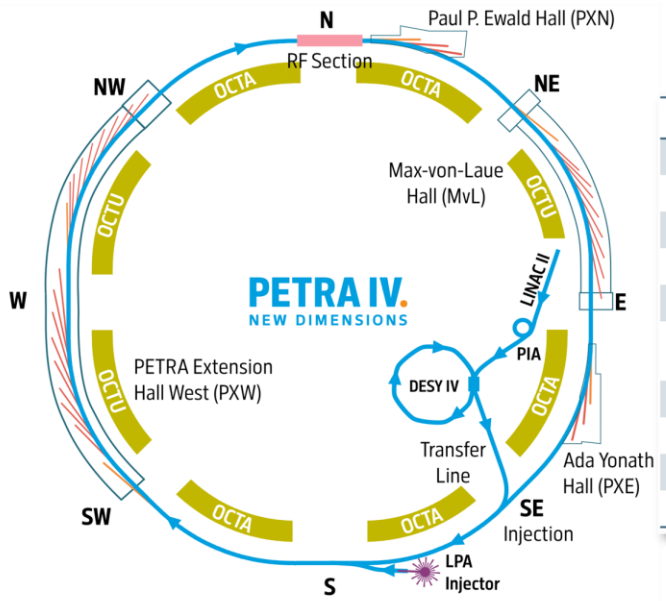






PETRA IV will be essentially a "New Machine"

- **Complete renewal** of accelerator, injector and beamlines
- New RF sender, magnets, orbit feedback, beam diagnostics
- New injector (LPA – Laser Plasma Accelerator) and new experimental hall (PXW)
- **MTCA.4** to become the **standard** for r/o electronics
- New control system based on European XFEL experiences



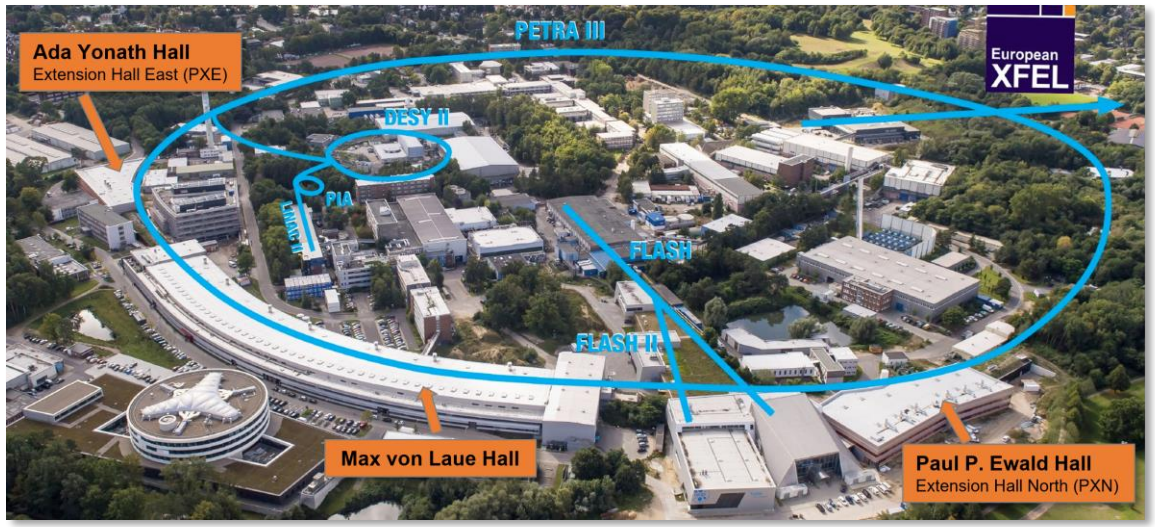
upgrade: until 2029 ← → from 2032

Parameter	PETRA III	PETRA IV
Energy	6 GeV	6 GeV
Length	2304 m	2304 m
Emittance (H/V)	1300/13 pm-rad	**< 20/3.33 pm rad**
Brightness Mode	480b@200 mA	**1920b@200 mA**
Timing Mode	40b@100 mA	**80b@80 mA**
RF Frequency	499.6643 MHz	499.6643 MHz + **1.4989929 GHz**
Harmonic Number	3840	3840
Revolution Freq.	130.121 kHz	130.121 kHz
Electronics Std.	VME, SEDAC, etc.	**MTCA**
Control System	Tine	**DOOCS + TANGO**

- New lattice type: **Hybrid Six-Bend Achromat (H6BA)**
- 8 arcs [9 H6BA cells/arc] + ID straight sections
- **More beamlines (37)** [**12** (von Laue Hall) + **3** (PXN) + **4** (PXE) + **18 (PXW)**]

Upgrade of PETRA III to PETRA IV

From the 3rd to the 4th-generation synchrotron radiation source



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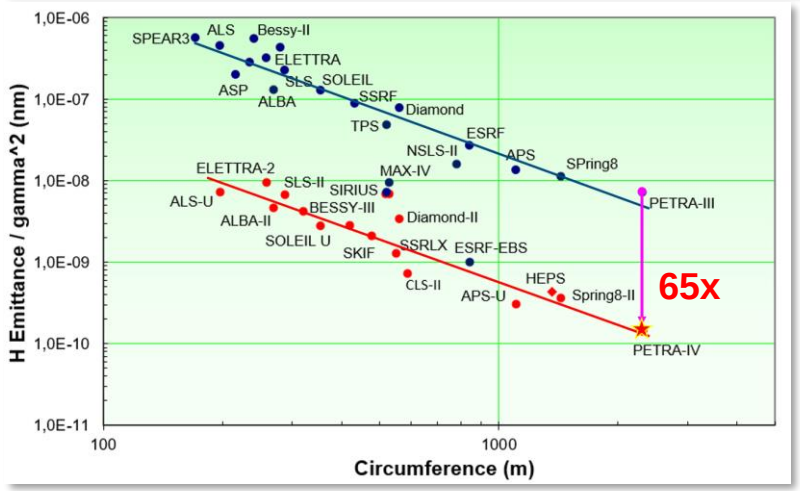

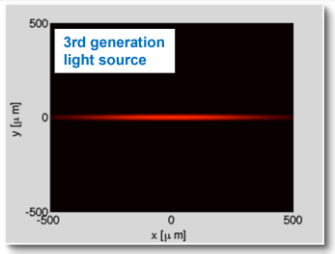

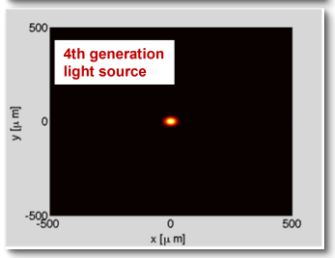

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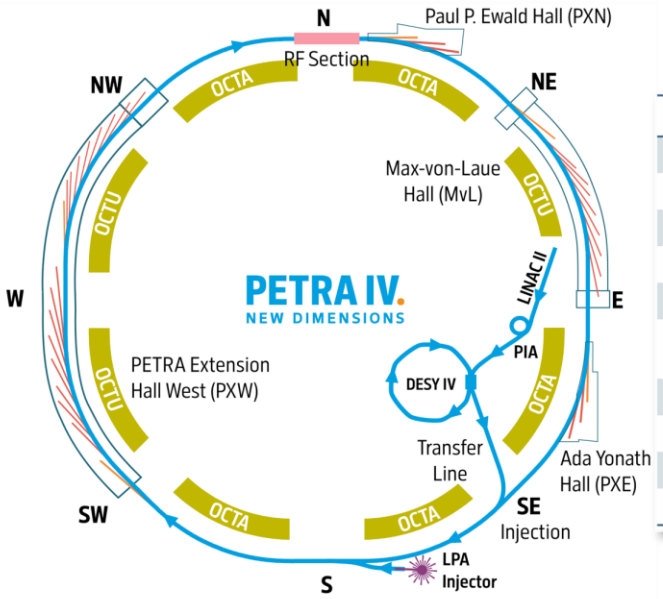
- New control system based on European XFEL experiences

New timing system needed!



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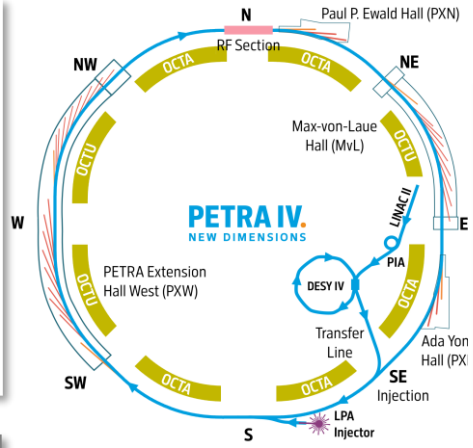
- New lattice type: **Hybrid Six-Bend Achromat (H6BA)**
- 8 arcs [9 H6BA cells/arc] + ID straight sections
- **More beamlines (37)** [**12** (von Laue Hall) + **3** (PXN) + **4** (PXE) + **18 (PXW)**]

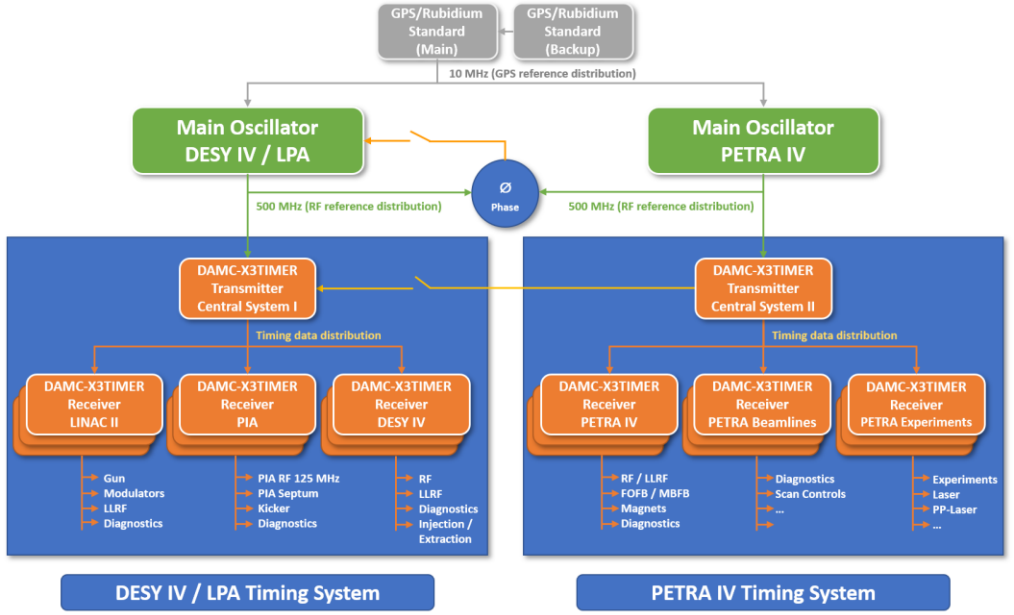
PETRA IV Timing System Concepts

Requirements

Machine & Experiments Requirements – Storage Ring

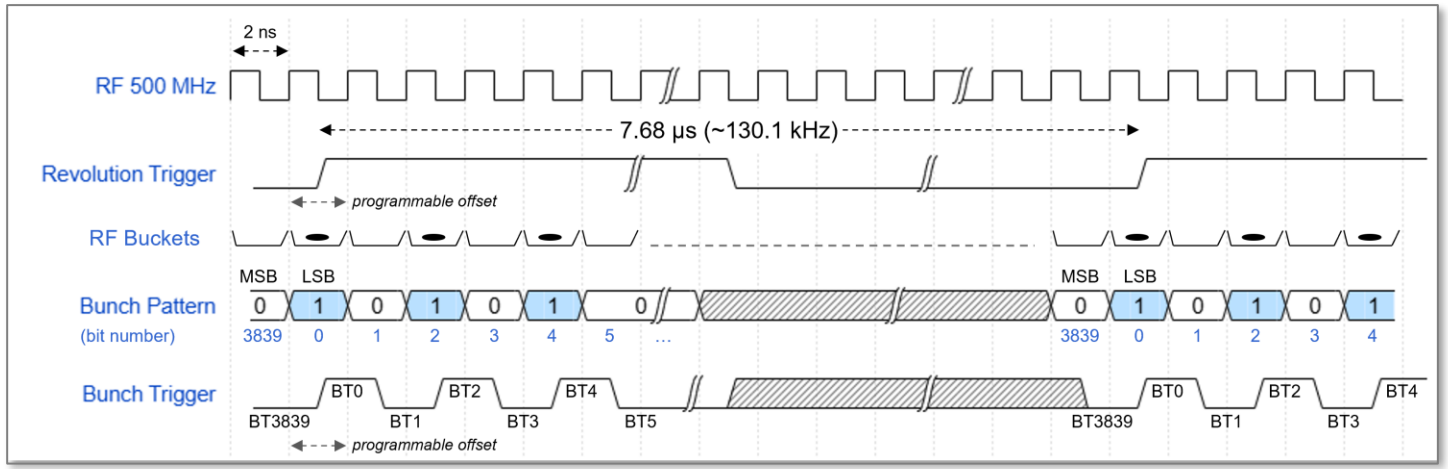
- RF Reference 500 MHz
- Revolution Frequency ~130.1 kHz
- 3840 RF buckets (2ns spacing)
- Two main operation modes:
  - Brightness mode: 1920b@200mA (4ns spacing)
  - Timing mode: 80b@ 80mA (96ns spacing)
- Two injectors (DESY IV / LPA)
- 37 beamlines in four halls





Key Requirements For The Timing System:

- Distributing a continuous RF reference signal
- Provide low jitter clocks (e.g. for ADC sampling)
- Provide continuous timing signals & trigger events
- Provide machine- & timing-specific data such as:
  - Revolution counter
  - Machine state, beam mode
  - Bunch pattern, beam currents, etc.
- Dedicated distribution network with drift compensation
- Common hardware for transmitter and receiver
- Common timing system for accelerator and beamlines (decoupled from the injector's timing system for chromaticity studies)



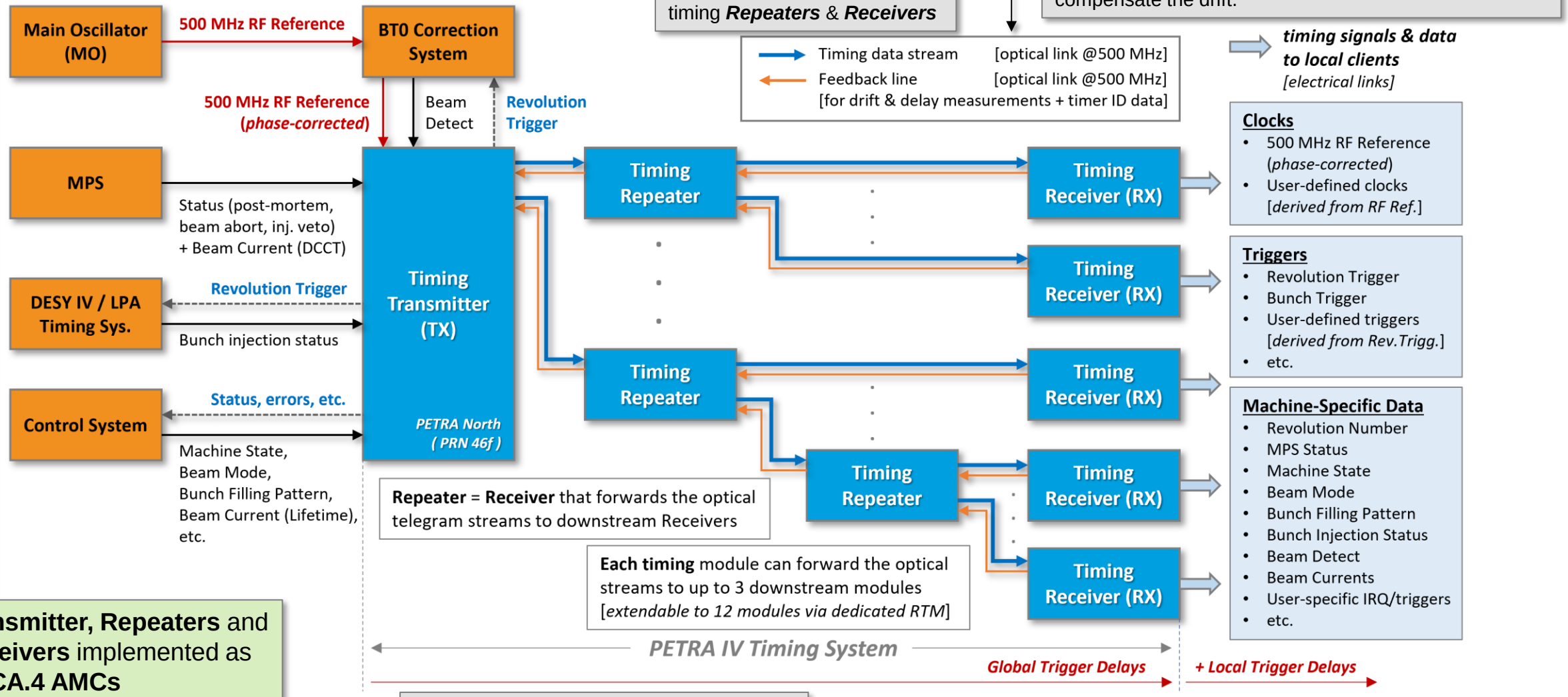
Generation of Revolution Trigger and Bunch Trigger in the PETRA IV Timing System. The example describes the case of a 4ns gap between two consecutive filled RF buckets (as in Brightness Mode). The configuration of the first filled RF bucket will be stored in the LSB of the Bunch Pattern.

PETRA IV Timing System Concepts

Layout, Topology & Distribution of Signals and Data

Star topology with one timing ***Transmitter*** and multiple timing ***Repeaters*** & ***Receivers***

Timing data: synchronisation and machine-specific data transmitted continuously in frames at ~130.1 kHz. **Routed back** to transmitting module to measure & compensate the drift.



Transmitter, Repeaters and **Receivers** implemented as **MTCA.4 AMCs**

Repeaters & **Receivers** are distributed along the storage ring and beamlines

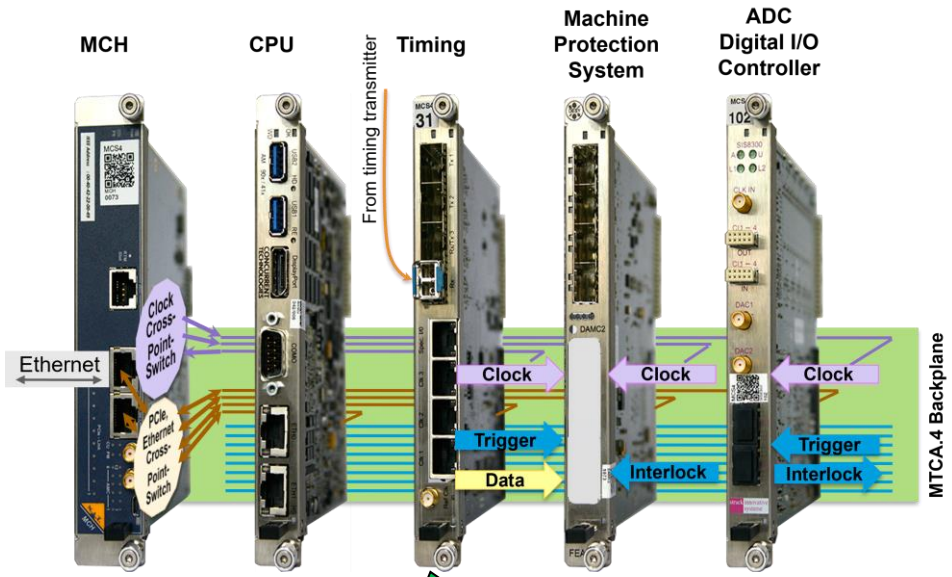
Each Repeater & Receiver
- recovers the **500 MHz RF Reference**
- decodes the **Timing** data from the input optical stream.

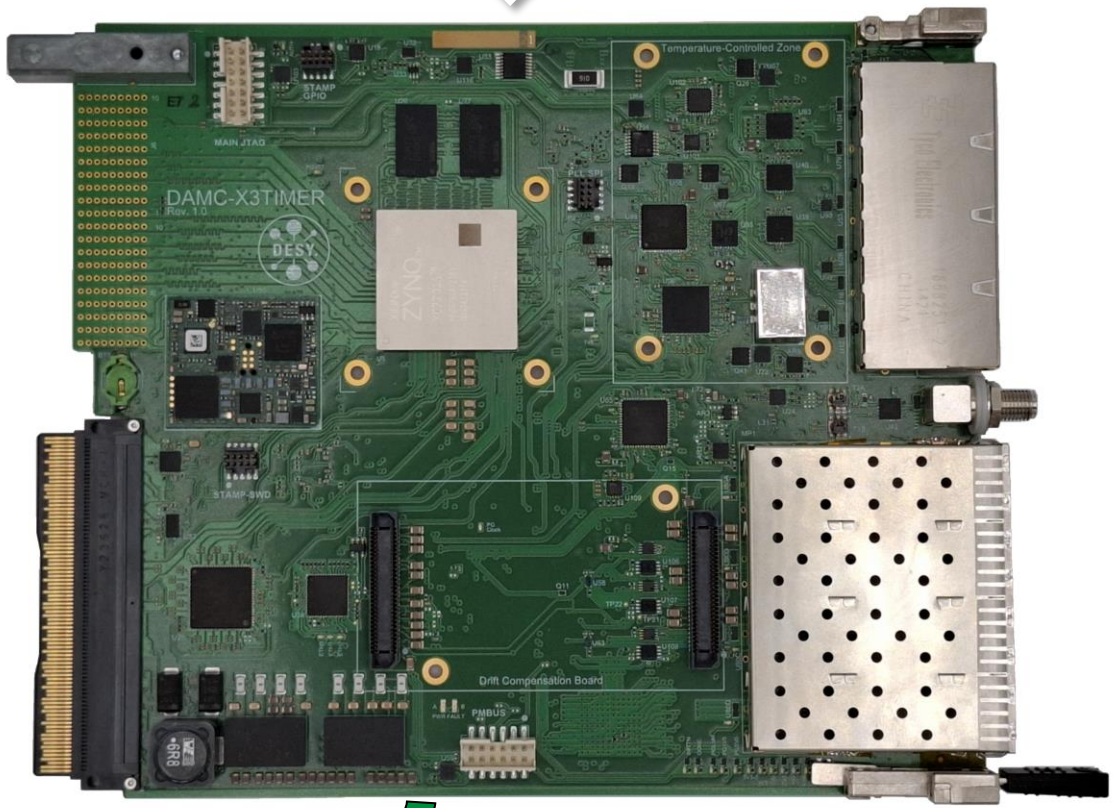
PETRA IV Timing System

DAMC-X3TIMER – Demonstrator

- **Based on** the concept & functionality of the **x2timer** timing module
- Improvements w.r.t. x2timer:
  - Clock jitter reduction
  - Better short- & long-term signal stability
  - Fine delay adjustment
  - Enhanced processing capabilities [Zynq SoC FPGA]
  - Modern AMC card management
  - etc.

Talk: Wed, 03.12, 11:15, Hendrik Lippek
"DAMC-X3TIMER Status Update"

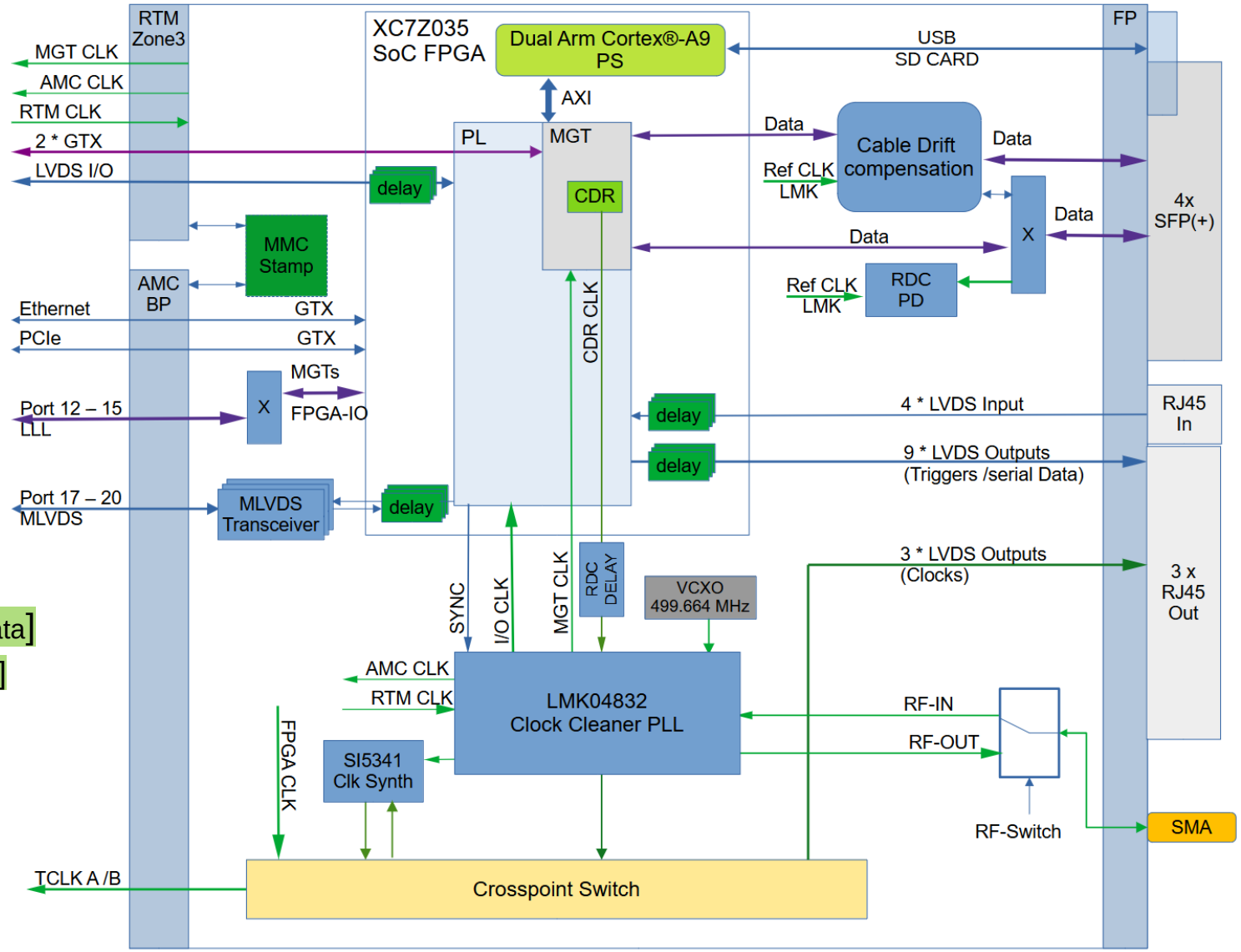




DAMC-X3TIMER Module

Main I/O Ports

- **Front Panel**
  - SFP(+) → timing data TX/RX
  - SMA → RF input/output
  - RJ45 → LVDS output [clocks, triggers, data]
  - RJ45 → LVDS input [ext. sync/triggers]
  - USB → debug/JTAG to MMC Stamp
  - SD-Card → aux. FW / SoC SW
- **AMC Backplane**
  - PCIe → communication to MTCA-CPU
  - Ethernet → access to Zynq PS
  - TCLK A/B → clock distribution
  - Ports 12-15 → low latency links [clocks, triggers, data]
  - Ports 17-20 → M-LVDS lanes [clocks, triggers, data]
  - IPMI to MMC → management, firmware update
- **RTM Zone 3 [Class D1.1]**
  - MGT Lanes → timing data distribution
  - LVDS → clocks, triggers, data
  - SPI / I2C → board configuration



PETRA IV Timing System

Machine-Specific Data to Local Clients

Channel A update rate ~130.2 kHz

"Timing Data" Frame [M/LVDS Link @ ~125 MHz]

7.68 µs – one PIV Revolution

16-bit Word Number	Bit Number 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
0	TIMING RX STATUS [7:0] | K28.5	Channel A
1	REVOLUTION NUMBER [15:0]	
2	REVOLUTION NUMBER [31:16]	
3	REVOLUTION NUMBER [47:32]	
4	MPS STATUS [7:0] | TIMING TRIGGERS [7:0]	
5	BEAM MODE [4:0] | MACHINE STATE [10:0]	
6	BEAM CURRENT DCCT@MPS [11:0] | B. MODE [8:5]	
7	BEAM CURRENT LIFETIME [10:0] | B.C. MPS [16:12]	
8	[9:8] | BEAM CURRENT LIFETIME [24:12]	
9	SPARE BITS [25:10]	
10	CRC-A [15:0]	
11	CRC-A [31:16]	
12	DATA BLOCK HEADER [15:0]	Channel B
13	DATA BLOCK HEADER [31:15]	
14	TIMING DATA [15:0]	
...	...	
45	TIMING DATA [511:496]	
46	CRC-B [15:0]	
47	CRC-B [31:16]	

Field	Width [bits]	Description
PAYLOAD	768	Timing Data (Channel A & B)
OVERHEAD	192	8b/10b overhead bits
FRAME LENGTH	960	Total number of bits per frame @~125 MHz

Serial interface @~125 MHz over M-LVDS [MTCA backplane] and/or LVDS cable [RJ45]

- REVOLUTION NUMBER [47:0]
- TIMING RX STATUS [7:0]
- TIMING TRIGGERS [7:0]
- MPS STATUS [7:0]
- S MACHINE STATE [9:0]
- S BEAM MODE [7:0]
- S BEAM CRT. DCCT@MPS [15:0]
- S BEAM CRT. LIFETIME [23:0]
- BUNCH PATTERN [3839:0] → update rate: ~18.3 kHz

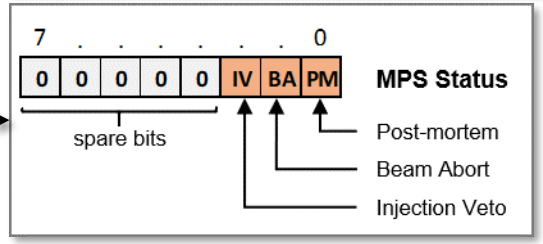
- 48-bit unique value → unambiguous tagging of recorded data
- provides the number of elapsed PIV revolutions since start of the project
- continuously generated in each timing module

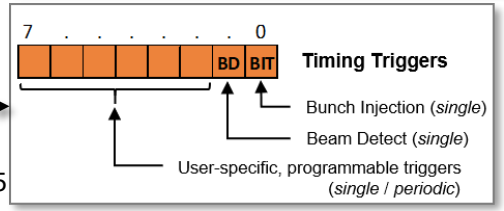
Period of operation	Num P4 turns (dec)	Num P4 turns (hex)
1 second	1,30208E+05	1 FCA0
1 day	1,12500E+10	2 9E8D 6080
1 (lap) year	4,11750E+12	3BE AE1F F700
10 (lap) years	4,11750E+13	2572 CD3F A600
40 (lap) years	1,64700E+14	95CB 34FE 9800
60 (lap) years	2,47050E+14	E0B0 CF7D E400

from Controls / MPS; format & content still to be defined

S = status flag → 1 = new data (in the given PIV turn)
→ 0 = unchanged data (w.r.t. previous PIV turn)

Bit Num	Description
0	Lost communication with the timing TX module
1	CRC error in Channel A (optical link TX → RX)
2	CRC error in Channel B (optical link TX → RX)
3-7	Not allocated (set permanently to zero)





Design in progress!

Summary

European XFEL Timing System (with x2timer AMC and RTM)

- In operation since 2017
- Provides:
  - 10ps RMS jitter and drift after 4 km
  - Triggers with delays and width (9.23ns resolution)
  - 3 channels with 5ps resolution on optional RTM
  - Wide range of phase-stable clocks
  - Reliable distribution of timing data and bunch patterns
  - Divider synchronisation with main repetition rate
  - 23 outputs on front panel, backplane & RTM backplane
  - User panels for complex output functions
- Timing server has more than 2200 properties
  [including 160 archived channels]
- Timing module designed by **DESY & Uni Stockholm**, available from **N.A.T.** as **NAMC-psTimer**

PETRA IV Timing System (with DAMC-X3TIMER)

- In development phase
  [PETRA IV start of operation planned for 2032]
- Based on concept and functionality of x2timer + improvements
  - Clock jitter
  - Short- & long-term stability
  - Fine delay
  - Zynq SoC FPGA, etc.
- Timing module demonstrator being tested
- Timing firmware & software being developed

Thank you!

Contact

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