

Rapid Hardware Integration with the ChimeraTK Software Framework

Martin Hierholzer

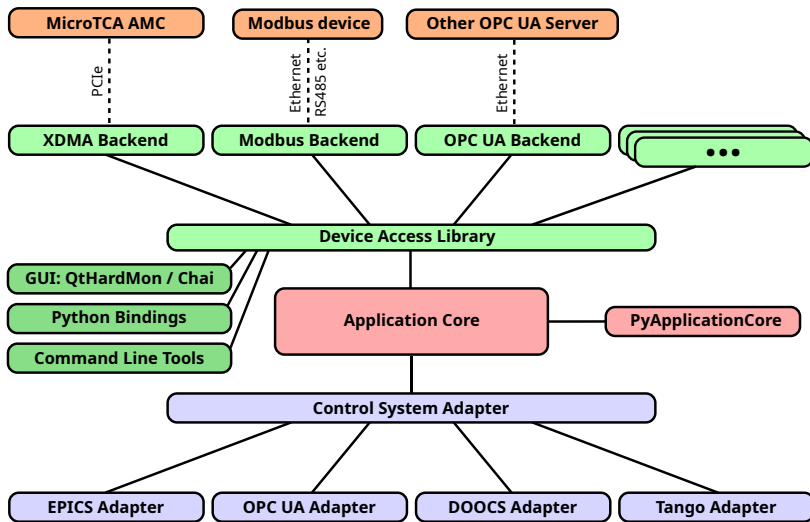
MicroTCA Workshop 2025, Hamburg,
2025-12-02

What is ChimeraTK?

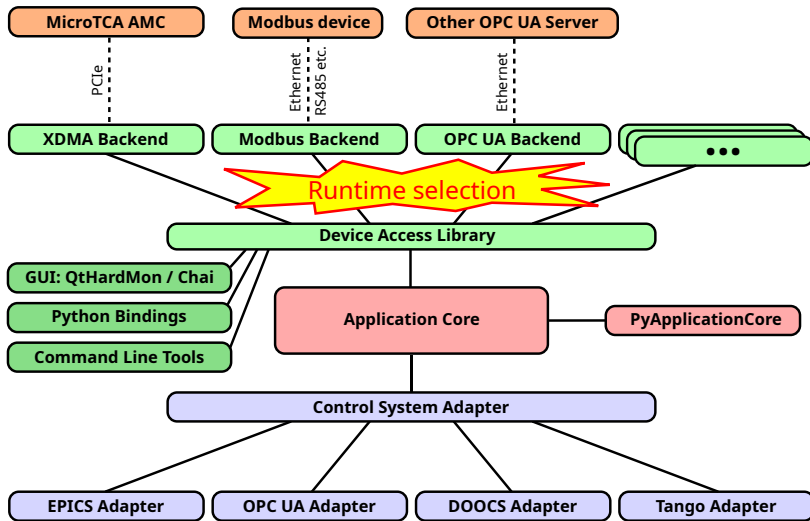


Control system and Hardware Interface with Mapped and
Extensible Register-based device Abstraction Tool Kit

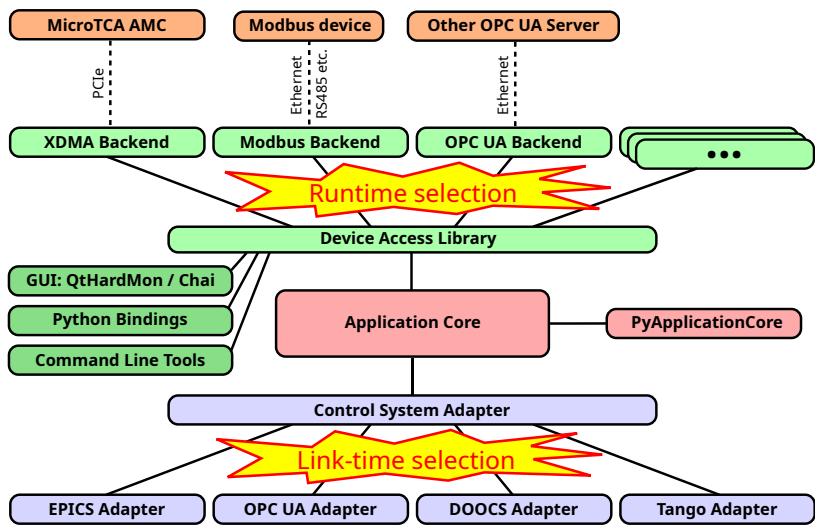
ChimeraTK overview



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ChimeraTK overview



ChimeraTK overview

- > ChimeraTK is a set of C++ libraries (with Python bindings) and stand-alone tools
- > Can interface with hardware through various protocols via “DeviceBackends”
- > Can interface with the rest of your control system through one of the “ControlSystemAdapters”

First contact

Let's talk to our hardware!

Assumptions

- > MicroTCA crate with MCH



Assumptions

- > MicroTCA crate with MCH



- > Some AMC board to talk to



Assumptions

- > MicroTCA crate with MCH



- > Some AMC board to talk to



- > FPGA firmware



Assumptions

> AMC CPU



> MicroTCA crate with MCH



> Some AMC board to talk to



> FPGA firmware



Assumptions

> AMC CPU



> MicroTCA crate with MCH



> Ubuntu 24.04



> Some AMC board to talk to



> FPGA firmware



Assumptions

> AMC CPU



> MicroTCA crate with MCH



> Ubuntu 24.04

Only example setup!

> None of these are mandatory requirements!

Ubuntu

> Some AMC board to talk to



> FPGA firmware



Setup Ubuntu Package Repository

- > For Ubuntu 24.04: Use DESY DOOCS package repository

```
wget -O - https://doocs-web.desy.de/pub/doocs/DOOCS-key.gpg.asc \
| sudo gpg --dearmor -o /etc/apt/trusted.gpg.d/doocs-keyring.gpg
sudo sh -c 'echo "deb https://doocs-web.desy.de/pub/doocs \
$(lsb_release -cs) main" > /etc/apt/sources.list.d/doocs.list'
sudo apt update
```

- > See “DOOCS installation manual” on <https://doocs.desy.de>

- > Install packages:

```
apt install qthardmon chimeratk-chai opcua-generic-chimeratk-server02
```

- > May also choose epics-generic-chimeratk-server02,
doocs-generic-chimeratk-server02 or tango-generic-chimeratk-server02

What you get from FWK firmware: the map file

Taken from SIS8300KU example design

@MAPFILE_REVISION 2.6.0-0-g1d930b9b

@![0,1] {"INTC" : {"path": "DAQ", "version":1} }

@![0,2] {"INTC" : {"path": "RTM", "version":1} }

@![0] {"INTC" : {"path": "APP", "version":1} }

@![1] {"INTC" : {"path": "TIMING", "version":1} }

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

BSP.ID	1	0x00000000	4	0	32	0	0	RO
ch0_top.BSP	19201	0x00000000	76804	0	32	0	0	RW
BSP.VERSION	1	0x00000004	4	0	32	0	0	RO
BSP.PRJ_ID	1	0x00000008	4	0	32	0	0	RO
BSP.PRJ_VERSION	1	0x0000000C	4	0	32	0	0	RO
BSP.PRJ_SHASUM	1	0x00000010	4	0	32	0	0	RO
BSP.PRJ_TIMESTAMP	1	0x00000014	4	0	32	0	0	RO
BSP.SCRATCH	1	0x00000018	4	0	32	0	0	RW
BSP.RESET_N	1	0x0000001C	4	0	1	0	0	RW
BSP.CLK_MUX	6	0x00000020	24	0	2	0	0	RW
BSP.CLK_SEL	1	0x00000038	4	0	1	0	0	RW
BSP.CLK_RST	1	0x0000003C	4	0	1	0	0	RW
BSP.CLK_FREQ	4	0x00000040	16	0	32	0	0	RO
BSP.CLK_ERR	1	0x00000050	4	0	2	0	0	RO

What you get from FWK firmware: the map file

Taken from SIS8300KU example design

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@![0] {"INTC" : {"path": "APP", "version":1} }
@![1] {"INTC" : {"path": "TIMING", "version":1} }
```

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

BSP.ID	1	0x00000000	4	0	32	0	0	RO
ch0_top.BSP	19201	0x00000000	76804	0	32	0	0	RW
BSP.VERSION	1	0x00000004	4	0	32	0	0	RO
BSP.PRJ_ID	1	0x00000008	4	0	32	0	0	RO
BSP.PRJ_VERSION	1	0x0000000C	4	0	32	0	0	RO
BSP.PRJ_SHASUM	1	0x00000010	4	0	32	0	0	RO
BSP.PRJ_TIMESTAMP	1	0x00000014	4	0	32	0	0	RO
BSP.SCRATCH	1	0x00000018	4	0	32	0	0	RW
BSP.RESET_N	1	0x0000001C	4	0	1	0	0	RW
BSP.CLK_MUX	6	0x00000020	24	0	2	0	0	RW
BSP.CLK_SEL	1	0x00000038	4	0	1	0	0	RW
BSP.CLK_RST	1	0x0000003C	4	0	1	0	0	RW
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What you get from FWK firmware: the map file

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```
@![0,1] {"INTC" : {"path": "DAQ", "version":1} }  
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@![0] {"INTC" : {"path": "APP", "version":1} }  
@![1] {"INTC" : {"path": "TIMING", "version":1} }
```

interrupt definition

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

BSP.ID	1	0x00000000	4	0	32	0	0	RO
ch0_top.BSP	19201	0x00000000	76804	0	32	0	0	RW
BSP.VERSION	1	0x00000004	4	0	32	0	0	RO
BSP.PRJ_ID	1	0x00000008	4	0	32	0	0	RO
BSP.PRJ_VERSION	1	0x0000000C	4	0	32	0	0	RO
BSP.PRJ_SHASUM	1	0x00000010	4	0	32	0	0	RO
BSP.PRJ_TIMESTAMP	1	0x00000014	4	0	32	0	0	RO
BSP.SCRATCH	1	0x00000018	4	0	32	0	0	RW
BSP.RESET_N	1	0x0000001C	4	0	1	0	0	RW
BSP.CLK_MUX	6	0x00000020	24	0	2	0	0	RW
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interrupt definition

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APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

BSP.ID	1	0x00000000	4	0	32	0	0	RO
ch0_top.BSP	19201	0x00000000	76804	0	32	0	0	RW
BSP.VERSION	1	0x00000004	4	0	32	0	0	RO
BSP.PRJ_ID	1	0x00000008	4	0	32	0	0	RO
BSP.PRJ_VERSION	1	0x0000000C	4	0	32	0	0	RO
BSP.PRJ_SHASUM	1	0x00000010	4	0	32	0	0	RO
BSP.PRJ_TIMESTAMP	1	0x00000014	4	0	32	0	0	RO
BSP.SCRATCH	1	0x00000018	4	0	32	0	0	RW
BSP.RESET_N	1	0x0000001C	4	0	1	0	0	RW
BSP.CLK_MUX	6	0x00000020	24	0	2	0	0	RW
BSP.CLK_SEL	1	0x00000038	4	0	1	0	0	RW
BSP.CLK_RST	1	0x0000003C	4	0	1	0	0	RW
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BSP.CLK_ERR	1	0x00000050	4	0	2	0	0	RO

register name

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@![0,2] {"INTC" : {"path": "RTM", "version":1} }  
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```

interrupt definition

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

```
BSP.ID  
ch0_top.BSP  
BSP.VERSION  
BSP.PRJ_ID  
BSP.PRJ_VERSION  
BSP.PRJ_SHASUM  
BSP.PRJ_TIMESTAMP  
BSP.SCRATCH  
BSP.RESET_N  
BSP.CLK_MUX  
BSP.CLK_SEL  
BSP.CLK_RST  
BSP.CLK_FREQ  
BSP.CLK_ERR
```

register name

1	0x00000000
19201	0x00000000
1	0x00000004
1	0x00000008
1	0x0000000C
1	0x00000010
1	0x00000014
1	0x00000018
1	0x0000001C
6	0x00000020
1	0x00000038
1	0x0000003C
4	0x00000040
1	0x00000050

nb. of elements

4	0	32	0	0	RO
76804	0	32	0	0	RW
4	0	32	0	0	RO
4	0	32	0	0	RO
4	0	32	0	0	RO
4	0	32	0	0	RO
4	0	32	0	0	RO
4	0	32	0	0	RW
4	0	1	0	0	RW
24	0	2	0	0	RW
4	0	1	0	0	RW
4	0	1	0	0	RW
16	0	32	0	0	RO
4	0	2	0	0	RO

nb. of bytes

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```
@![0,1] {"INTC" : {"path": "DAQ", "version":1} }
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interrupt definition

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

```
BSP.ID
ch0_top.BSP
BSP.VERSION
BSP.PRJ_ID
BSP.PRJ_VERSION
BSP.PRJ_SHASUM
BSP.PRJ_TIMESTAMP
BSP.SCRATCH
BSP.RESET_N
BSP.CLK_MUX
BSP.CLK_SEL
BSP.CLK_RST
BSP.CLK_FREQ
BSP.CLK_ERR
```

register name

1	0x00000000	4	0	32	0	0	RO
19201	0x00000000	76804	0	32	0	0	RW
1	0x00000004	4	0	32	0	0	RO
1	0x00000008	4	0	32	0	0	RO
1	0x0000000C	4	0	32	0	0	RO
1	0x00000010	4	0	32	0	0	RO
1	0x00000014	4	0	32	0	0	RO
1	0x00000018	4	0	32	0	0	RW
1	0x0000001C	4	0	1	0	0	RW
6	0x00000020	24	0	2	0	0	RW
1	0x00000038	4	0	1	0	0	RW
1	0x0000003C	4	0	1	0	0	RW
4	0x00000040	16	0	32	0	0	RO
1	0x00000050	4	0	2	0	0	RO

nb. of elements address nb. of bytes BAR

What you get from FWK firmware: the map file

Taken from SIS8300KU example design

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```
@![0,1] {"INTC" : {"path": "DAQ", "version":1} }
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```

interrupt definition

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

```
BSP.ID
ch0_top.BSP
BSP.VERSION
BSP.PRJ_ID
BSP.PRJ_VERSION
BSP.PRJ_SHASUM
BSP.PRJ_TIMESTAMP
BSP.SCRATCH
BSP.RESET_N
BSP.CLK_MUX
BSP.CLK_SEL
BSP.CLK_RST
BSP.CLK_FREQ
BSP.CLK_ERR
```

register name

1	0x00000000	4	0	32	0	0	RO
19201	0x00000000	76804	0	32	0	0	RW
1	0x00000004	4	0	32	0	0	RO
1	0x00000008	4	0	32	0	0	RO
1	0x0000000C	4	0	32	0	0	RO
1	0x00000010	4	0	32	0	0	RO
1	0x00000014	4	0	32	0	0	RO
1	0x00000018	4	0	32	0	0	RW
1	0x0000001C	4	0	1	0	0	RW
6	0x00000020	24	0	2	0	0	RW
1	0x00000038	4	0	1	0	0	RW
1	0x0000003C	4	0	1	0	0	RW
4	0x00000040	16	0	32	0	0	RO
1	0x00000050	4	0	2	0	0	RO

nb. of elements address nb. of bytes BAR fixed point info

What you get from FWK firmware: the map file

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```
@![0,1] {"INTC" : {"path": "DAQ", "version":1} }
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```

interrupt definition

APP.ISR.TRIGGER	0	0x00000000	0	0	0	0	0	INTERRUPT0:0
APP.ISR.DAQ	0	0x00000000	0	0	0	0	0	INTERRUPT0:1
DAQ.ISR.START	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:0
DAQ.ISR.DONE	0	0x00000000	0	0	0	0	0	INTERRUPT0:1:1

```
BSP.ID
ch0_top.BSP
BSP.VERSION
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BSP.RESET_N
BSP.CLK_MUX
BSP.CLK_SEL
BSP.CLK_RST
BSP.CLK_FREQ
BSP.CLK_ERR
```

register name

1	0x00000000
19201	0x00000000
1	0x00000004
1	0x00000008
1	0x0000000C
1	0x00000010
1	0x00000014
1	0x00000018
1	0x0000001C
6	0x00000020
1	0x00000038
1	0x0000003C
4	0x00000040
1	0x00000050

nb. of elements

4
76804
4
4
4
4
4
4
4
24
4
4
16
4

nb. of bytes

0
0
0
0
0
0
0
0
0
0
0
0
0
0

BAR

32	0	0
32	0	0
32	0	0
32	0	0
32	0	0
32	0	0
32	0	0
32	0	0
1	0	0
2	0	0
1	0	0
1	0	0
32	0	0
2	0	0

fixed point info

RO
RW
RO
RO
RO
RO
RO
RW
RW
RW
RW
RO
RO

access

Define your devices

... by writing a DMAP file

```
MyAMC      (xdma:xdma/slot6?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot8      (xdma:xdma/slot8?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot7      (xdma:xdma/slot7?map=some_other_map_file.mapp)
OPCUADev   (opcua:127.0.0.1?port=16664)
```

Define your devices

... by writing a DMAP file

MyAMC	(xdma:xdma/slot6?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot8	(xdma:xdma/slot8?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot7	(xdma:xdma/slot7?map=some_other_map_file.mapp)
OPCUADev	(opcua:127.0.0.1?port=16664)
alias name	

Define your devices

... by writing a DMAP file

MyAMC	(xdma:xdma/slot6?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot8	(xdma:xdma/slot8?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot7	(xdma:xdma/slot7?map=some_other_map_file.mapp)
OPCUADev	(opcua:127.0.0.1?port=16664)
alias name	ChimeraTK Device Descriptor

> ChimeraTK Device Descriptor (CDD):

- (backend_type:address?key1=value1&key2=value2)
- CDD can be part of another CDD as a parameter value

Define your devices

... by writing a DMAP file

MyAMC	(xdma:xdma/slot6?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot8	(xdma:xdma/slot8?map=sis8300ku_example_design_dwc10_2.6.0-0-g1d930b9b.mapp)
Slot7	(xdma:xdma/slot7?map=some_other_map_file.mapp)
OPCUADev	(opcua:127.0.0.1?port=16664)
alias name	ChimeraTK Device Descriptor

map file names

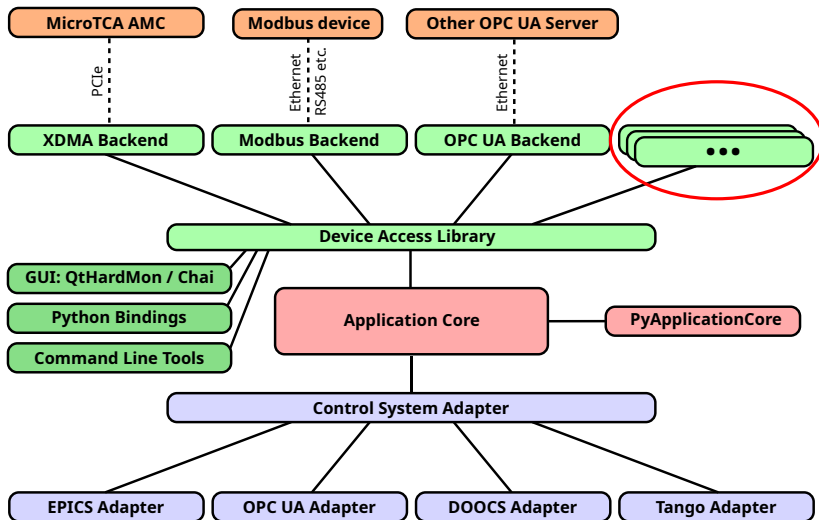
> ChimeraTK Device Descriptor (CDD):

- (backend_type:address?key1=value1&key2=value2)
- CDD can be part of another CDD as a parameter value

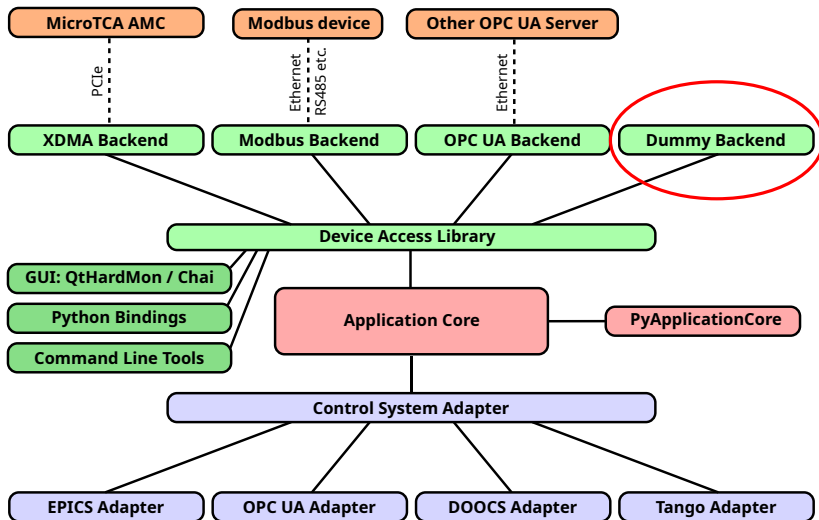
Live demo

- > Show map file used throughout the demo
- > QtHardMon and Chai
- > Show dmap file

Dummy backend



Dummy backend



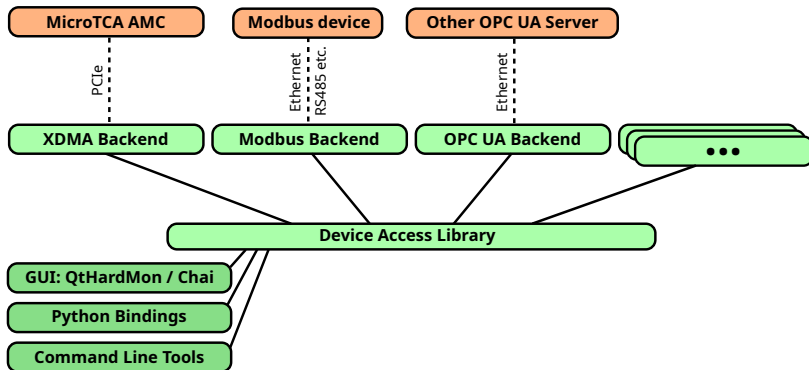
Live demo

- > Simulate hardware/firmware with second Chai

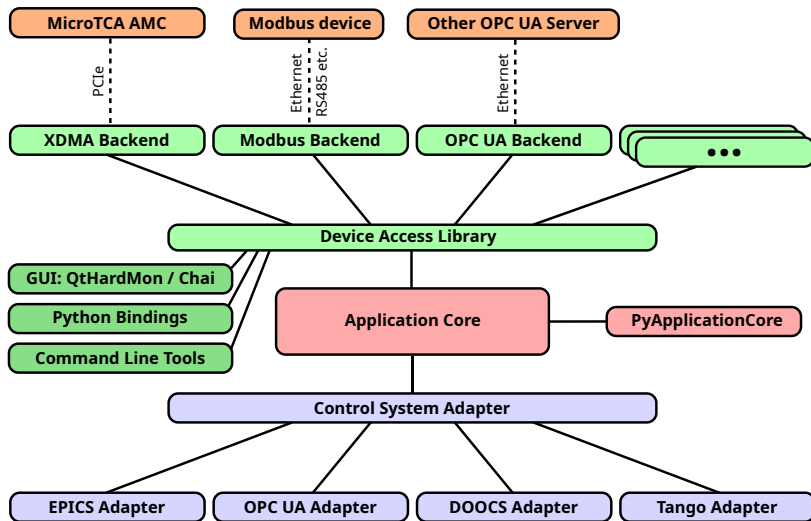
Integrate with your control system

using the GenericDeviceServer

ApplicationCore and the GenericDeviceServer



ApplicationCore and the GenericDeviceServer



ApplicationCore and the GenericDeviceServer

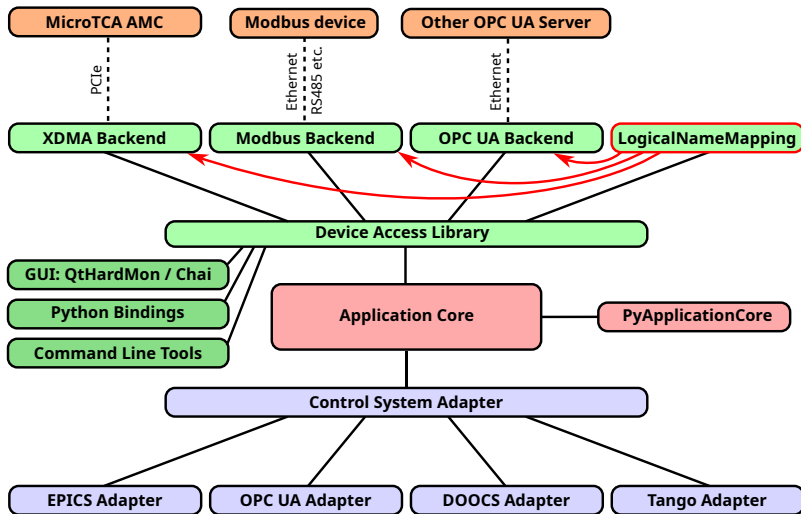
- > GenericDeviceServer is ready-to-use ApplicationCore executable
- > Linked against any of the adapter (EPICS, OPC UA, DOOCS, Tango)
- > Will expose registers from devices to control system
- > Configuration: which devices to expose and how
- > No C++ or Python code needs to be written!

Live demo

- > GenericDeviceServer configuration
- > “Replace” first Chai with GenericDeviceServer
- > Introduce logical name mapping

Logical Name Mapping backend

A meta-backend targeting any backend type



Logical name mapping

- > Filter out registers not to be exposed
- > Rename registers
- > Extract array elements
- > Extract individual bits and bit ranges
- > Apply (simple) math transformations
- > ... and many more things!

Documentation:

<https://chimeratk.github.io/ChimeraTK-DeviceAccess/head/html/lmap.html>.

Common task: expose bits of bit field

 FPGA Firmware Documentation

BSP for SIS8300-KU board

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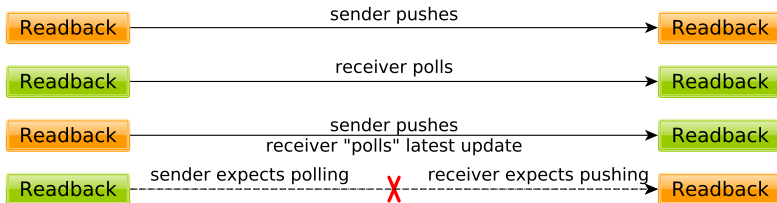
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```
} BOOT_STATUS;  
  
reg {  
  desc = "MGT reference clock PLL control register [br]  
    0: start PLL configuration at rising edge [br]  
    1: reset PLL fsm at rising edge [br]  
    2: clear PLL interrupt at rising edge [br]  
    Note: One-Hot (or all '0') entry should be used for this register";  
  default sw = rw;  
  default hw = r;  
  default swmod;  
  field {} data[3];  
} MGT_PLL_CONTROL;  
  
reg {  
  desc = "MGT reference clock PLL status register [br]  
    0: active high indicator for PLL configuration DONE [br]  
    1: active high indicator for PLL I2C interface BUSY [br]  
    2: active high indicator for sticky PLL interrupt";  
  default sw = r;  
  default hw = rw;  
  field {} data [3];  
} MGT_PLL_STATUS;
```

Live demo

- > Logical name mapping:
 - Single bit access
 - Math plugin

Triggering scheme and interrupts



- > Normal registers are passive:
 - read: poll-type
 - write: push-type
- > Hardware interrupt: push-type (but no data: void-type)
- > Map file can specify registers to poll on interrupt
- > Interrupt can be used as readout trigger

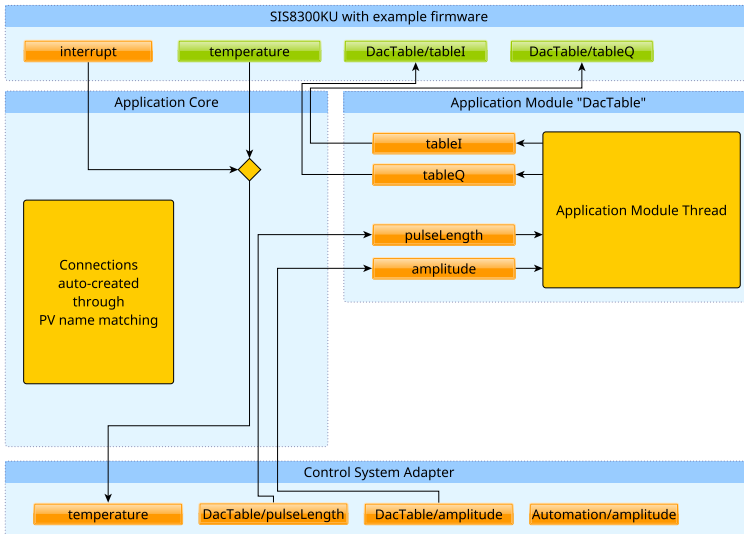
Live demo

- > Interrupts as push-type variables
- > Interrupts as trigger for polling

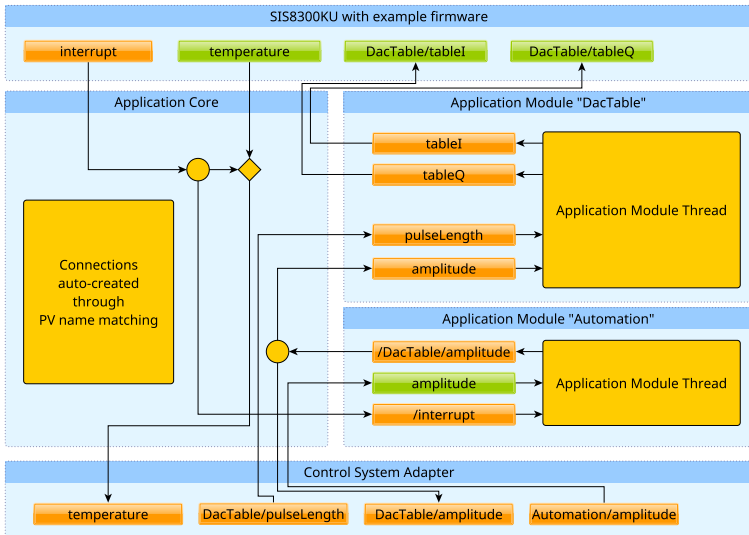
Adding complex application logic

with PyApplicationCore

ApplicationCore modularity



ApplicationCore modularity

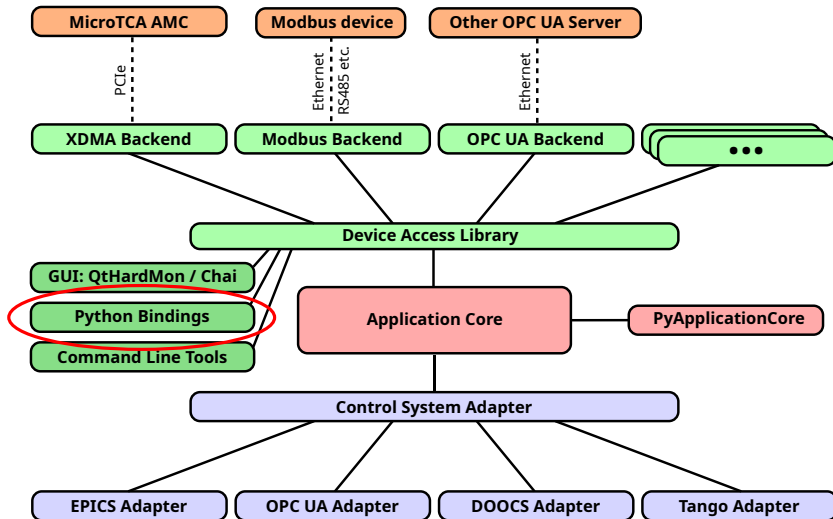


Live demo

- > Source code of Python module
- > Inject errors:
 - Python exception (use undefined variable)
 - Data type mismatch
 - PV name mismatch
- > Add second Python module (modules shall be small, so use many!)

Device initialisation

DeviceAccess Python bindings



Live demo

- > Python script with *DeviceAccess* Python bindings
- > Add script to GenericDeviceServer configuration

Summary and Close-out

Things we did NOT talk about

- > Control system specific configuration:
 - Each ControlSystemAdapter (OPC UA, EPICS, TANGO, DOOCS) has specific config file format
 - Allows to rename variables (e.g. to re-use application in different context)
 - Control specific features like history, special data types etc.
- > Target non-MicroTCA hardware with other backends:
 - available for many industry standards like OPC UA, Modbus, SCPI
- > Integrate SPI/I2C/... attached hardware with SubDeviceBackend
 - will have its own map file
 - several protocols supported (register layout in primary map file from FWK)
- > Write ApplicationModules in C++
 - very similar to PyApplicationCore
 - recommended for maximum stability

Summary

- > ChimeraTK framework for hardware access and control system interface
- > GenericDeviceServer publishes device to control system
- > Dummy backend for easy development on desktop PC
- > Logical name mapping to select what to publish and how
- > PyApplicationCore: implement application logic in Python
 - Modular approach: use many small ApplicationModules
 - Connect to registers and control system variables by (fully-qualified) name
- > DeviceAccess Python bindings: device initialisation

Thank you!

- > Live demo files: <https://github.com/mhier/ApplicationCoreLiveDemo>
- > ChimeraTK documentation: <https://chimeratk.github.io>
- > FWK documentation: <https://fpgafw.pages.desy.de/docs-pub/fw/main>

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