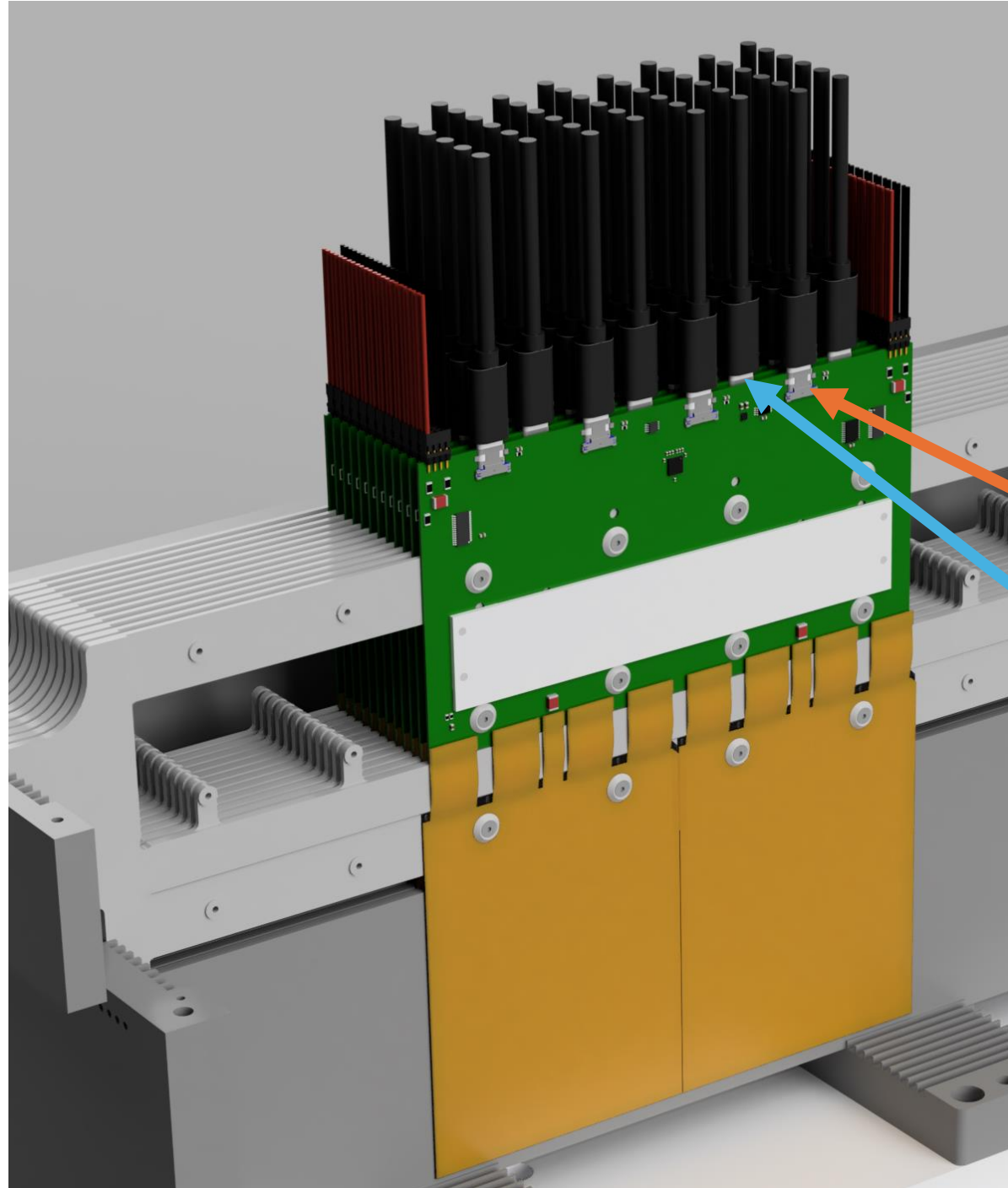
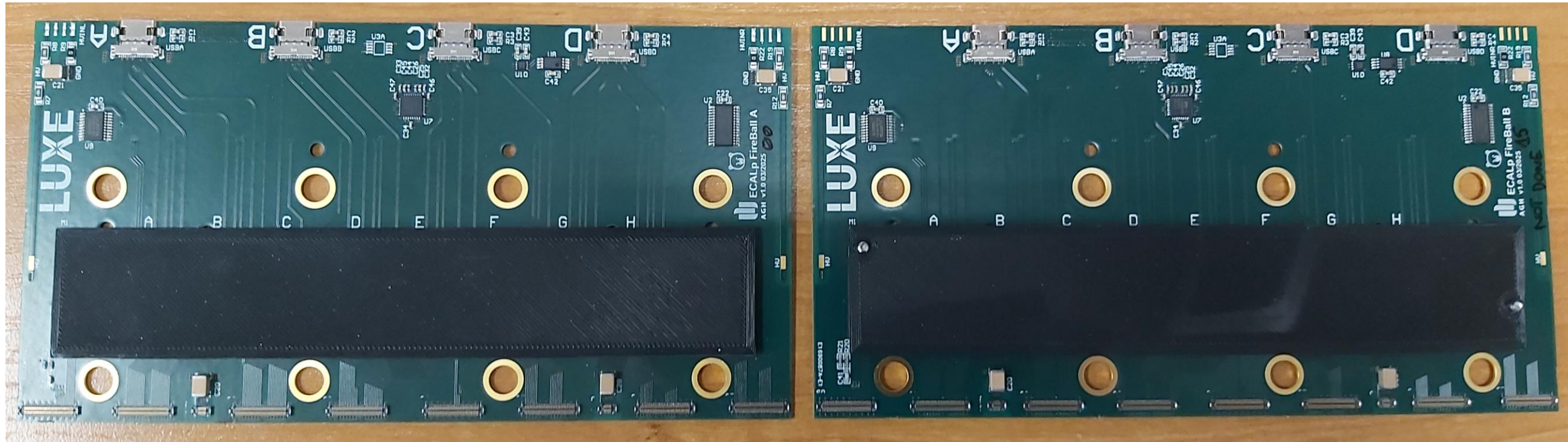


FLAME-based ECAL-p readout status

- Rack:
 - **Backplane: 3 pcs ready** (2 + 1 spare)
 - **Synchronization card: 3 pcs ready** (2+ 1 spare)
- FPGA:
 - **Rack cards: 12 pcs ready** (10 + 2 spares)
 - **Trenz FPGA modules: 12 pcs ready** with heatsinks (10 + 2 spares)
- FEBs:
 - **Type “A”** (see next slide): **8 pcs** (almost) **ready** (5 + 3 spares)
 - **Type “B”**: **6 pcs** (almost) **ready** (5 + 1 spare) and:
 - One with one ASIC dead (but on the edge of the sensor)
 - One with ASICs glued, but not wirebonded (we run out of bonding wire)
 - *Przemek managed to wirebond 7 FEBs in less than 3 days (usually it would take ~8-9 days (more than 1000 wirebonds per FEB...))*
He is now in hospital, should return on begin of June. If all will go well, we should have all 8 FEBs type “B” ready before 9th of June...



- USB-C cables, used for FLAME data transmission are too thick to fit into 4.7mm
- Solution: cables staggered (shifted) between layers:
 - Even layers – cables shifted to the left
 - Odd layers – cables shifted to the right
- Apart from USB-C sockets position, FEBs “A” and “B” are identical



FEB “A” (sockets shifted left)

FEB “B” (sockets shifted right)

- There is no assignment of “A” or “B” to odd or even layer. The boards should simply be placed alternately.
- Missing parts:
 - HV connectors (we have parts, just needs to be soldered)
 - HV capacitors too thick – we have thinner, needs to be replaced (miscommunication with assembly company)
 - Aluminum, thin ASIC covers (made by Warsaw) in place of 3D-printed (black) ones

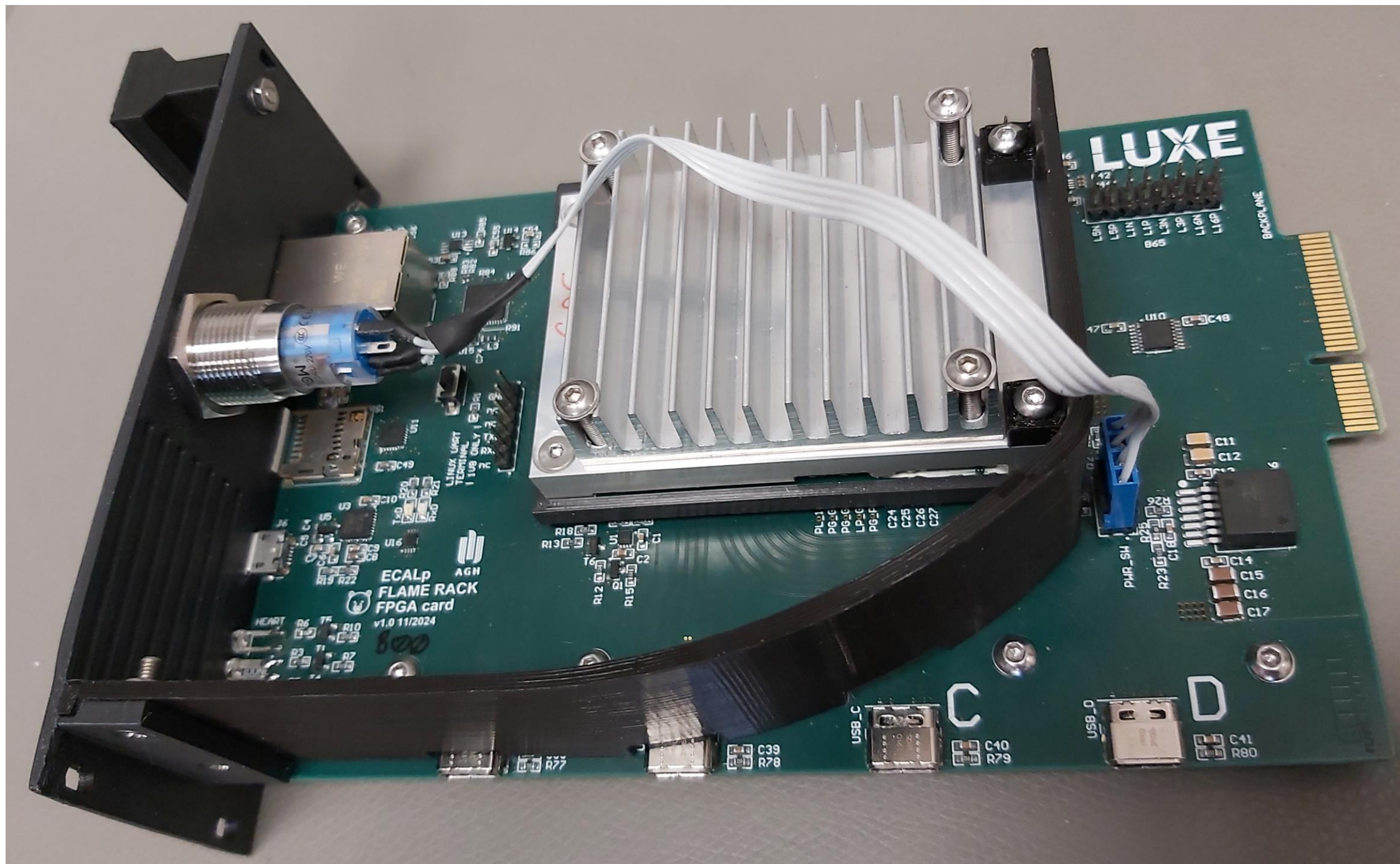
Channel numbering - hardware

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15				A0	0	2	4	6	8	10	1	3	5	7	9	11
14				A4	4	6	8	10	12	14	16	18	20	22	24	26
13			A3	A4	12	14	16	18	20	22	24	26	28	30	0	2
12				A4	5	7	9	11	13	15	17	19	21	23	25	27
11			A3	A4	13	15	17	19	21	23	25	27	29	31	1	3
10			A2	A3	20	22	24	26	28	30	0	2	4	6	8	10
9			A1	A2	28	30	0	2	4	6	8	10	12	14	16	18
8			A2	A3	21	23	25	27	29	31	1	3	5	7	9	11
7			A1	A2	29	31	1	3	5	7	9	11	13	15	17	19
6				A1	4	6	8	10	12	14	16	18	20	22	24	26
5			A0	A1	12	14	16	18	20	22	24	26	28	30	0	2
4				A1	5	7	9	11	13	15	17	19	21	23	25	27
3			A0	A1	13	15	17	19	21	23	25	27	29	31	1	3
2																
1																
0																

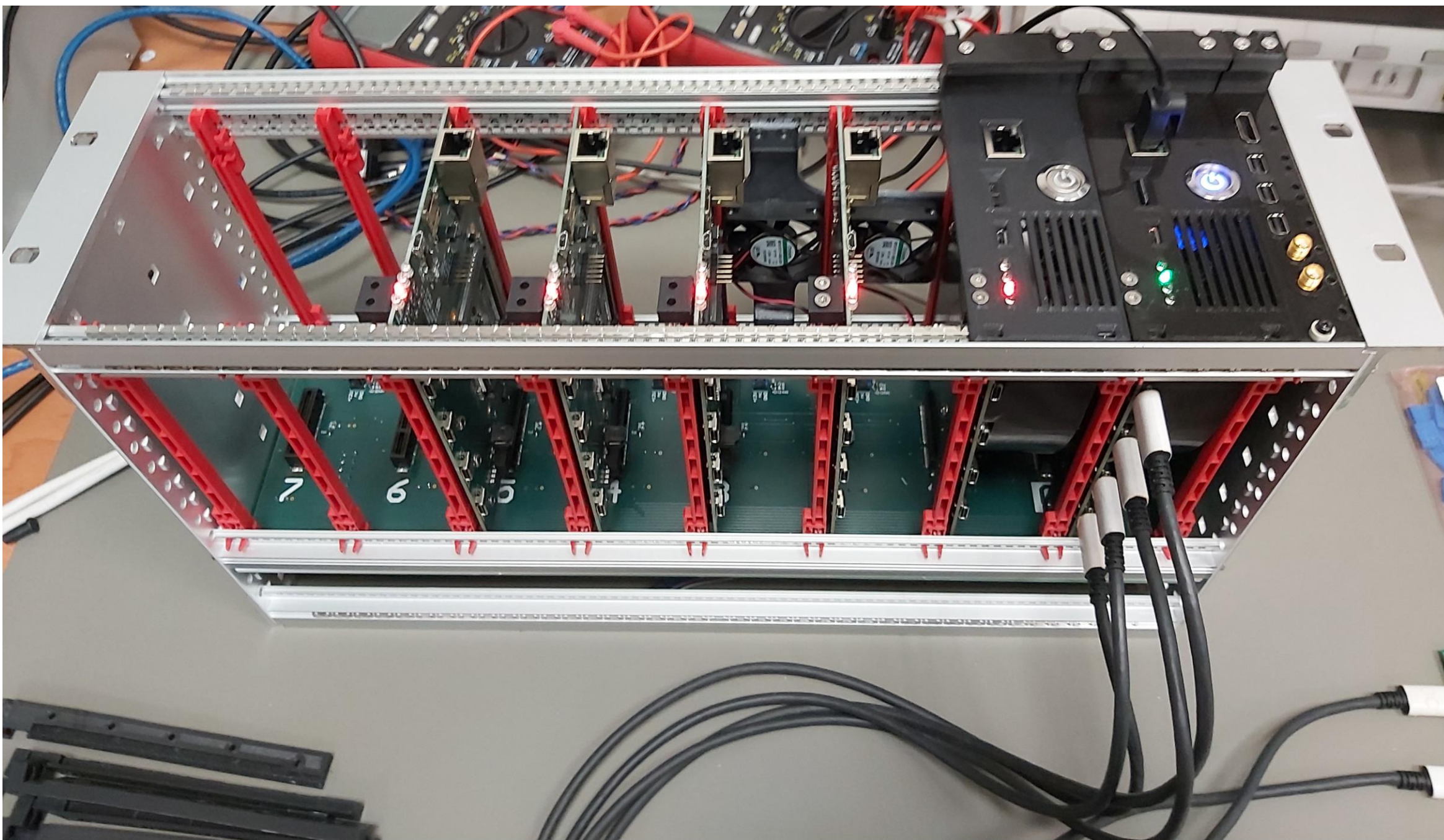
0	1	2	3	4	5	6	7	8	9
29	31	28	30					A4	
16	18	20	22	24	26	28	30	A7	
0	2	4	6	8	10	12	14	A7	
17	19	21	23	25	27	29	31	A7	
1	3	5	7	9	11	13	15	A7	
16	18	20	22	24	26	28	30	A6	
0	2	4	6	8	10	12	14	A6	
17	19	21	23	25	27	29	31	A6	
1	3	5	7	9	11	13	15	A6	
16	18	20	22	24	26	28	30	A5	
0	2	4	6	8	10	12	14	A5	
17	19	21	23	25	27	29	31	A5	
1	3	5	7	9	11	13	15	A5	

	Left sensor column															Right sensor column																			
Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
15					240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255															
14					220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235												236	237	238	239
13					200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215												216	217	218	219
12					180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195												196	197	198	199
11					160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175												176	177	178	179
10					140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155												156	157	158	159
9					120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135												136	137	138	139
8					100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115												116	117	118	119
7					80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95												96	97	98	99
6					60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75												76	77	78	79
5					40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55												56	57	58	59
4					20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35												36	37	38	39
3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19															
2																																			
1																																			
0																																			

FPGA card



Rack with FPGA cards



- Firmware:
Finally seems ready (not yet fully tested)
First correct data package received just minutes ago...
- Middleware (software for FPGA): in progress (first version hopefully till the end of this week)
- Software:
 - EUDAQ producer ready for tests (done by our student, Arek)
 - Online monitoring well advanced (done by Dawid)
 - DAQ control GUI (also website) in progress (by Dawid)
 - Arek and Dawid are now working on merging producer with monitoring and control GUI
- We hope to start full integration tests (FPGA + EUDAQ producer) next week

- HDDs: currently 4 x 4 TB, I asked Yan to buy/borrow 4 x 16 TB for testbeam
- 10 Gbps ethernet card – borrowed from our IT department
 - A variety of fiber cables (10m, 20m, 30m, 50m) bought
- 4x 1 Gbps backup ethernet card ready (EUDAQ producer can work with both)
 - A lot of 1 Gbps cables, varies lengths, bought
- Not done yet (parts ready):
 - LV cables for racks
 - HV cables
 - **We do not have yet the HV power supply!** (*who is responsible for it?*)
- Open question: mechanical integration?
Grzegorz, Filip – how do we want to proceed?