



<https://www.desy.de/>

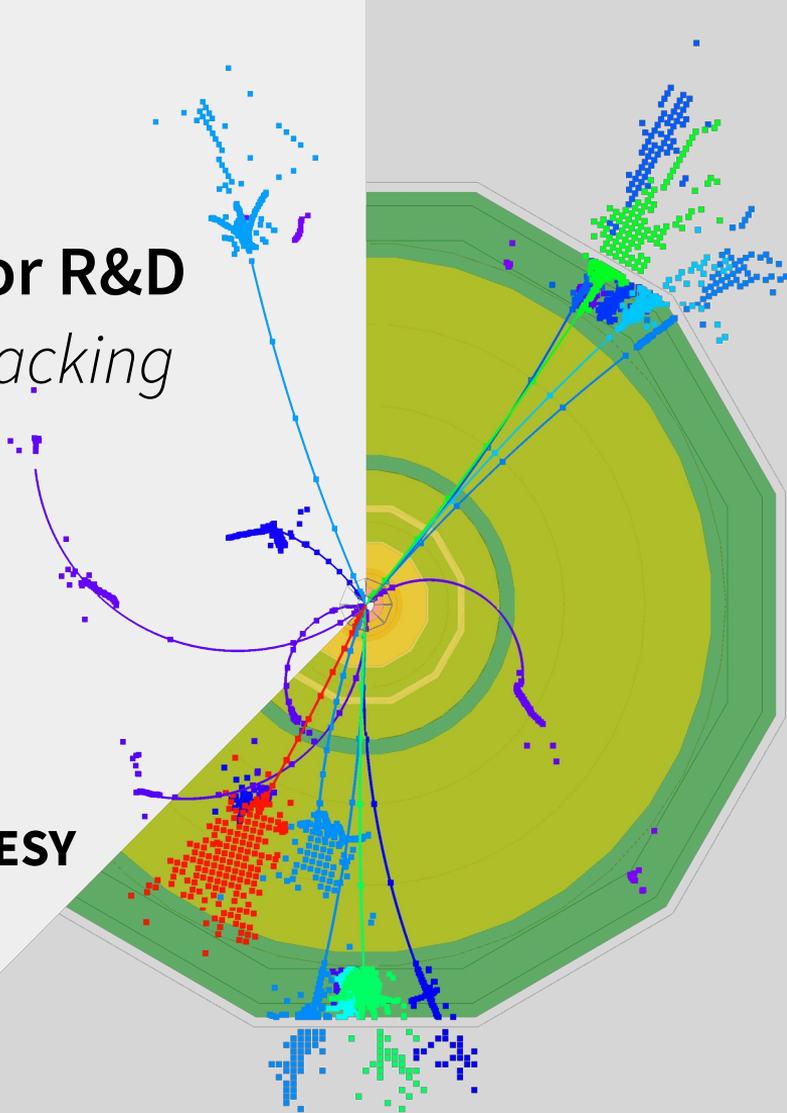
Semiconductor Detector R&D

*A Vision for Vertexing & Tracking
at Future Colliders*

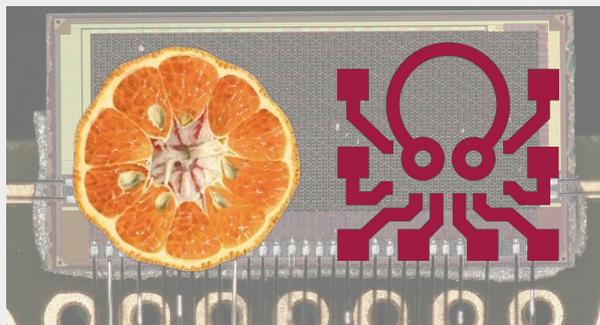
Simon Spannagel, DESY

DESY Detector Retreat

16 June 2025



Many Detector Prototypes, Concepts & Tools



Next-gen High-precision Tracking Detectors

TANGERINE & OCTOPUS



Semiconductor MC simulations

Allpix Squared



Control & DAQ for Small Setups

Constellation



Track Reco at Test Beams

Corryvreckan



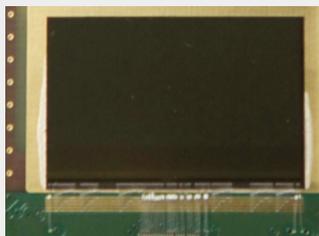
High-Bandwidth Data Transmission

SOPHIE



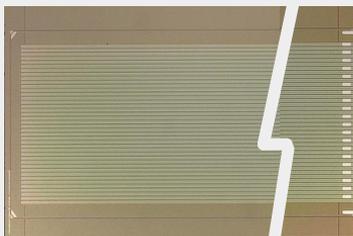
Pixels w/ Picosecond Time Resolution

Monolithic Digital SiPM



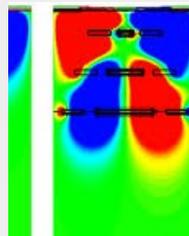
Flexible region-of-interest trigger

TelePix2 HV-MAPS



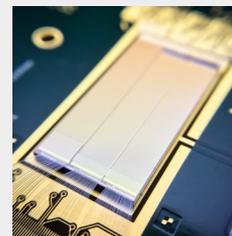
Cost-effective large-area instrumentat.

CMOS Strip Sensors



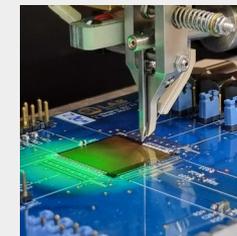
Enhancing Resolution

ELAD



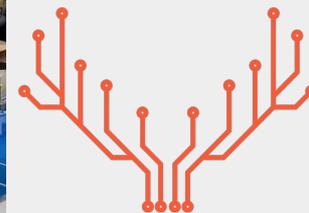
Collaboration with DESY-AP

AstroPix



Possib. Belle II VTX Upgrade

OBELIX / TJMp2



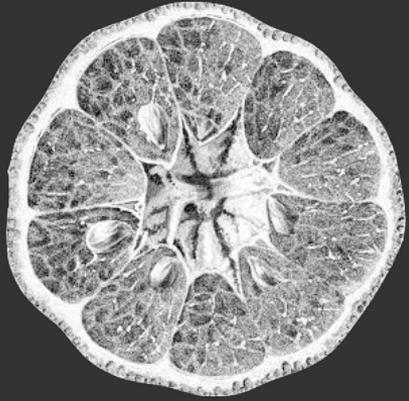
Flexible DAQ for Prototypes

Caribou

Vertex Detector Requirements at Lepton Colliders

- Precision measurements very demanding on vertex detectors
 - Impact parameter resolution: high resolution, min. scattering, small radii
 - Time resolution : fast sensor response, large S/N
 - Heat dissipation: low power consumption

	Lepton Colliders		(HL-) LHC (ATLAS/CMS)
Material budget	$< 1\% X_0$		10% X_0
Single-point resolution	$\leq 3 \mu\text{m}$		$\sim 15\mu\text{m}$
Time resolution	$\sim \text{ns}$		25ns
Granularity	$\leq 25 \mu\text{m} \times 25 \mu\text{m}$		50 $\mu\text{m} \times 50\mu\text{m}$
Radiation tolerance	$< 10^{11} n_{\text{eq}} / \text{cm}^2$		$O(10^{16} n_{\text{eq}} / \text{cm}^2)$
Duty cycle	$< 0.01 \text{ ‰ @ } \sim\text{ms (linear)}$	100 % @ $\sim\text{ns (circular)}$	100 % @ 25ns



Tangerine

Towards next generation silicon detectors
A Helmholtz Innovation Pool Project



The Tangerine Project

Towards the Next Generation of Silicon Detectors



Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass [...] To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial.

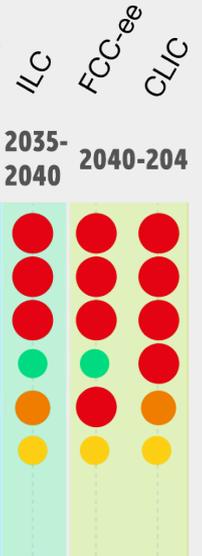
ECFA Detector R&D Roadmap, Research Goal DRDT 3.1

- Explore MAPS technologies as candidates for **vertex detector sensors at future lepton colliders**
- Develop **simulation approach for MAPS** to allow predictive studies on sensor layouts
- **Design & characterize prototypes** with fast front-ends and full digital integration

ECFA DRD Roadmap, 2020

Vertex detector²⁾

	DRDT
Position precision	3.1,3.4
Low X/X_0	3.1,3.4
Low power	3.1,3.4
High rates	3.1,3.4
Large area wafers ³⁾	3.1,3.4
Ultrafast timing ⁴⁾	3.2
Radiation tolerance NIEL	3.3
Radiation tolerance TID	3.3

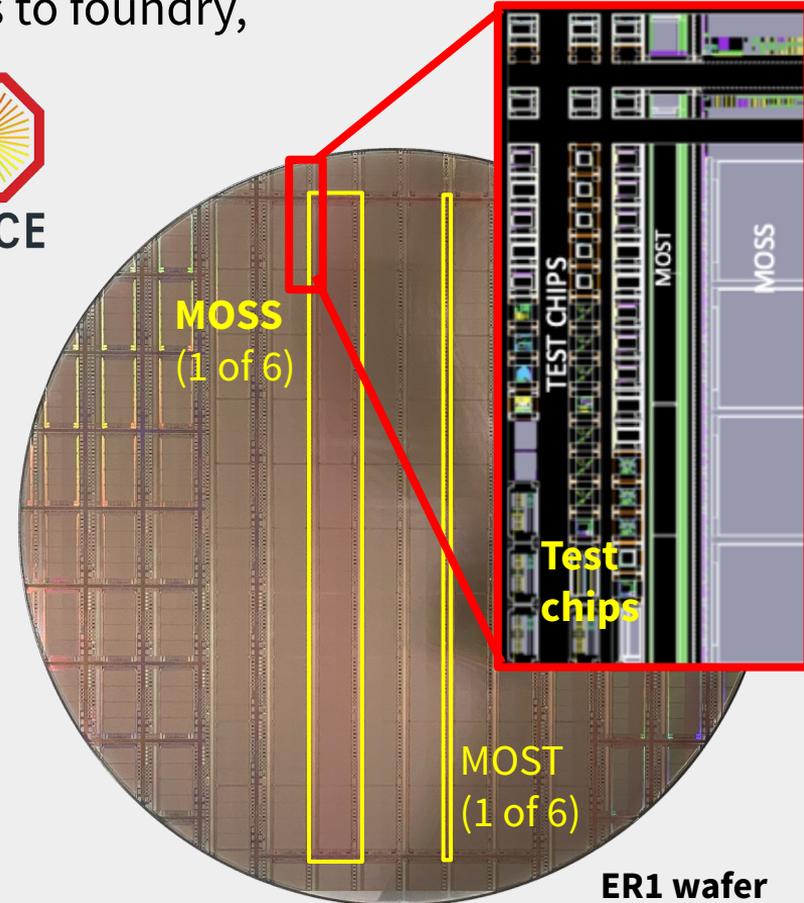


Technology: 65nm CMOS Imaging Process

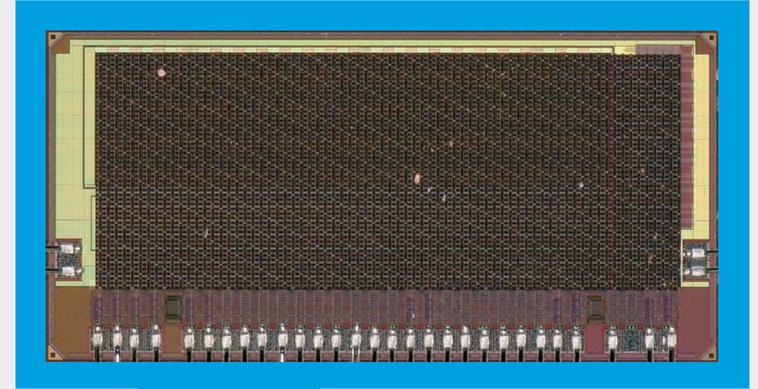
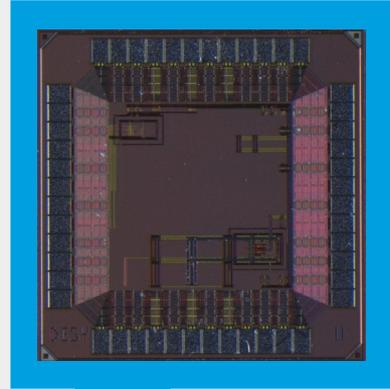
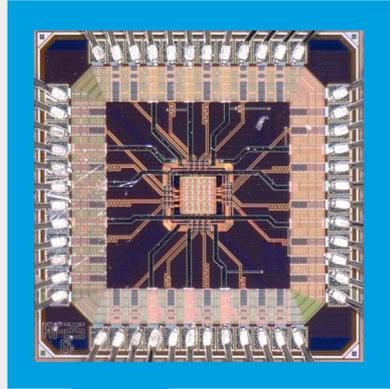
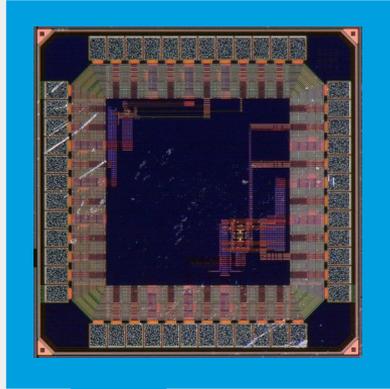
submissions supported by



- International collaboration for common submissions to foundry, organized through CERN EP R&D programme
 - Strongly driven by ALICE ITS3 collaboration
 - First application in HEP
 - Two submissions received back & tested
- Goal: explore new technology in terms of
 - Performance: efficiency, ...
 - Scalability: wafer-scale sensors, stitching
 - Timing: sensor layout optimization



Investigated Chips within Tangerine



Aglieri et al, 2024

V1 MLR1

- Test chip for fast CSA front-end
- 2 x 2 pixels + test circuits

APTS

- Analog test chip
- 4 x 4 pixels
- Different pitches, layouts & front-ends

V2 ER1

- FE test chip for H2M
- 2 x 2 pixels
- Improved CSA front-end

H2M

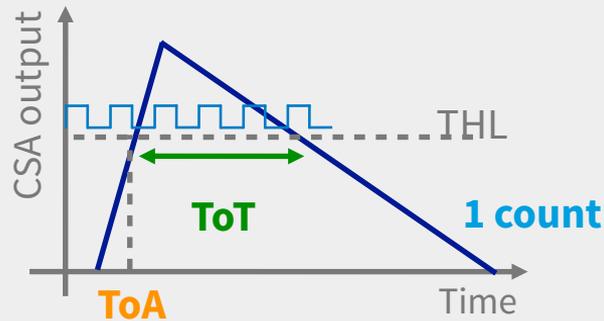
- 3 x 1.5 mm² chip area
- 64 x 16 square pixels, 35 um pitch
- Krummenacher-type CSA front-end
- Full digitization

all design supported by



Hybrid-2-Monolithic: Integrated Digital-on-Top Design

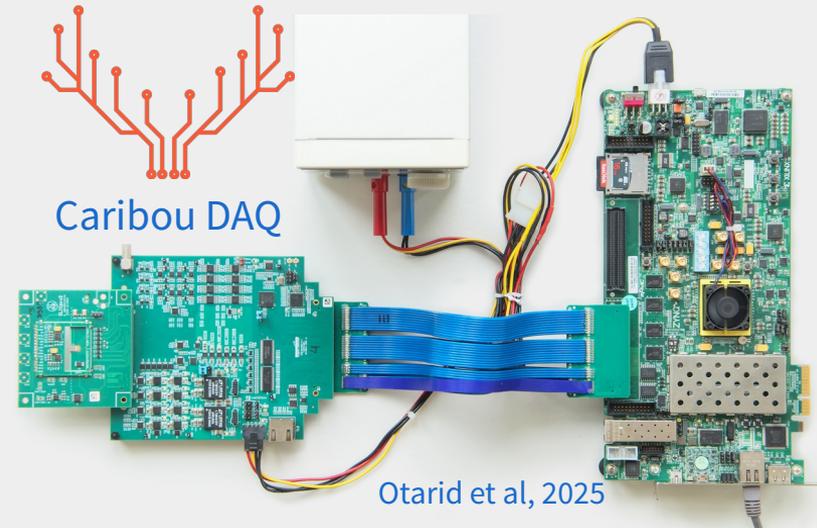
- Ports a **hybrid pixel detector architecture**
- **Digital-on-top** design workflow



- **Timepix-like 4 acquisition modes:**
 - 8 bit **ToT**,
 - 8 bit **ToA** (100 MHz clock - 10 ns binning),
 - **photon counting** (number of hits above threshold),
 - triggered (binary readout after hit validated by ext. trigger)

Integrated into the **Caribou DAQ system**

- Re-usable hardware, firmware and software
- Supports ~20 different prototypes



Constellation

Autonomous Control and Data Acquisition System

Constellation is a control and data acquisition system for small-scale experiments and experimental setup with volatile and dynamic constituents such as testbeam environments or laboratory test stands.

[Get Started](#)[Concepts](#)[See Application Developer Guide →](#)[See Framework Reference →](#)

Autonomous

Constellation operates without a central server, satellites exchange heartbeats to keep in touch.

Flexible

Automatic network discovery of satellites make it easy to add and remove satellites on the fly.

Fast Integration

The finite state machine and satellite interface are designed for fast and easy integration of devices.

Robust

Constellation is based on widely adopted networking libraries such as [ZMQ](#) and [MsgPack](#).

Some early adopters:



Swedish Radioactive Waste Handling



electronCT
DESY DGP project



ETROC



Beam Instrumentation Group
Timepix4 Beam Telescope

Website & Documentation

<https://constellation.pages.desy.de>

Testbeam Performance of H2M

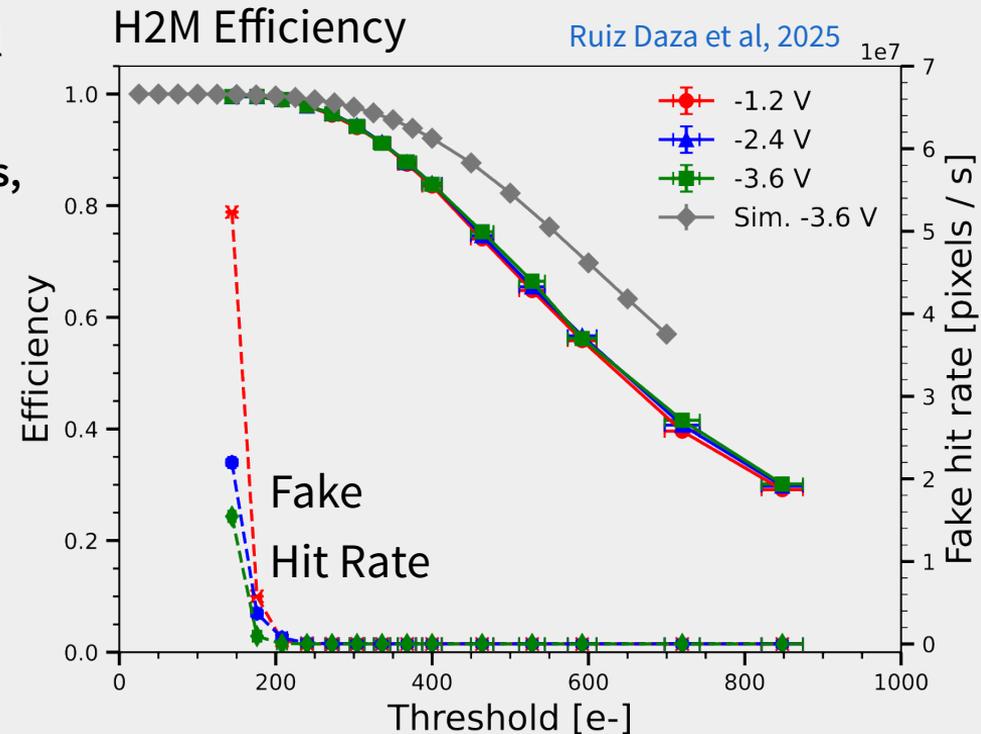


- Measurements performed at DESY II Testbeam Facility
- Crucial facility for detector R&D



- **Corryvreckan** Testbeam Data Analysis Tool
- Developed & maintained at DESY
- **Standard tool used by all LHC experiments, future collider studies & beyond**

- H2M prototype is fully efficient at threshold 144 e-, bias -3.6 V
- Higher efficiency was expected from preliminary simulations...





Allpix Squared

The Semiconductor Detector
Monte Carlo Simulation Framework

... I spare you the logos of
> 35 collaborating institutes &
> 70 contributors



Nikhef

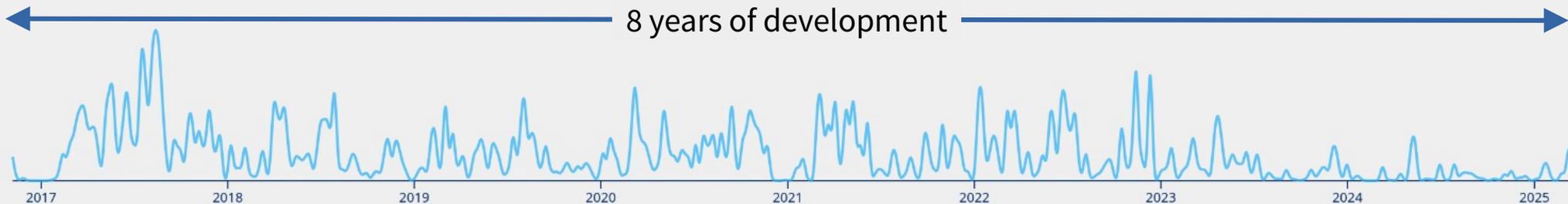
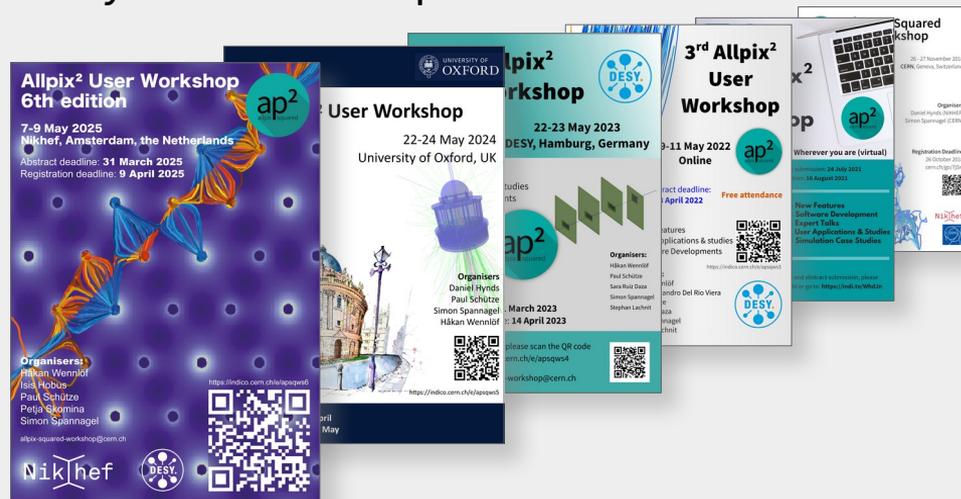


The Allpix² Framework

- **Leading Monte Carlo simulator for semiconductor detectors**
- Now > 8 years of development with
 - 54 releases, current version 3.2.0
 - More than 70 code contributors
 - More than 160 citations
- **Development & maintenance: DESY, Nikhef**



Yearly User Workshops

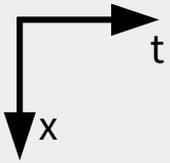


| 9079 commits | Last commit ≈ 2 weeks ago | 26 stars | 94 forks

Combining Tools for Full End-to-End Simulations



Spannagel et al, 2018
Dannheim et al, 2020
Spannagel et al, 2022
Wennl6f et al, 2025



SYNOPSYS
Sentaurus TCAD

Energy Deposition

Charge Transport

Signal Transfer

AC/DC

Digitization

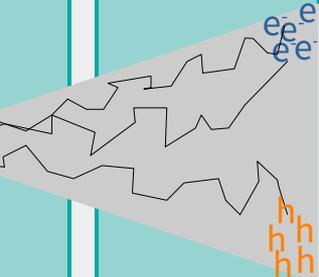


cadence
Spectre Simulation

incident radiation



e h e h e h



AC/DC

0111010010100101

detector readout

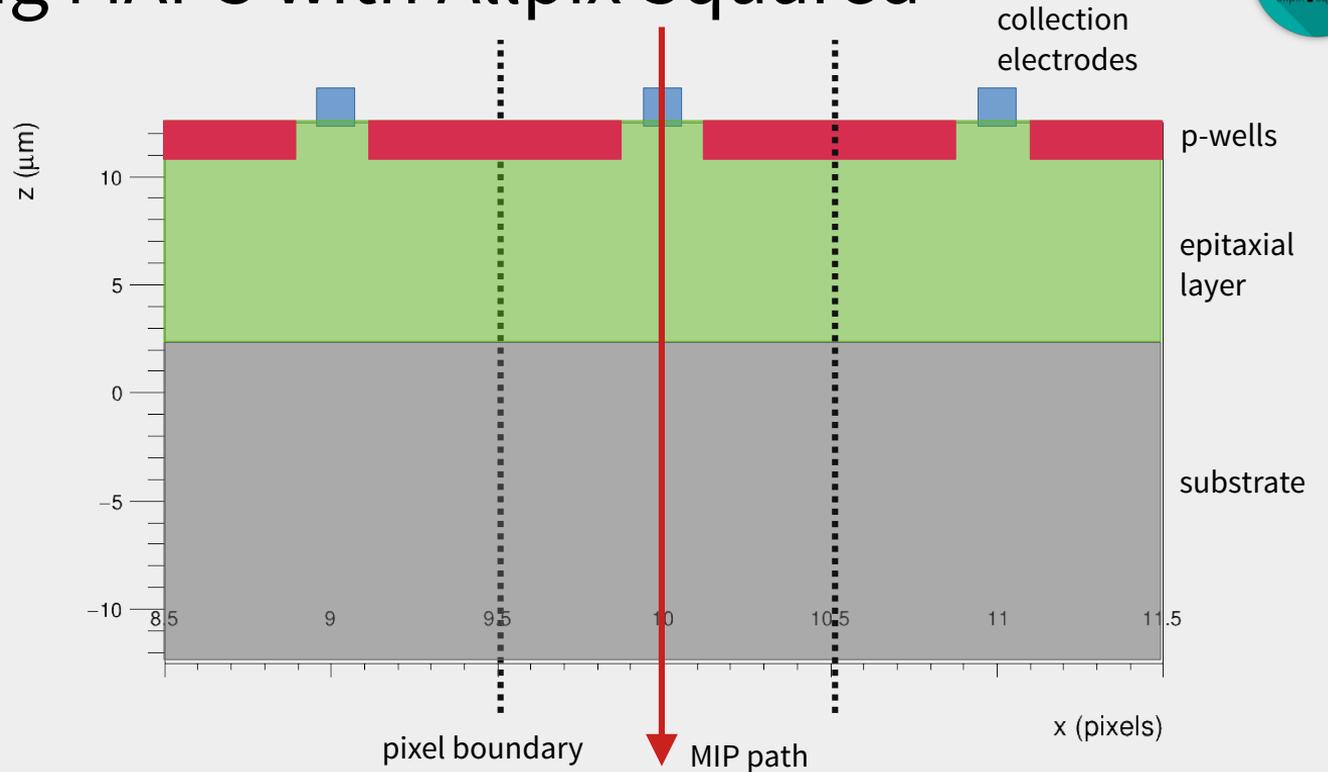


Example: Simulating MAPS with Allpix Squared



Structure of simulated sensor:

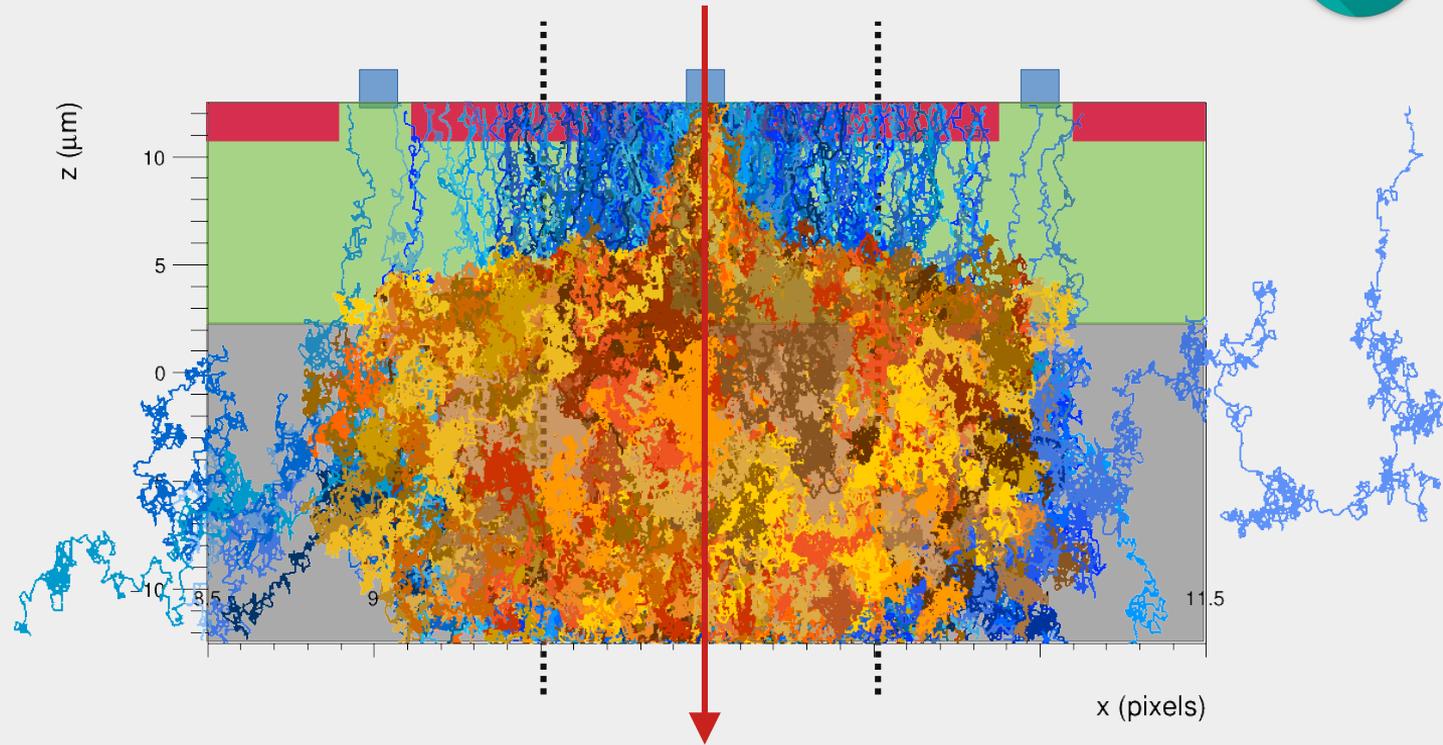
- Small-electrode sensor
- High-resistivity epi layer, electronics-grade substrate
- Deep wells protect circuit from field in sensor



Simulating response to minimum ionizing particle incident perpendicular to surface

A Simplistic Approach

- Applying linear electric field
 - Bias voltage -1.2 V
 - Depletion depth 10 μm
- Carrier mobility:
 - Standard Canali model (doping-independent)

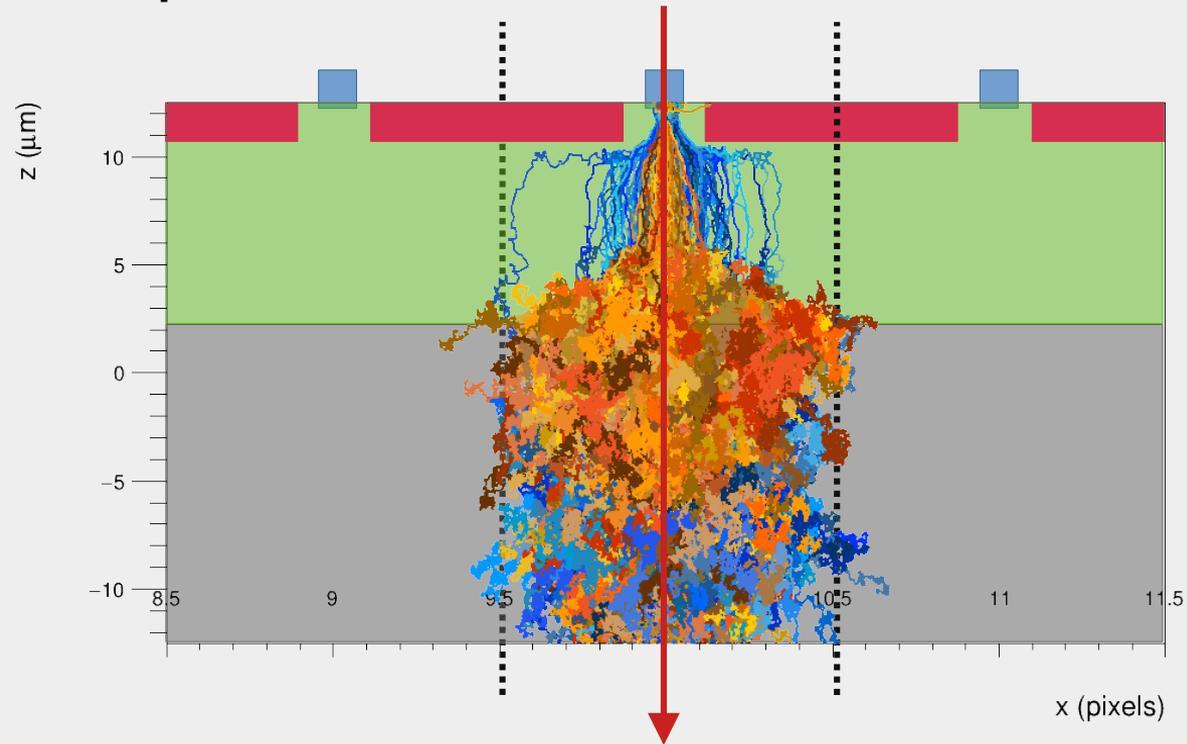


- Diffusion dominant in undepleted volume
- Linear drift of charge carriers towards sensor surface, no drift to electrodes
- Large charge cloud & cluster size, significant signal contribution from substrate

■ electrons
■ holes

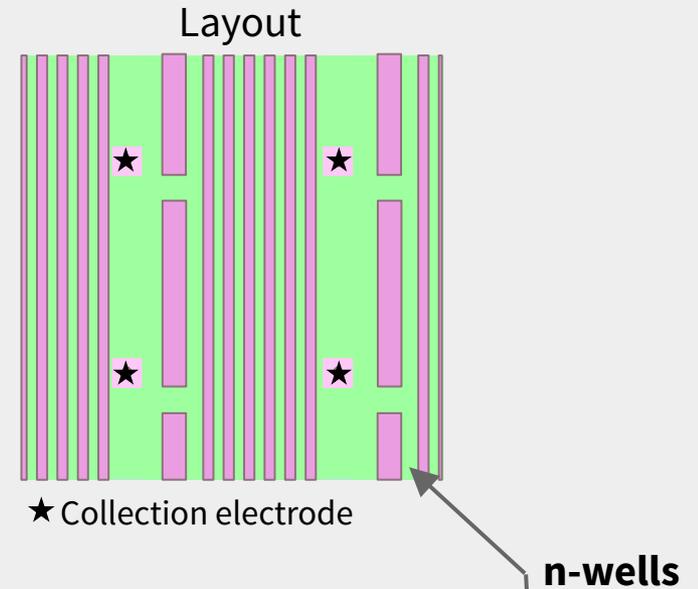
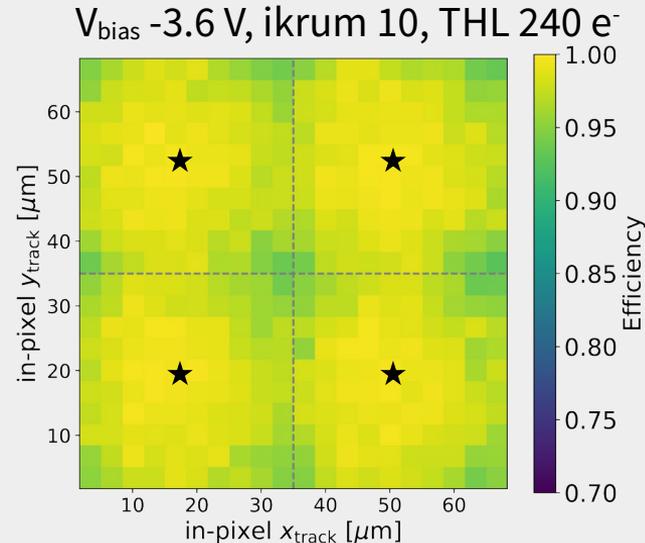
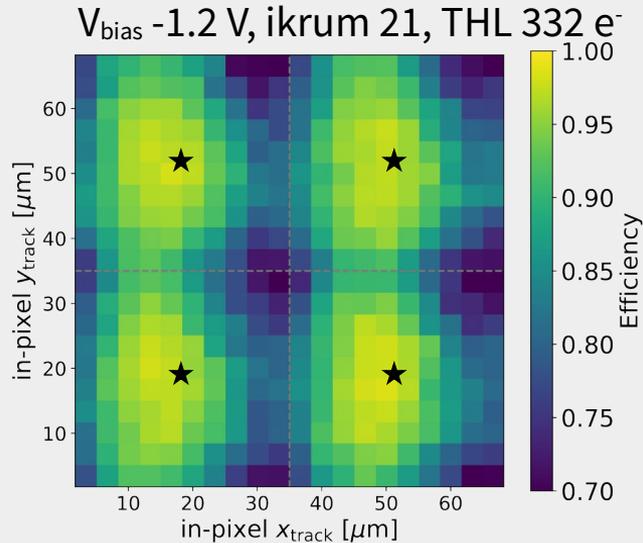
Realistic Simulation Requires More Information

- Applying **TCAD electric field**
 - Bias voltage -1.2 V
 - Depletion depth 10 μm
- Setting **doping for epi & subs.**
- Carrier mobility:
 - **Masetti-Canali** model (doping dependent)
- Recombination: **combined SRH-Auger** model



- Carrier drift obeys sensor features (p-wells), collection at electrodes
 - Significant reduction of diffusion in highly-doped substrate, less charge sharing from substrate contributions
 - Significant reduction of substrate contributions due to short lifetime in high-doping volume
- electrons
■ holes

Back to H2M: Non-Uniformity of In-Pixel Response

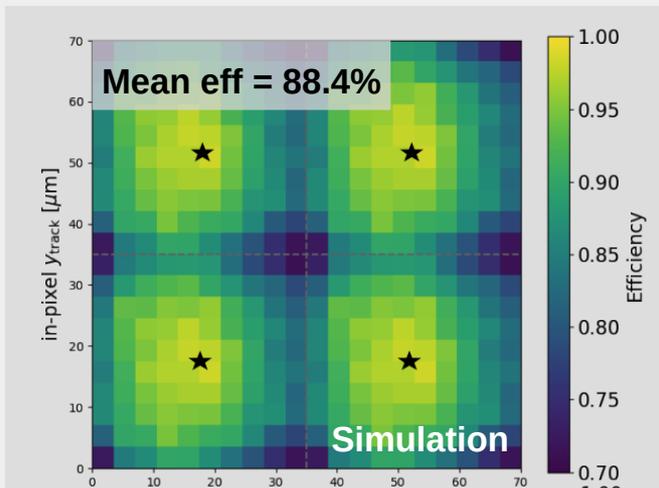
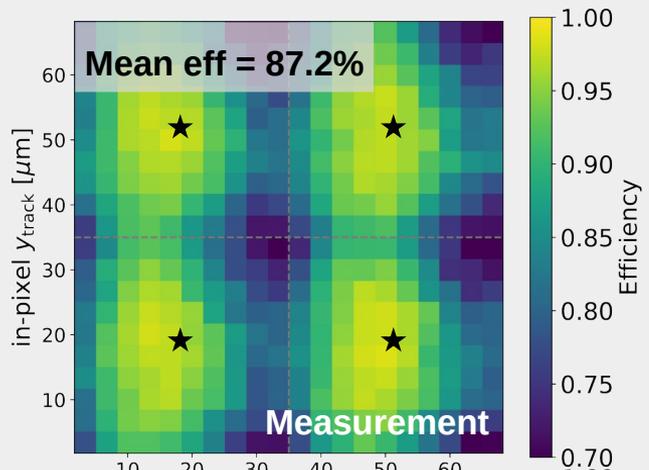


- Related to the **size and location of the n-wells** of the analog circuitry
 - Large n-well to house feedback capacitance for amplifier
 - N-wells of digital circuitry small & regular
- For future designs: investigating effects of relocating n-wells **with simulations**

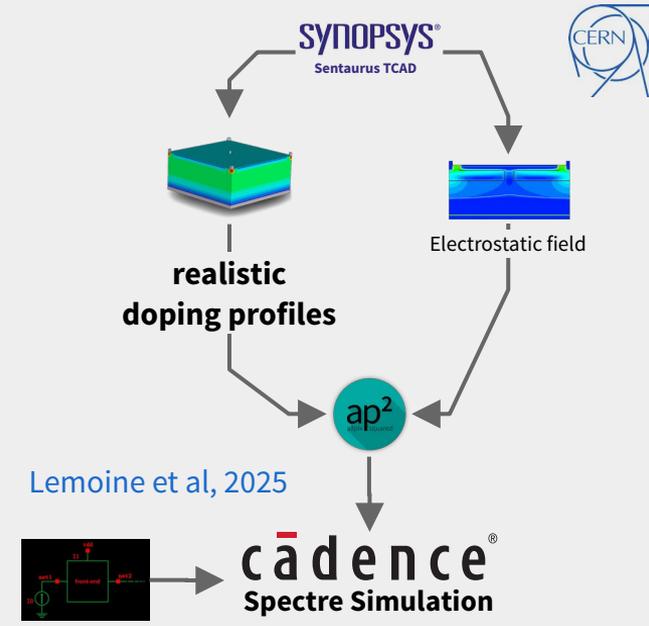
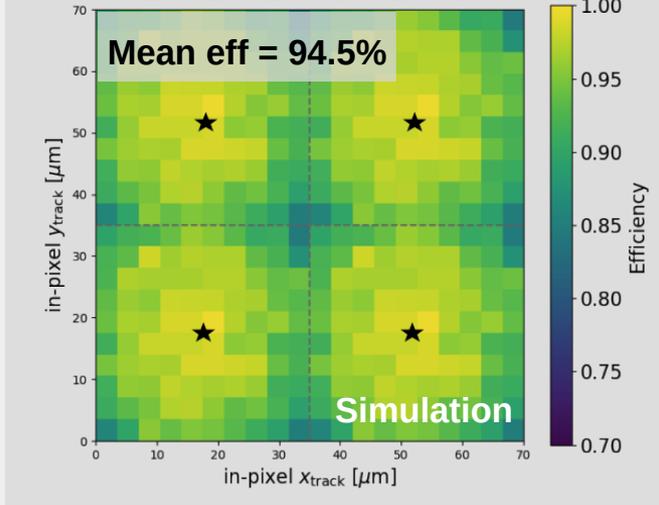
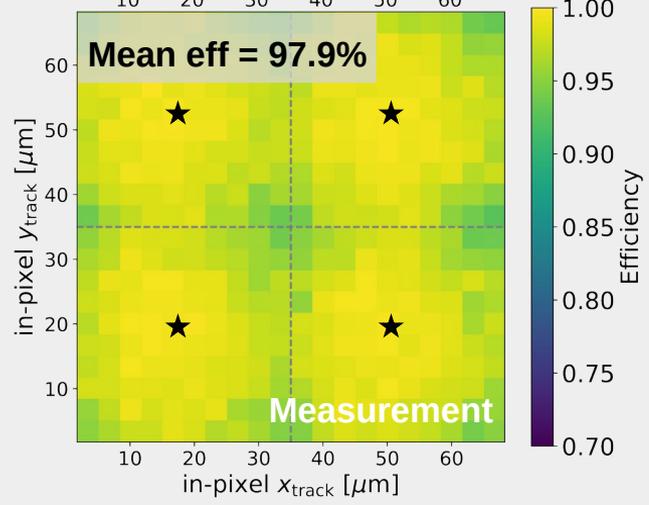


Confirmation by Simulation with N- Wells

$V_{bias} -1.2 V, THL 332 e^-$



$V_{bias} -3.6 V, THL 240 e^-$



- Simulation with **realistic doping** profiles
- Includes n-well structure within p-well
- Simulation can qualitatively reproduce effect in **efficiency as well as ToA**
- **Slowing-down of charge carriers** traveling below large n-wells



SOPHIE

Silicon Photonic Integrated Electronics
A Helmholtz Innovation Pool Project



Monolithic Silicon Photonics

Bandwidth & power consumption of data transmission **critical for future experiments:**

$$\frac{1 \text{ cm}^2 \text{ chip area}}{(15 \mu\text{m})^2 \text{ pixel pitch}} \geq 450 \text{ kPix} \rightarrow 450 \text{ kPix} \cdot 20 \text{ bit} \cdot 10^{-5} \text{ occupancy} \simeq 90 \text{ b} \rightarrow \frac{90 \text{ bit}}{20 \text{ ns}} \geq 4.5 \text{ Gb s}^{-1} \text{ cm}^{-2}$$

Particle physics	Photon science	Laser-based approaches in the community		State-of-the-art silicon photonics	
<p>CMS</p>	<p>DSSC</p>	<p>CERN's VTRx+</p>	<p>SAMTEC's FireFly</p>	<p>MACOM's 400G</p>	<p>Teramount's Phot Plug</p>
<ul style="list-style-type: none"> Millions of channels μm, ps & mV resolution 		<ul style="list-style-type: none"> Throughput: terabits/second Compactness: tens of Gigabits/s/cm² 		<ul style="list-style-type: none"> EMI & H-field immunity radiation tolerance low material budget power-over-fiber 	

Electronic-Photonic Integrated Circuit

GF's 45-nm SOI CMOS industry-grade process

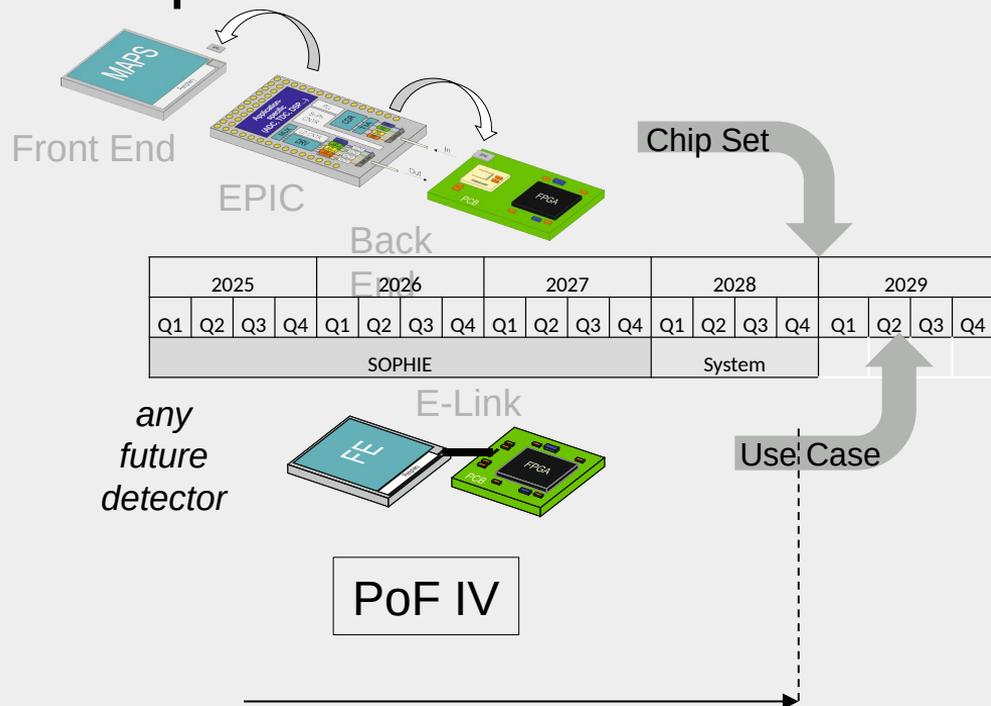
Monolithic - photonics & electronics on a chip

Advanced Packaging

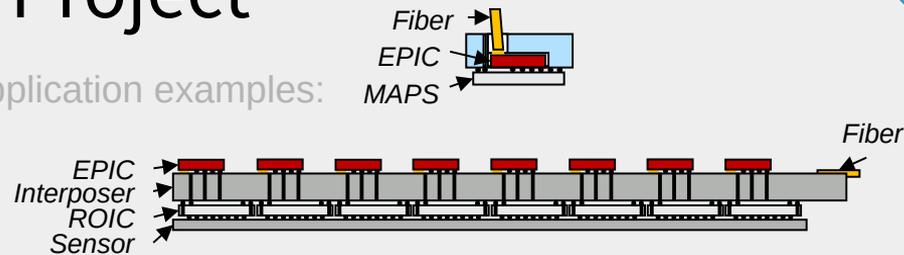
Scalable to exploit full potential of CMOS process

Fiber-chip coupling & electrical/optical interposer

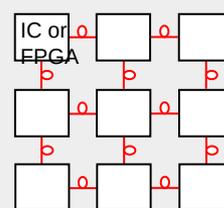
Perspectives From The SOPHIE Project



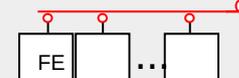
Application examples:



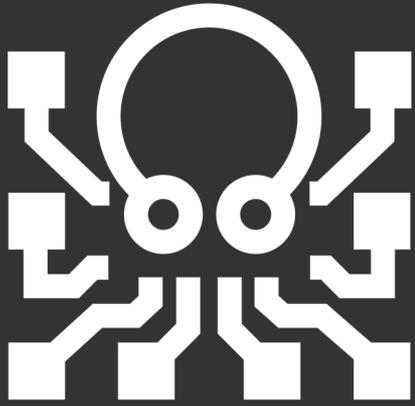
Distributed Processing



Pixel Column



- Realize system EPIC
- Investigate & select packaging technologies
- Apply to 1st single-chip detector
- Investigate & select photonic interposer technologies
- Elaborate detector concepts
- Build a demonstrator



OCTOPUS

Optimized CMOS Technology for Precision in Ultra-thin Silicon
The 1st Project in the Framework fo the ECFA DRD3 Collaboration



DRD3 Project OCTOPUS

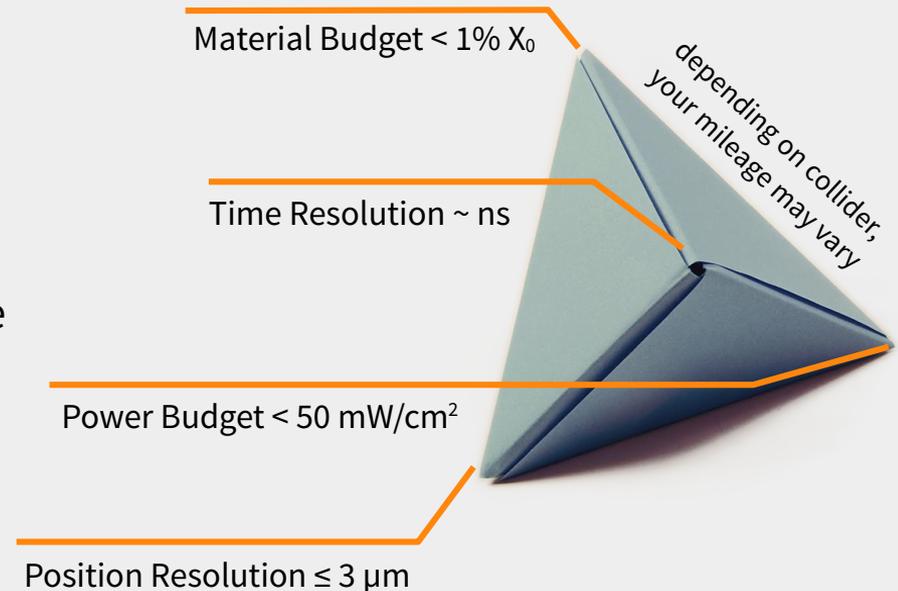


The ECFA Detector R&D Collaborations

- Addressing challenges of future particle physics experiments
- DRD3 focusing on Solid State Detectors & Technologies

OCTOPUS – A Project for a Future Vertex Detector

- DRD goal: *”Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors”*
- Development of a **monolithic sensor prototype**
- **Staged approach:** further refinement of performance targets after conclusion of strategy update
- Intermediate target: Development of **high-resolution sensors for beam telescopes**



Summary

- Strong Semiconductor Detector R&D at DESY-FH
- Strategic goal: develop technology for next generation of particle physics experiments
 - Challenging specs, require novel approaches
 - Key technology: Monolithic detectors, highly integrated systems
 - Many applications possible on the way
- DESY-FH develops several tools crucial to detector R&D
 - Many have become standard in HEP
 - Some well beyond particle physics
 - DESY has a lot of visibility in community through development & maintenance

DESY-FH is applying its expertise to future projects
OCTOPUS, SOPHIE, tools for Detector R&D...

