uTCA mother board for FMC ADC daughter cards

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Agenda

Introduction

Project Goals:

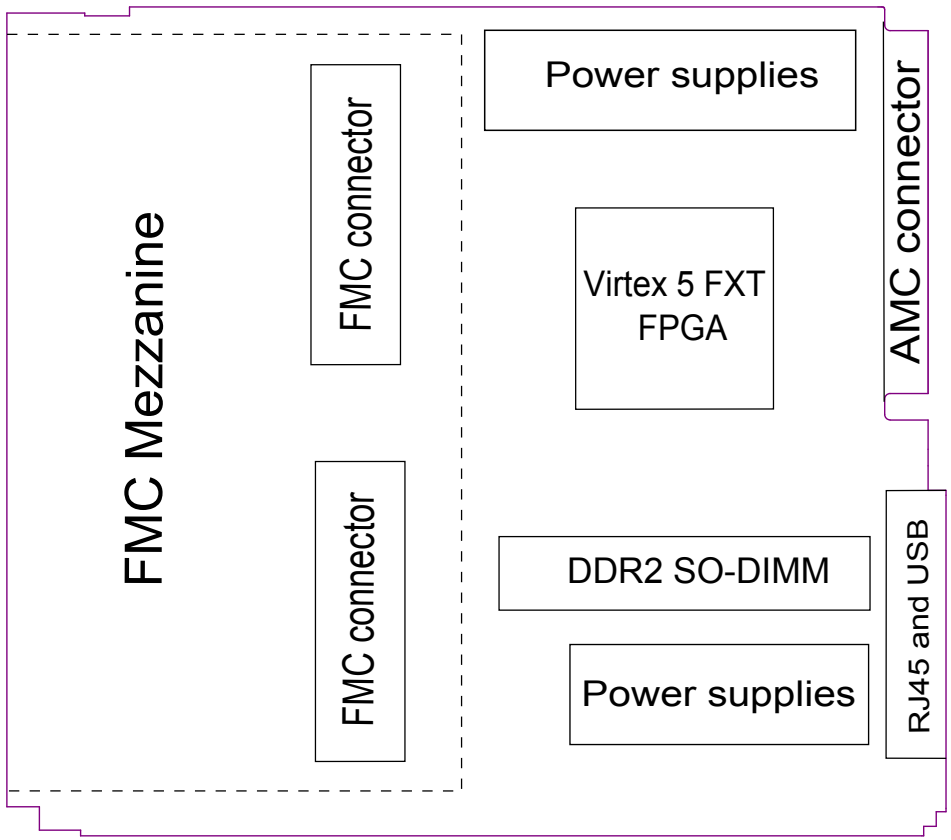
- Primary - upgrade of Bunch Arrival Time Monitor electronics (ACB2.1 board)
- uTCA platform for direct sampling board (Samer Bou Habib)

Basic Features:

- Support for high accuracy (up to 16 bits) and high speed (up 1GSPS) ADCs
- uTCA format - officially chosen for X-FEL and FLASH electronics,
- Application specific (analog) part on FMC mezzanines
  - Common components (FPGA, power supplies, etc.) are placed on base board
  - Commercial FMC modules can be used
  - Dedicated FMC modules (for BAM) can be designed and reused in future in other projects
- High performance Virtex-5 FPGA used

Carrier Board

- Support for double width or two single width FMC
- AMC.4 compatibility with IPMI support
- High performance FPGA on board

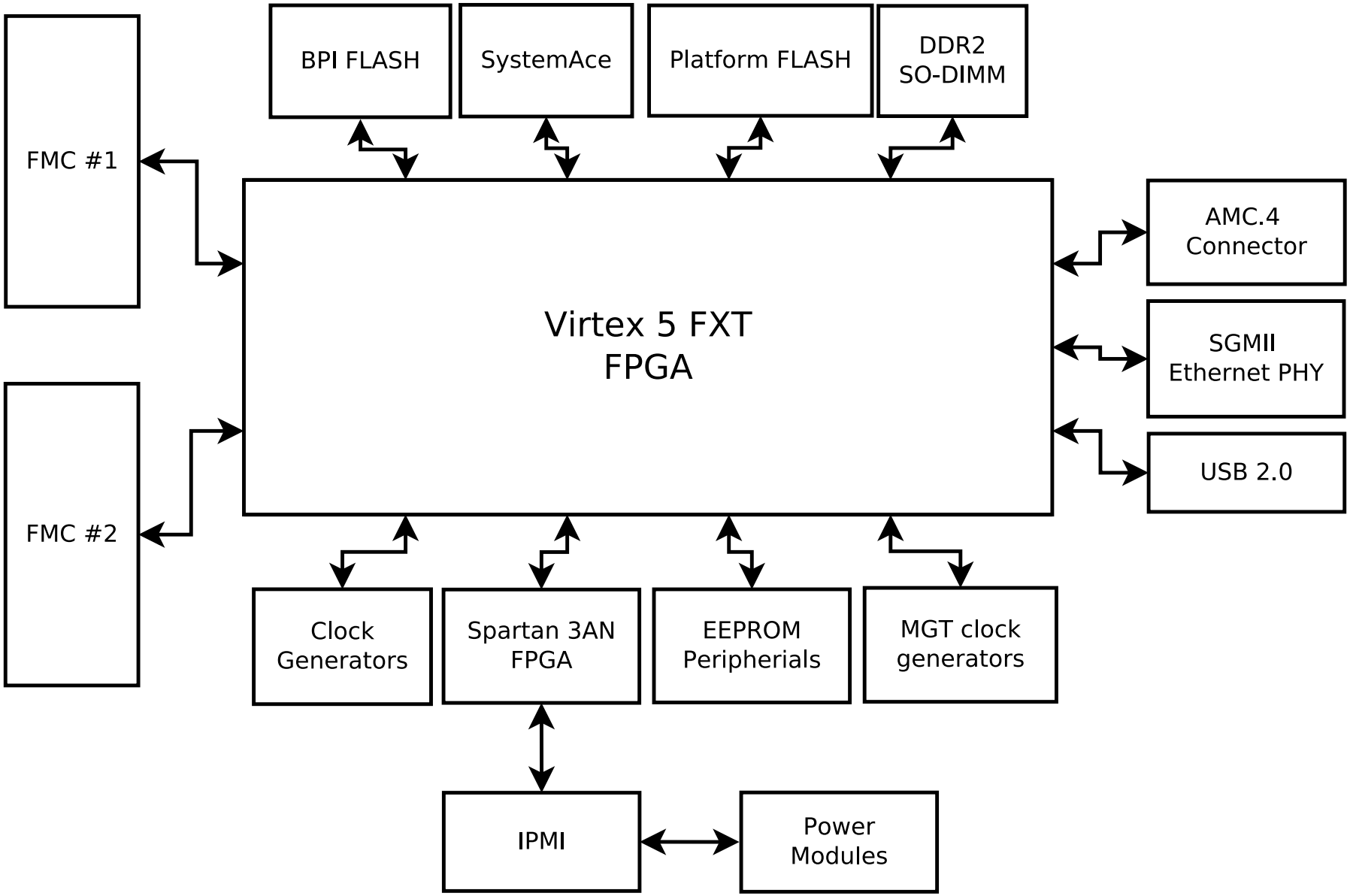


Analog mezzanines - FMC

FMC - FPGA Mezzanine Card Standard (ANSI/VITA 57.1)

- Commercial standard (Xilinx involved in standard definition)
- I/O mezzanine module,
- works intimately with an FPGA
- minimize signal latency
- maximize data throughput.

Block Diagram



Board Features

- Two single or one double size FMC mezzanine support
- Over 70 differential pairs or 140 single ended signals available for each FMC slot
- Four Gigabit serial channels per FMC slot
- Virtex5 FXT70 FPGA with embedded PowerPC440 processor
- DDR2 SO-DIMM connector
- IPMI unit
- Advanced configuration modes with fail-safe configuration memory
- CF card as a configuration memory, and non-volatile storage for embedded systems
- Serial port and JTAG over USB
- Gigabit Ethernet PHY and RJ45 socket for stand-alone operation
- Watchdog and configuration supervisor implemented in separate small FPGA
- AMC.4 communication lanes:
  - Gigabit Ethernet
  - PCI Express
  - Two point-2-point links
  - Two M-LVDS links
  - CLKA and CLKB routed to FPGA
  - JTAG

Difficulties - Schematics

- Understanding standards and products (a lot of reading...):
  - AMC4
  - FMC
  - DDR2
  - Xilinx products
- Clock generation and distribution circuits
- FMC and FPGA clock domains
- FPGA programming

Difficulties - PCB

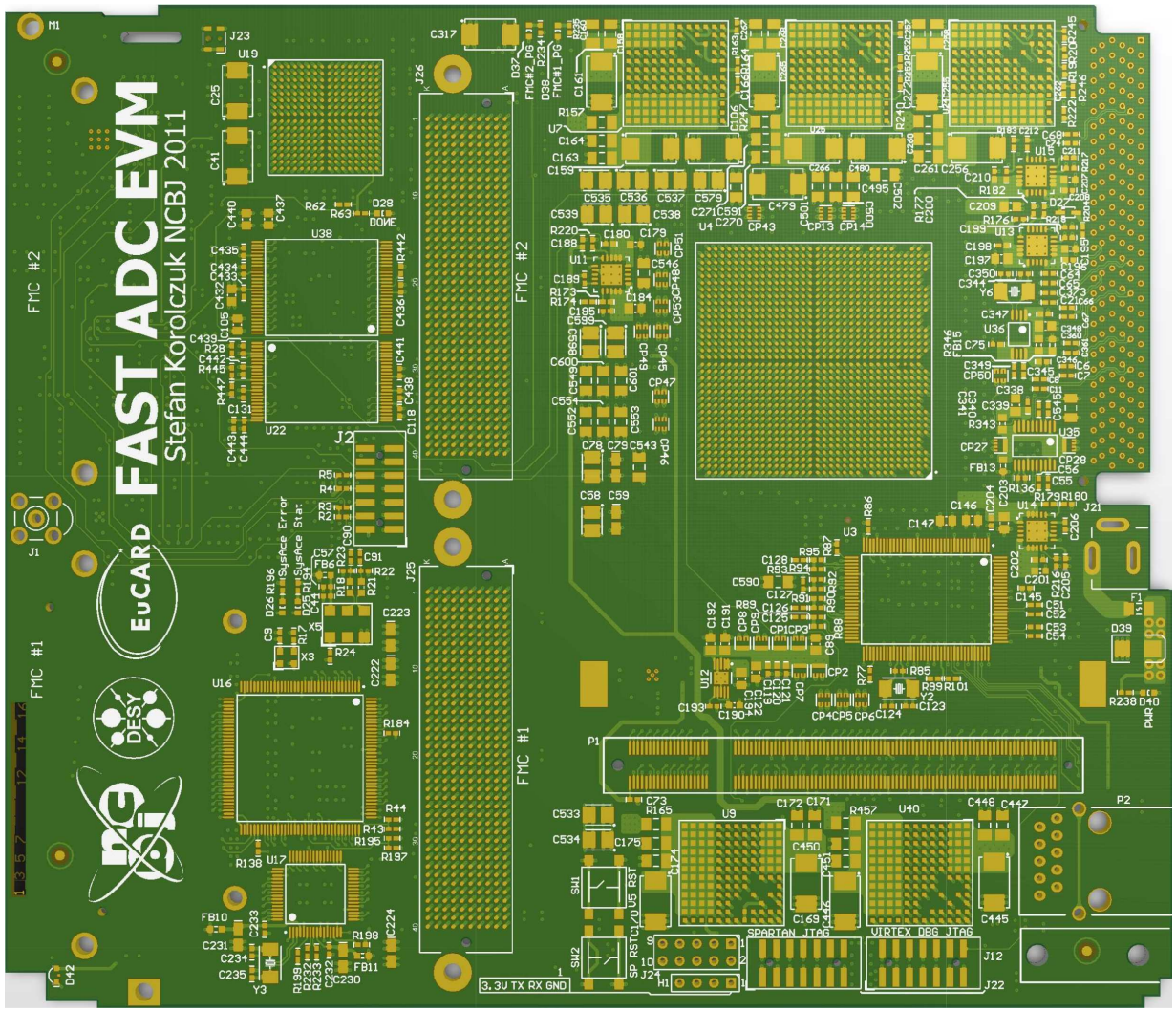
- High speed signal integrity
- FPGA fanout signals (more than 90% of 1136 FPGA pins usage)
- DDR2 layout
- Power Distribution Network
- Gigabit transceivers
- Clock distribution network
- FMC differential lines matched length:
  - two HPC FMC slots - 160 differential data lines + clock + Gb lanes
  - 8 clock domains with matched signal lengths (more than 16 diff pairs in one domain)
  - Signals matching is better than 10ps

Project Status

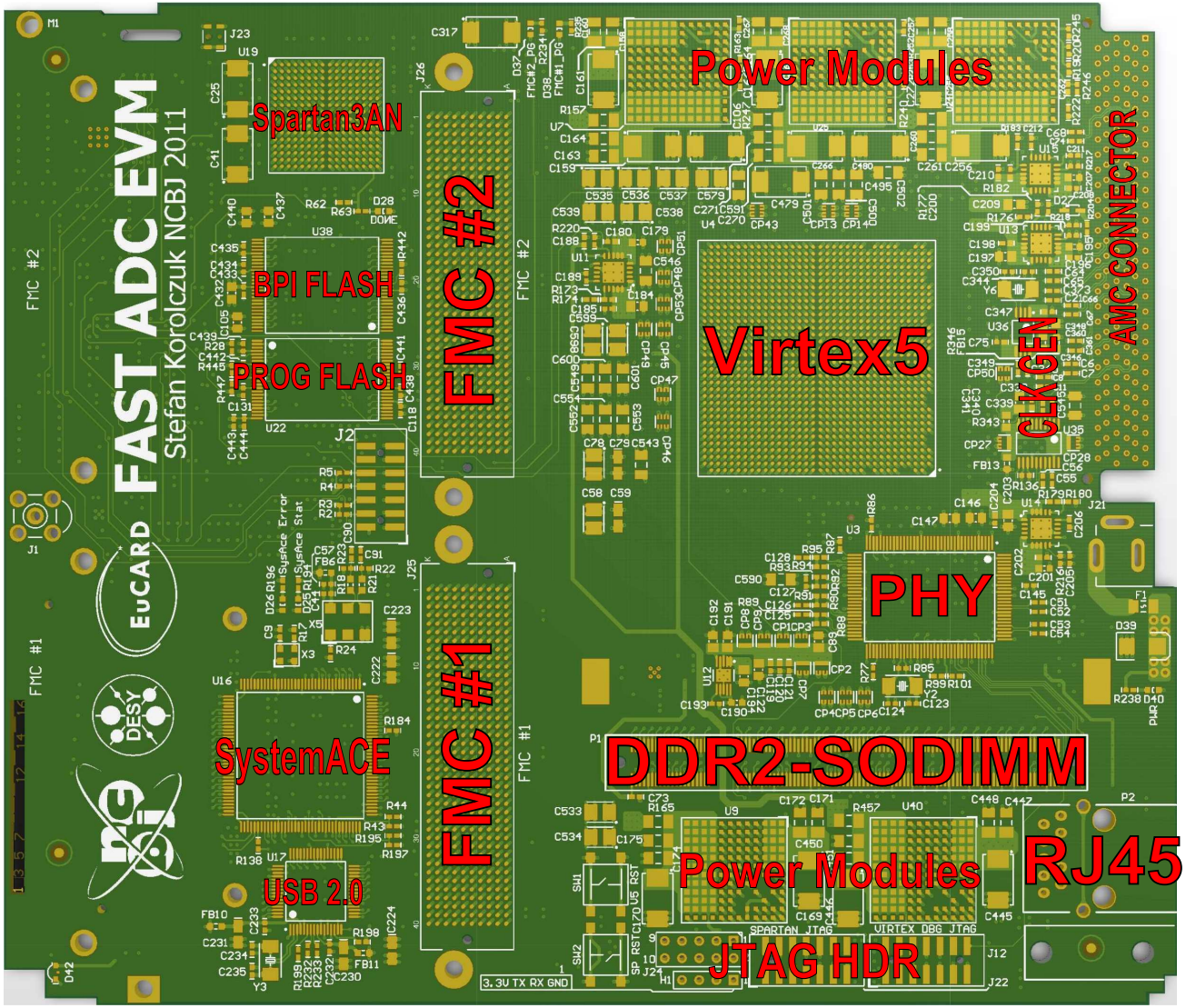
- Board has been send to production - expected on 1.01.2012
- VHDL projects for testing following peripherals has been developed:
  - DDR2 memory
  - Gigabit Ethernet
  - FMC connectors (path from connector to first flip-flop)

Board Layout - Top

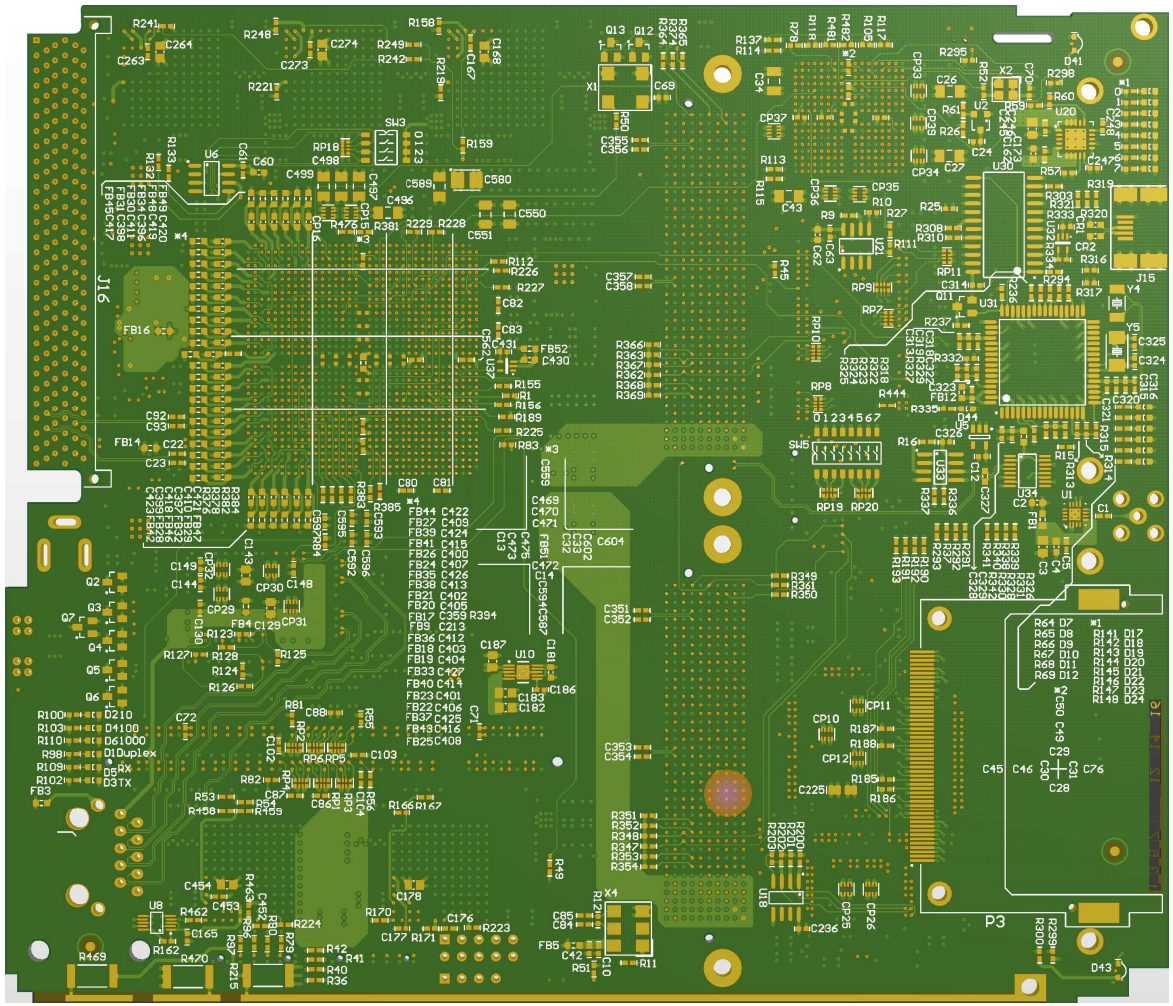
16-layers board, FR408 epoxy laminate and pre-preg.



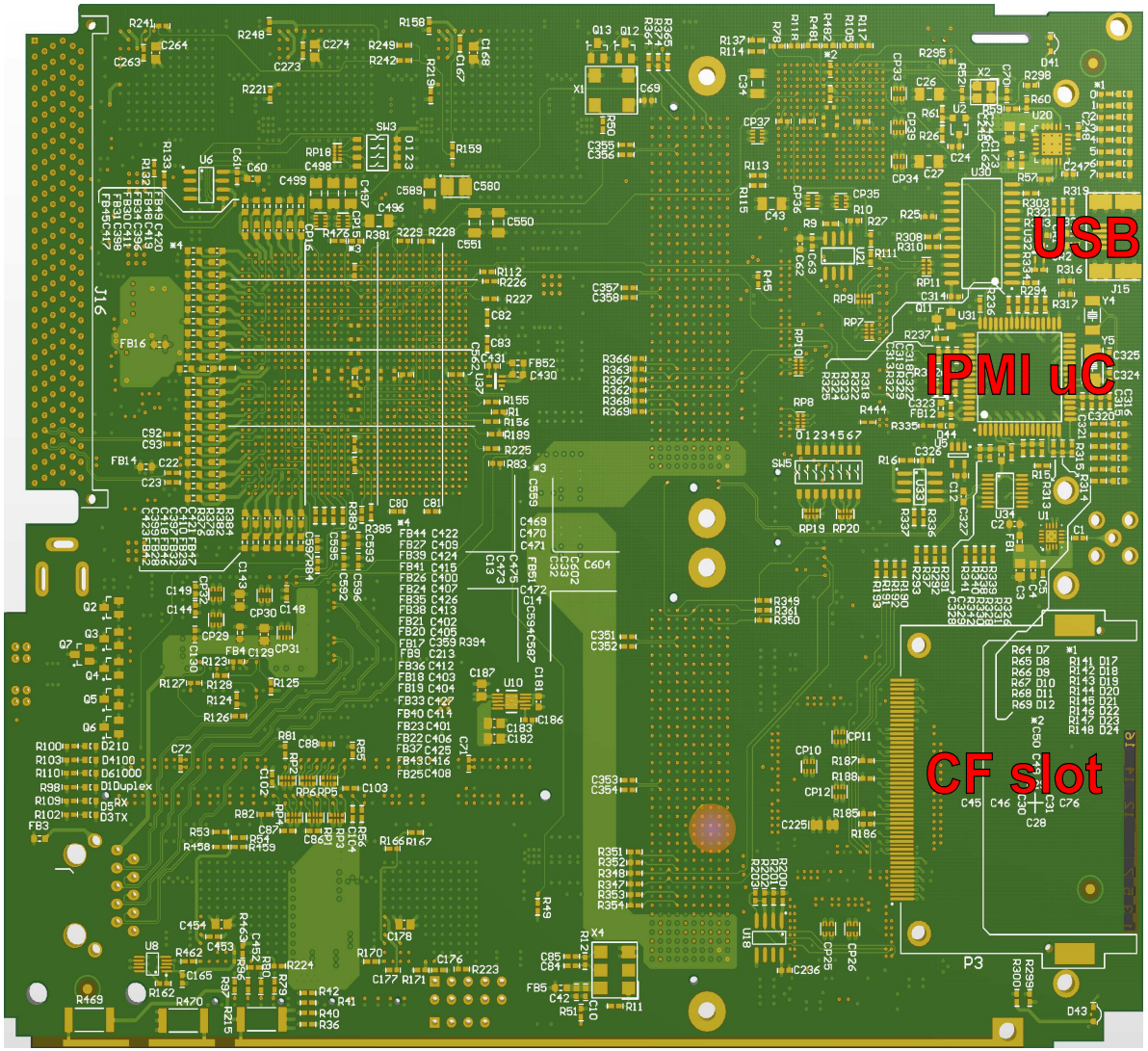
Component Placement - Top



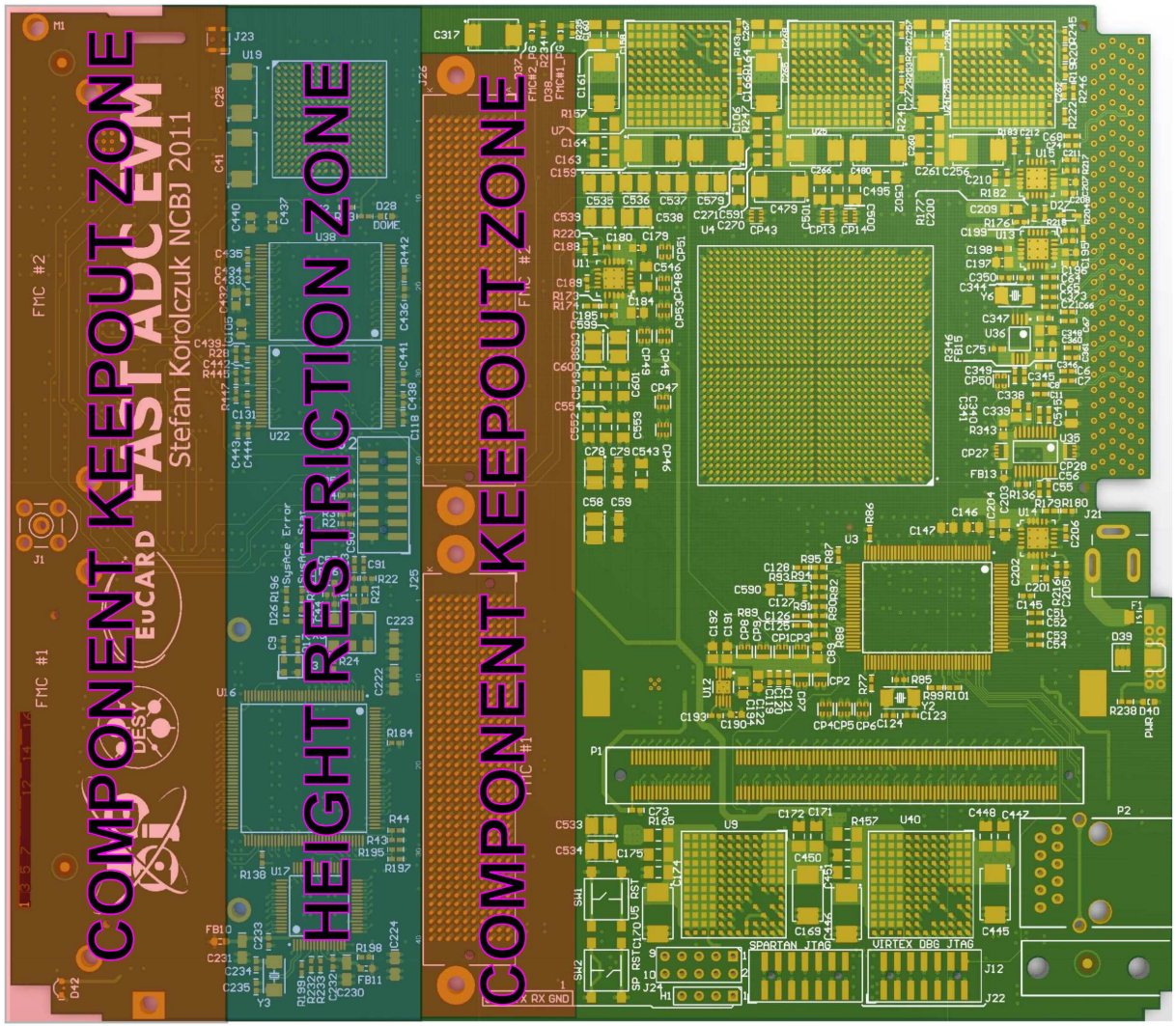
Board Layout - Bottom



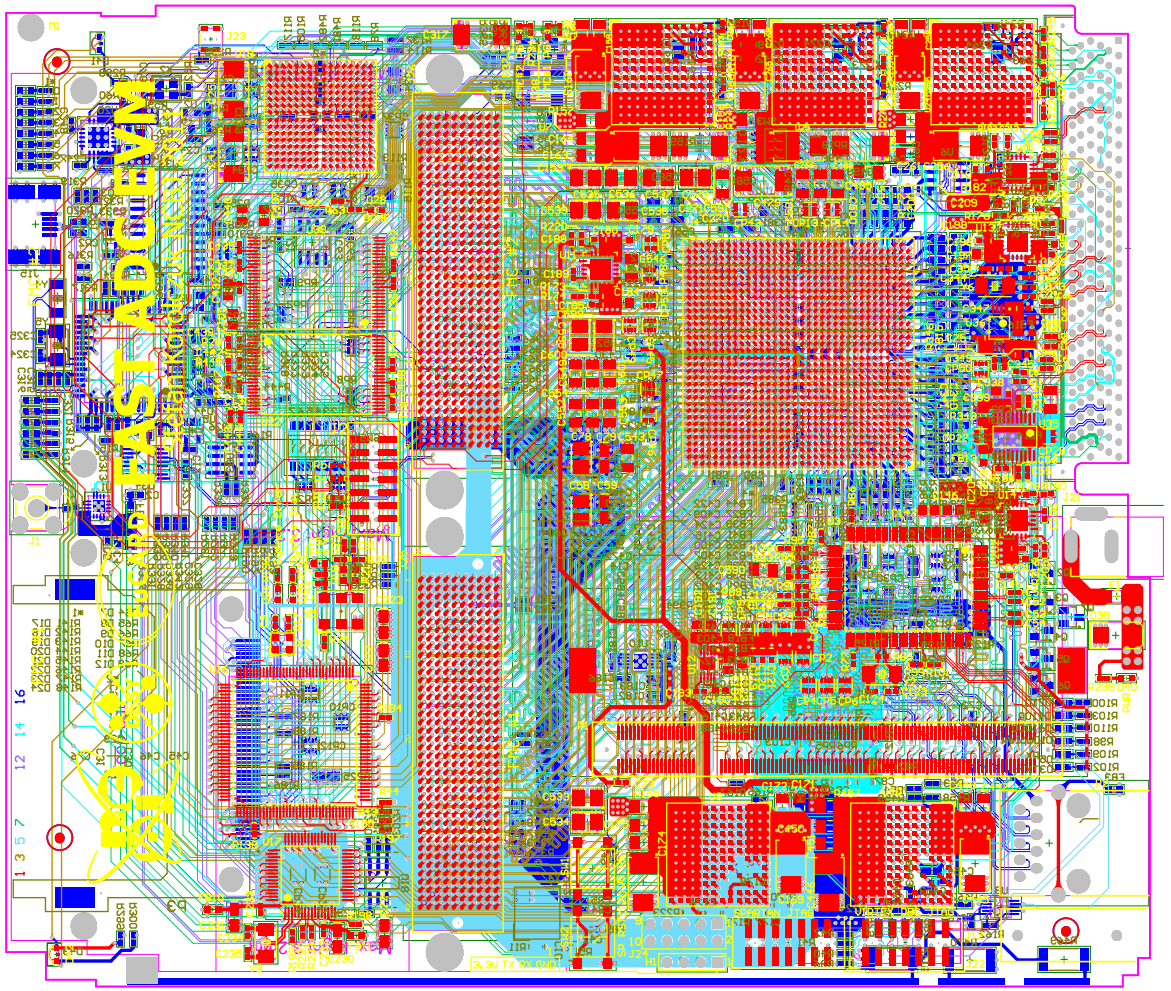
Component Placement - Bottom



Component Height Restriction



Signal Layers



The End

Thank you for your attention