TMCB Firmware

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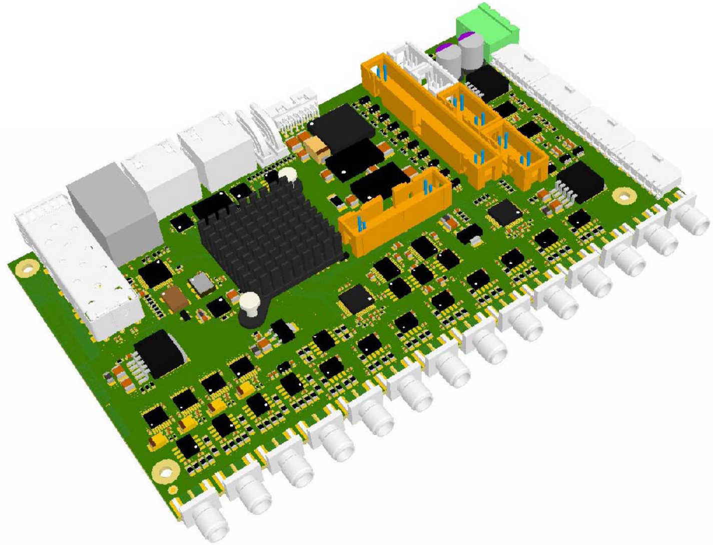
Agenda

1. TMCB status
2. Ethernet
3. Applications
4. Summary

The Board



Board features

- 1x Spartan-6 FPGA (XC6SLX45T-2FGG484C)
- 8x Analog input, 1 MSPS, 16 bit (2x AD7655 ADC)
- 4x Analog input, 128 kSPS, 24 bit (4x AD7767 ADC)
- 2x Analog output, 1 MSPS, 18 bit, (2x AD5781 DAC)
- 4x Temp sensor (2x ADS1248)
- 2x Peltier (1x DAC8552 DAC, 2x LTC2365 ADC)
- GPIO (20x IO)
- Ethernet (1x DP83848C, RMII mode)
- RocketIO fiber interface (1x SFP)
- 13x LVDS pairs
- 2x I2C channels
- 8x LED

Implementation status

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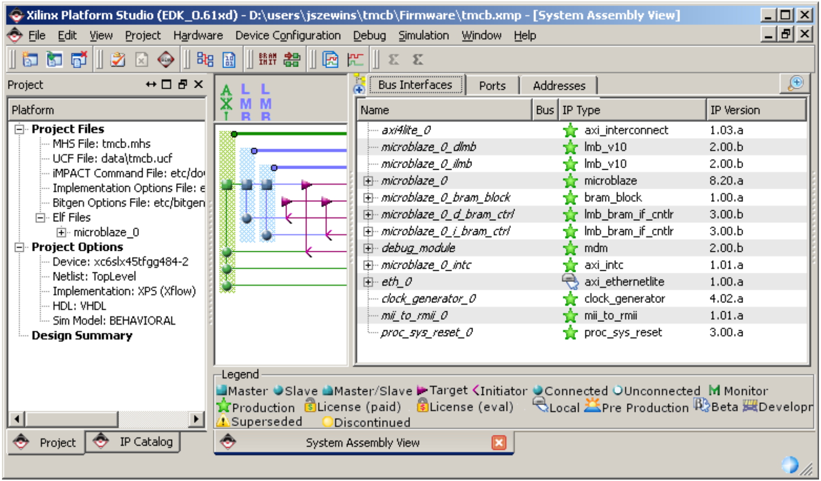
MicroBlaze based embedded system for the Ethernet



Xilinx Platform Studio (EDK_0.61xd) - D:\users\jszewins\tmcb\Firmware\tmcb.xmp - [System Assembly View]

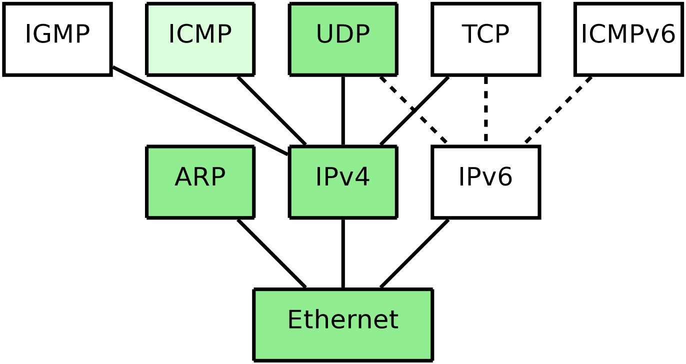
- Project Files
  - MHS File: tmcb.mhs
  - UCF File: data\tmcb.ucf
  - iMPACT Command File: etc/do
  - Implementation Options File: e
  - Bitgen Options File: etc/bitgen
  - Elf Files
    - microblaze_0
- Project Options
  - Device: xc6slx45tfgg484-2
  - Netlist: TopLevel
  - Implementation: XPS (Xflow)
  - HDL: VHDL
  - Sim Model: BEHAVIORAL
- Design Summary

Name	Bus	IP Type	IP Version
axi4lite_0		axi_interconnect	1.03.a
microblaze_0_dlmb		lmb_v10	2.00.b
microblaze_0_ilmb		lmb_v10	2.00.b
microblaze_0		microblaze	8.20.a
microblaze_0_bram_block		bram_block	1.00.a
microblaze_0_d_bram_ctrl		lmb_bram_if_cntlr	3.00.b
microblaze_0_i_bram_ctrl		lmb_bram_if_cntlr	3.00.b
debug_module		mdm	2.00.b
microblaze_0_intc		axi_intc	1.01.a
eth_0		axi_ethernetlite	1.00.a
clock_generator_0		clock_generator	4.02.a
mii_to_rmii_0		mii_to_rmii	1.01.a
proc_sys_reset_0		proc_sys_reset	3.00.a

TCP/IP Stack

- Standard LwIP stack could not be used because it needs at least 1MB of RAM - so new one has been created
- New stack supports minimal set of features needed to handle UDP protocol
- Memory is needed for TCP, to reconstruct big data blocks from fragmented packets (long buffer is needed)
- UDP transfers single packets, without taking care of data loss and packet order

Implemented parts of TCP/IP protocol family



Implementation

Protocol Stack:

- Support for Ethernet frames
- Support for the ARP protocol
- Support for the IPv4 protocol - without fragmentation and extended options (frame up to 1500 bytes)
- Support for the ICMP protocol - only response to echo request (ping)
- Support for the UDP protocol
- All code runs in 64kB of ram (probably less would be also fine)
- About 500 lines of C code

Software:

- MEX files for communication from Matlab are ready
- Dedicated DOOCS servers will be made for particular applications

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Firmware for Drift Calibration Module

- RF switches (GPIO) - ready
- Digital Controlled Attenuators (GPIO) - ready
- Temperature controller - under development
  - PID controller will be ported from ACB2.1
- Peltier (TEC) - to be done
- Amplitude RF detector, readout from 24-bit ADC - ready
- Operation modes (continues, switching) - under development
- Ethernet communication has used to set parameters - ready

Firmware for Fiber Link Optical Synchronization

- Analog monitoring (slow and fast ADCs) - ready
- Controller (*ADC* → *IIR* → *PID* → *DAC* feedback) - under development
  - Fast ADC readout - ready
  - DAC support - ready
  - PID controller will be ported from ACB2.1
  - Low-pass filter (2^{nd} order IIR) will be ported from ACB2.1
- Temperature monitoring - under development
- Temperature control with Peltier element - to be done
- Microwire protocol, for attenuators and phase shifters - to be done
- SFP fiber link interface - under development
- DOOCS server - to be done
  - C code for Ethernet communication with TMCB ready

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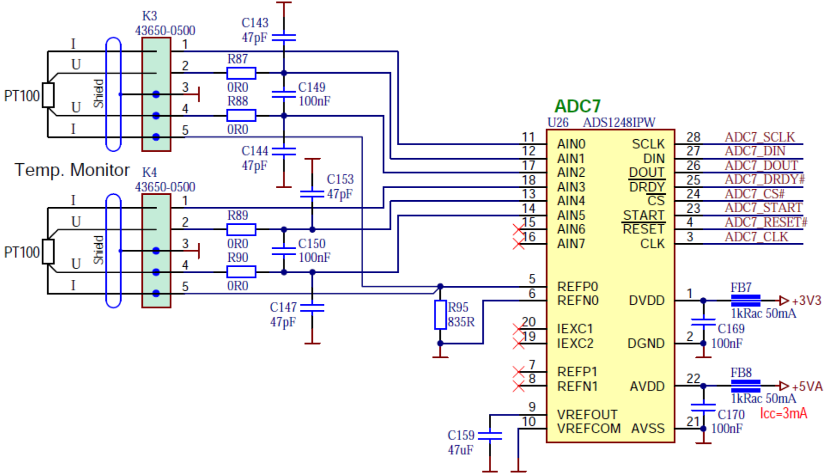
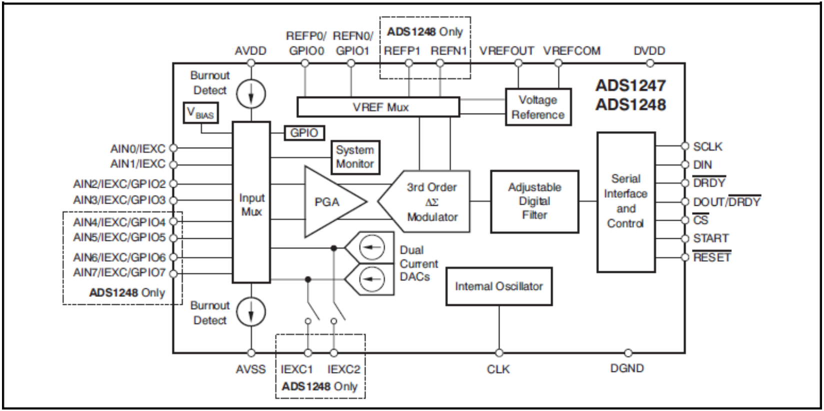
- **Temperature sensors**
  - The sensor is self (PT100) had to be obtained first (took some time)
  - The ADC for temperature monitoring is complex, and has to correctly configured to work properly

ADS1248 (1)

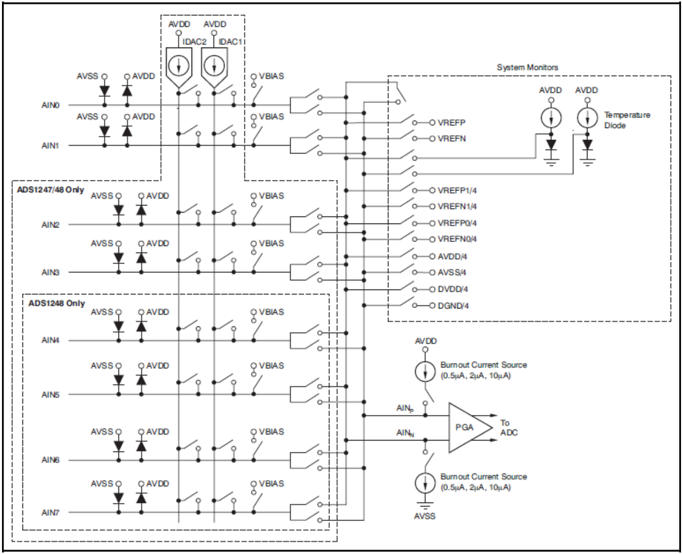

K3
43650-0500
C143
47pF
R87
0R0
R88
0R0
C149
100nF
C144
47pF
PT100
Shield
I
U
U
I
1
2
3
4
5
Temp. Monitor
K4
43650-0500
C153
47pF
R89
0R0
R90
0R0
C150
100nF
C147
47pF
R95
835R
ADC7
U26
ADS1248IPW
11 AIN0
12 AIN1
17 AIN2
18 AIN3
13 AIN4
14 AIN5
15 AIN6
16 AIN7
5 REFP0
6 REFN0
20 IEXC1
19 IEXC2
7 REFP1
8 REFN1
9 VREFOUT
10 VREFCOM
SCLK 28 ADC7_SCLK
DIN 27 ADC7_DIN
DOUT 26 ADC7_DOUT
DRDY 25 ADC7_DRDY#
CS 24 ADC7_CS#
START 23 ADC7_START
RESET 4 ADC7_RESET#
CLK 3 ADC7_CLK
DVDD 1
DGND 2
AVDD 22
AVSS 21
FB7
1kRac 50mA
+3V3
C169
100nF
FB8
1kRac 50mA
+5VA
C170
100nF
Icc=3mA
C159
47uF

ADS1248 (2)



ADS1248 Only
REFP0/ GPIO0
REFN0/ GPIO1
REFP1
REFN1
AVDD
VREFOUT
VREFCOM
DVDD
ADS1247
ADS1248
Burnout Detect
V_BIAS
VREF Mux
Voltage Reference
GPIO
System Monitor
AIN0/IEXC
AIN1/IEXC
AIN2/IEXC/GPIO2
AIN3/IEXC/GPIO3
AIN4/IEXC/GPIO4
AIN5/IEXC/GPIO5
AIN6/IEXC/GPIO6
AIN7/IEXC/GPIO7
ADS1248 Only
Input Mux
PGA
3rd Order ΔΣ Modulator
Adjustable Digital Filter
Serial Interface and Control
SCLK
DIN
DRDY
DOUT/DRDY
CS
START
RESET
Dual Current DACs
Internal Oscillator
Burnout Detect
AVSS
IEXC1
IEXC2
ADS1248 Only
CLK
DGND

ADS1248 (3)


AVDD
AVDD
IDAC2
IDAC1
System Monitors
AVSS
AVDD
VBIAS
AIN0
AVSS
AVDD
VBIAS
AIN1
ADS1247/48 Only
AVSS
AVDD
VBIAS
AIN2
AVSS
AVDD
VBIAS
AIN3
ADS1248 Only
AVSS
AVDD
VBIAS
AIN4
AVSS
AVDD
VBIAS
AIN5
AVSS
AVDD
VBIAS
AIN6
AVSS
AVDD
VBIAS
AIN7
AVDD
AVDD
Temperature
Diode
VREFP
VREFN
VREFP1/4
VREFN1/4
VREFP0/4
VREFN0/4
AVDD/4
AVSS/4
DVDD/4
DGND/4
AVDD
Burnout Current Source
(0.5μA, 2μA, 10μA)
AIN_P
AIN_N
PGA
To
ADC
Burnout Current Source
(0.5μA, 2μA, 10μA)
AVSS

Issues, plans

Issues:

- External RAM (SRAM, SDRAM) memory would make writing the embedded code easy.
- External EEPROM would be nice (for storing MAC address).
- Serial (USB-Serial) interface would be also nice (not critical).

Plans:

- DCM firmware is already being developed by B.Yang
- RF Optical fiberlink application will be developed by J.Szewinski

The end

Thank You