uTCA software structure -overview and vision-

"based on group discussions "

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DESY

Outline

- A brief timeline
- Software structuring
  - General comments
  - Block by block
  - Tasks to be done
- Discussion points

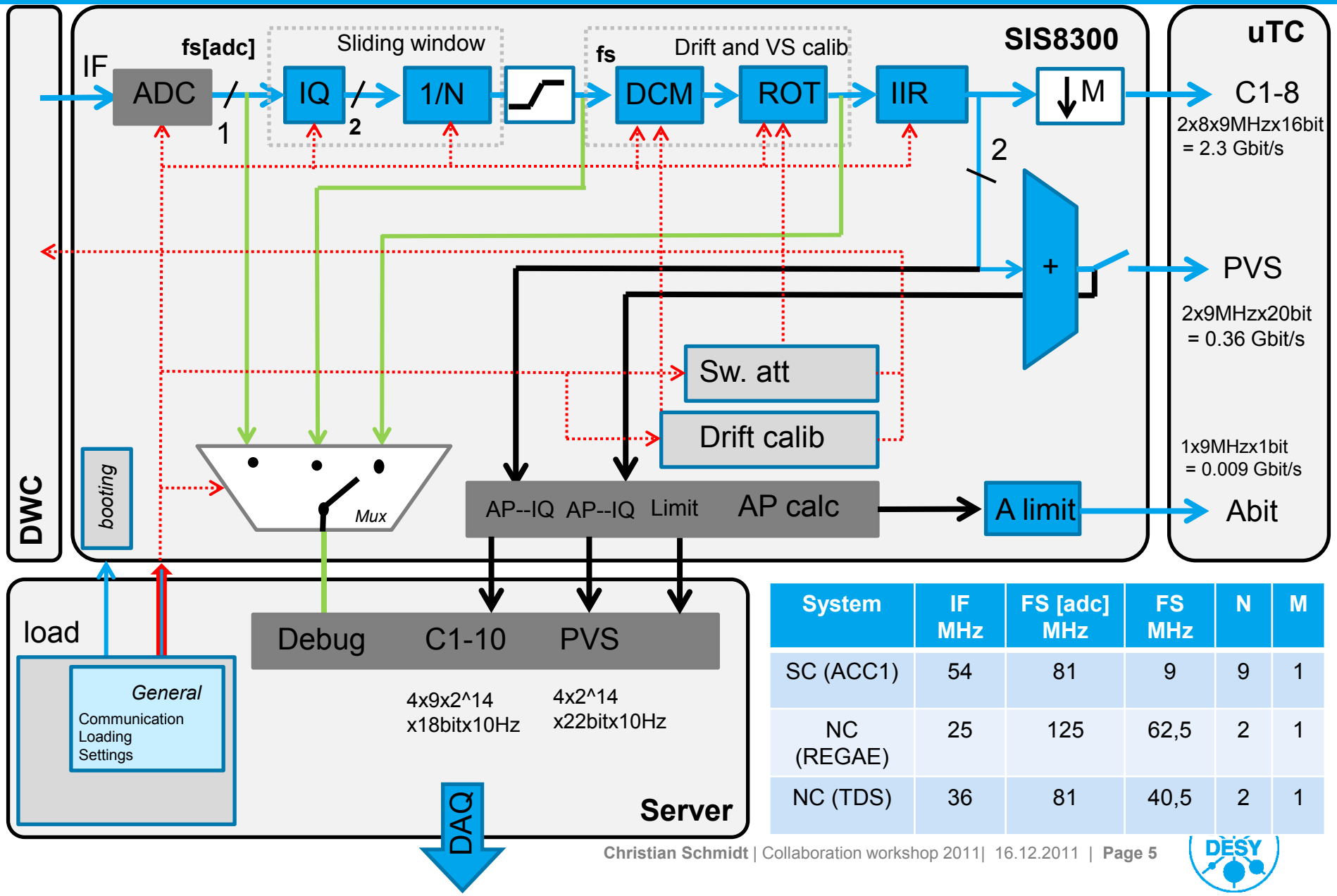
A brief (incomplete) timeline

- Started with DSP based digital controller
  - Machine size and control system distribution changed during time
- FPGA based SIMCON boards
  - Mixture of different systems along the machine
- Unification in 2010
  - All RF stations equipped with Simcon DSP
  - Same server, firmware structure, couple of important upgrades
- 2011 first uTCA test at ACC1
  - Conversion from vme based software to uTCA and linux compatible version
  - Goal keeping both Versions compatible for parallel development
- And now ?
  - Compatibility not given anymore, structural design is optimized for SIMCON
  - What will be the strategy for next development steps?

General comments to software design

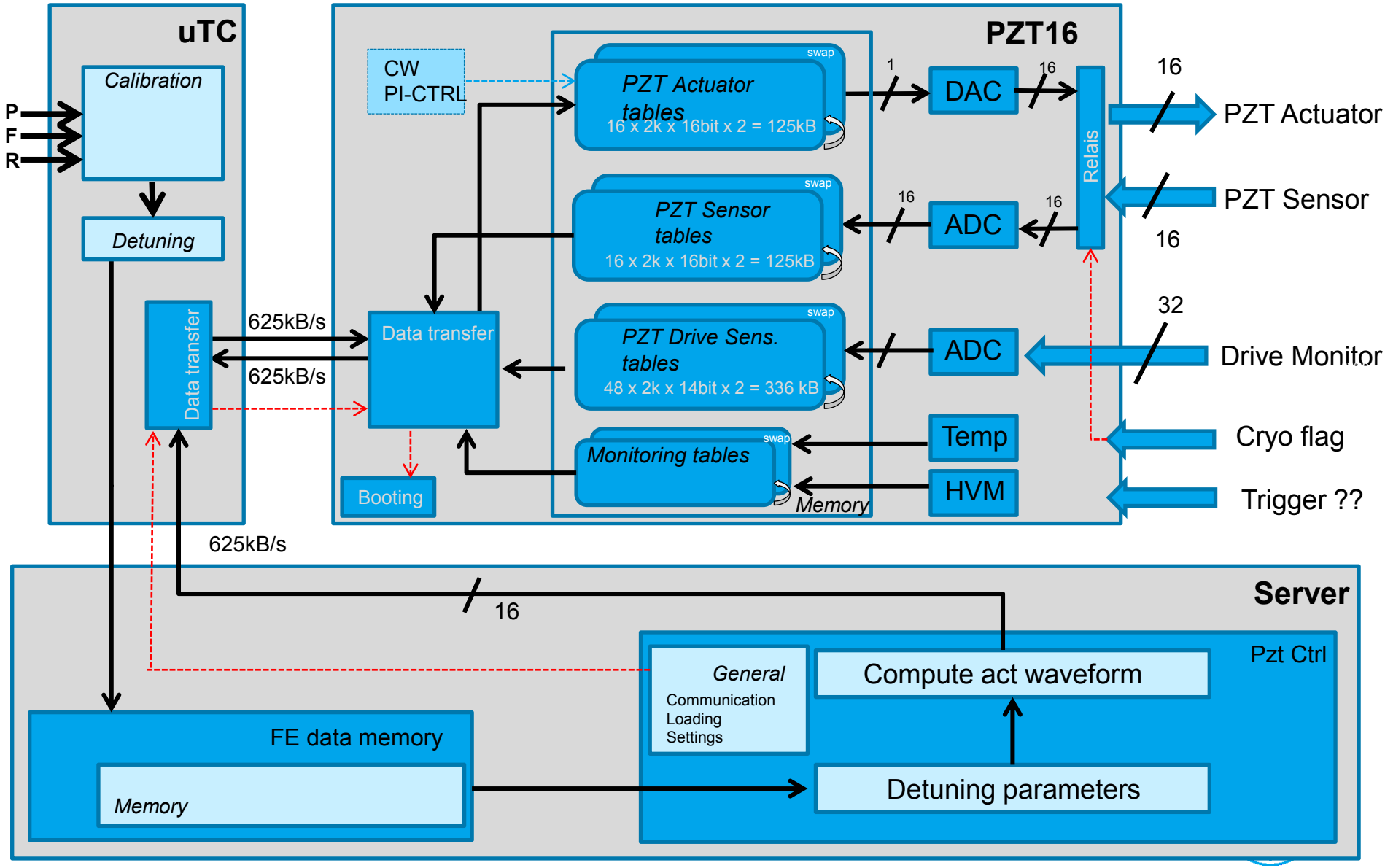
- Well documented inside the code as well as offline description
- Reliable and easy maintainable, performance should be reached
- Generic to use at different systems with different properties
  - Blocks are individual and can be modular plugged together depending on application needs
  - If possible use switches or dividers to adjust eg. for different frequencies
  - Must be extendable to XFEL main linac requirements (32 cavities, master/slave crate)
- Structuring must be extendable in future without major upgrade
  - Having margin in FPGA space, server CPU usage, communication bandwidth
  - Possible table doubling for FLASH2 and XFEL
- Not clear if all proposals can be implemented as thought
  - There will be still iteration steps to be made
- Functionality tests, benchmarks, setup procedures
- Design concept essential
  - Interface definition and communication bandwidth estimation
  - Estimation of FPGA requirements and server layout and resource needs

ADC board functional block diagram (proposal)

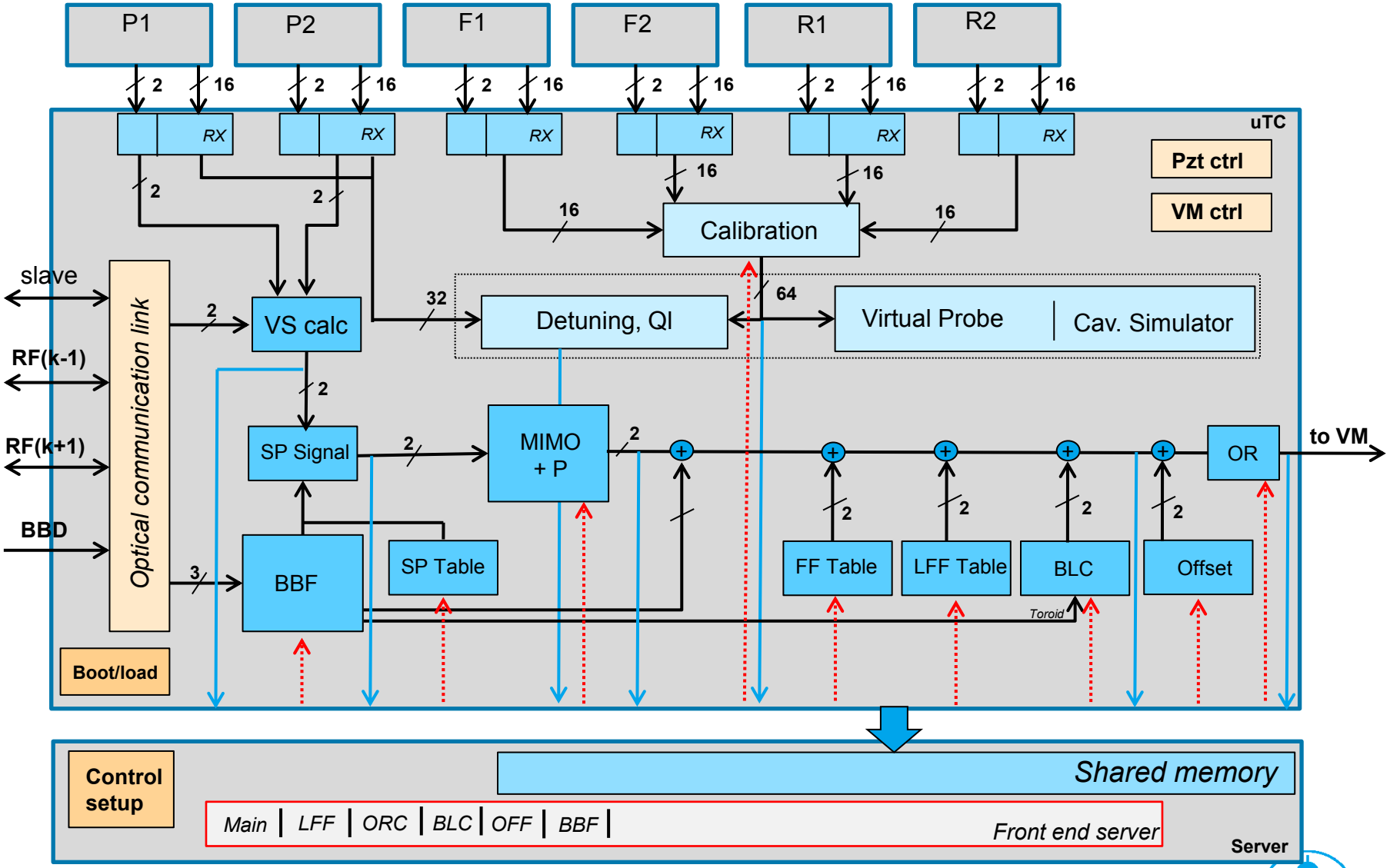


System	IF MHz	FS [adc] MHz	FS MHz	N	M
SC (ACC1)	54	81	9	9	1
NC (REGAE)	25	125	62,5	2	1
NC (TDS)	36	81	40,5	2	1

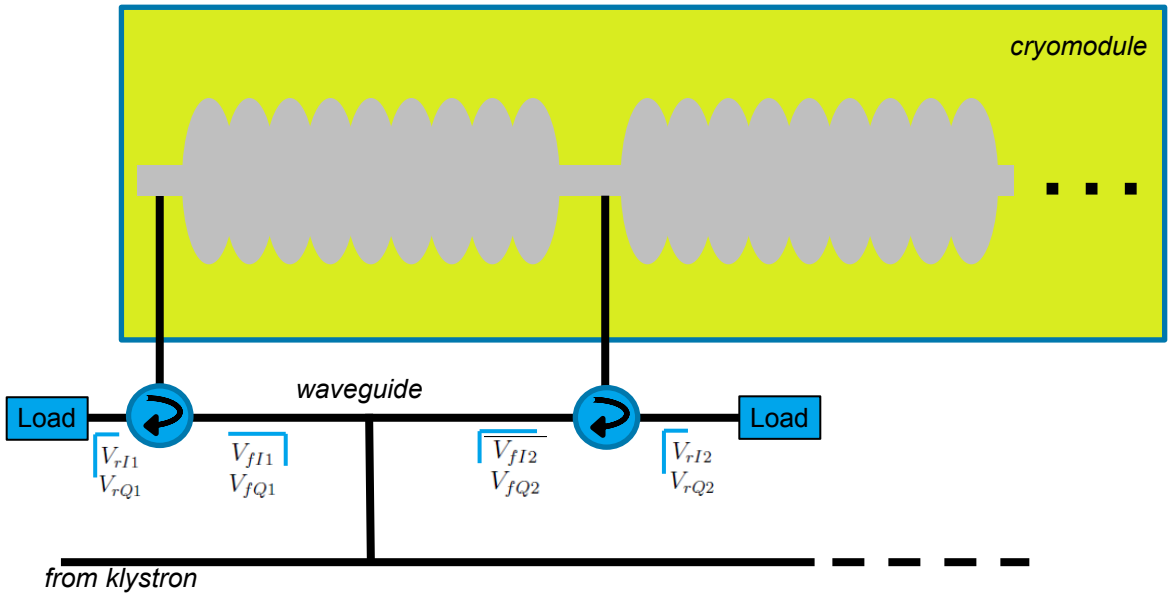
Pzt function block diagram (proposal)



Controller (Master) functional block diagram (proposal)



Calibrated waveguide signals (online)



- Coupling of cavity pairs on a waveguide branch
- Directivity of the couplers
- Required for virtual probe and detuning computation
- Should be implemented on uTC signal entry level

- 8x8 Matrix for 2 cavity channels
- 16 cavities for 1 uTC board, 9MHz
- Estimation: 256 DSP slices
  - One matrix for 4 channels
  - Optimization might further reduce size
  - 40% of FPGA size !!

$$\begin{pmatrix} V_{fI1c} \\ V_{fQ1c} \\ V_{rI1c} \\ V_{rQ1c} \\ \hline V_{fI2c} \\ V_{fQ2c} \\ V_{rI2c} \\ V_{rQ2c} \end{pmatrix} = \left(\begin{array}{cccccccc} 1 & 0 & c_{13} & c_{14} & c_{15} & c_{16} & c_{17} & c_{18} \\ 0 & 1 & c_{23} & c_{24} & c_{25} & c_{26} & c_{27} & c_{28} \\ c_{31} & c_{32} & 1 & 0 & c_{35} & c_{36} & c_{37} & c_{38} \\ c_{41} & c_{42} & 0 & 1 & c_{35} & c_{46} & c_{47} & c_{48} \\ \hline c_{51} & c_{52} & c_{53} & c_{54} & 1 & 0 & c_{57} & c_{58} \\ c_{61} & c_{62} & c_{63} & c_{64} & 0 & 1 & c_{67} & c_{68} \\ c_{71} & c_{72} & c_{73} & c_{74} & c_{75} & c_{76} & 1 & 0 \\ c_{81} & c_{82} & c_{83} & c_{84} & c_{85} & c_{86} & 0 & 1 \end{array}\right) \begin{pmatrix} V_{fI1} \\ V_{fQ1} \\ V_{rI1} \\ V_{rQ1} \\ \hline V_{fI2} \\ V_{fQ2} \\ V_{rI2} \\ V_{rQ2} \end{pmatrix}$$

Extract of software projects

- Important things to be done now:
  - Full test of crate setup, measurements of possible transfer rates
  - Quench detection server, later connection to online dw, QI detection ?
  - VS calibration server, fast calibration procedure necessary for XFEL
  - Piezo server and corresponding automation (first CMTB then ACC1)
  - Full test of crate setup, estimation of transfer rate
  - Beam based integration → shifts in July
  - Finite state machine for uTCA operation (needed also for REGAE ?)
- Cavity / cryomodule info server including:
  - Cavity values (QI, roQ, …), Quenching thresholds, model, general information
  - Displayed and accessed by DOOCS, interconnected to libraries
- Cavity status server, fast detection and information
  - Displaying on operator panel main parameters and combinations of alarm flags
- Panel renovation, also in focus of XFEL operability
  - large scale, generic for individual structure, GUN, 1- 4 cryomodules per RF station, …

To be discussed and decided

- Development only for uTCA, VME is only maintained
  - Allowing different server structure or even reconstruct for optimization
  - Long term project, demands definition of clear interface
- How should data be stored in DAQ system
  - 9MHz, 1MHz, … ; A/P or I/Q; usage bug fixing, failure detection, measurement support
- Should we fix the firmware implementation, e.g. ADC board
  - Collecting upgrades to make later and new upgrade
  - Firmware modular design and documentation → goal that all programmers could easily access and modify code
- Agreement to have same firmware and server structure for all applications
  - Additional features like REGAE laser control will be modular included?