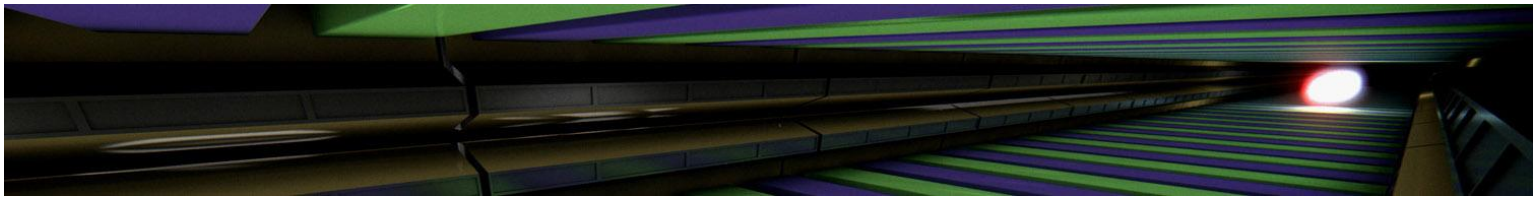


Laser synchronization firmware and software

Tomasz Kozak

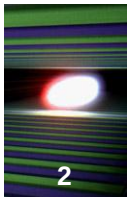
for the LbSync Team

(P. Prędki, S. Schulz, T. Lamb, M. Felber)

System Integration - LLRF Collaboration Meeting

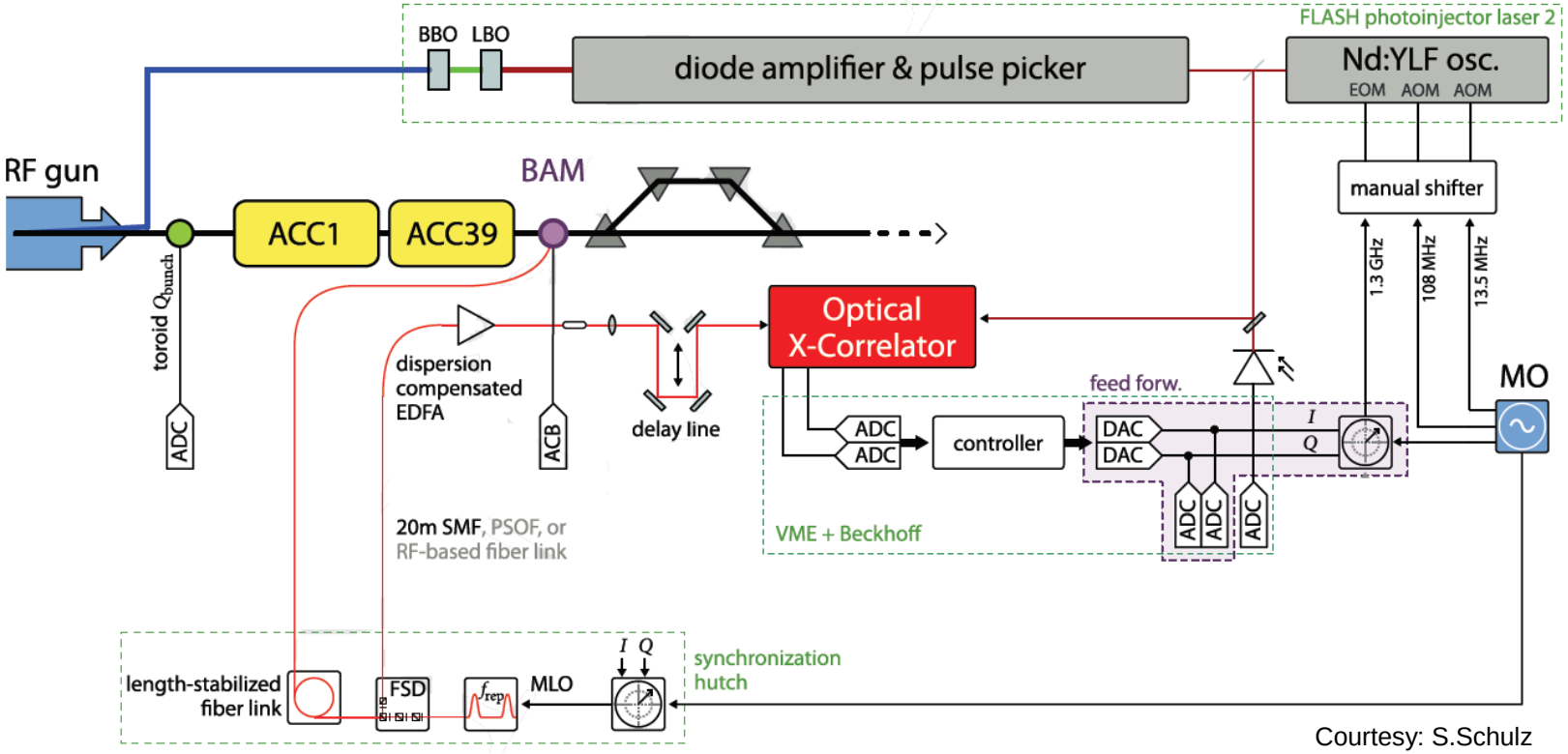
Warszawa, 16.12.2011

Agenda



- Optical Cross-Correlator (OXC) software
  - Introduction
  - Current status and future development
- VME based DSP System firmware and software for Optical Synchronization
  - Introduction
  - Current status and future development
- RF Lock Server for Laser Locking
  - Introduction
  - Current status and future development
- uTCA migration
- Summary

OXC Server - Introduction



Courtesy: S.Schulz

OXC provides:

- Information about pulse arrival time on photocathode with respect to MLO
- Possibility of implementing adaptive feed forward and fast feedback loops on laser arrival time

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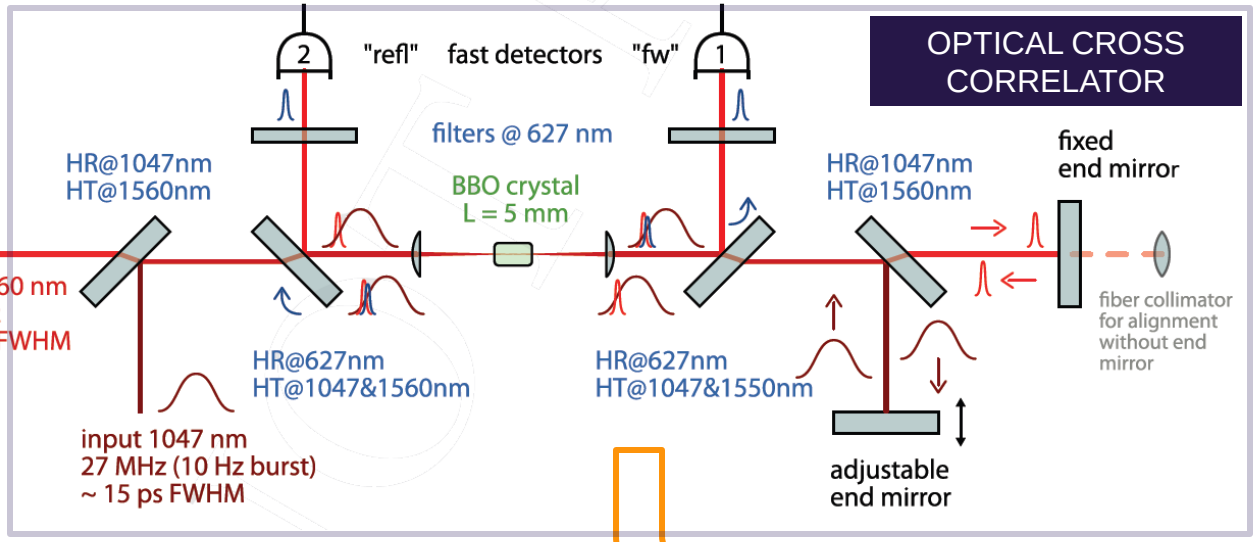
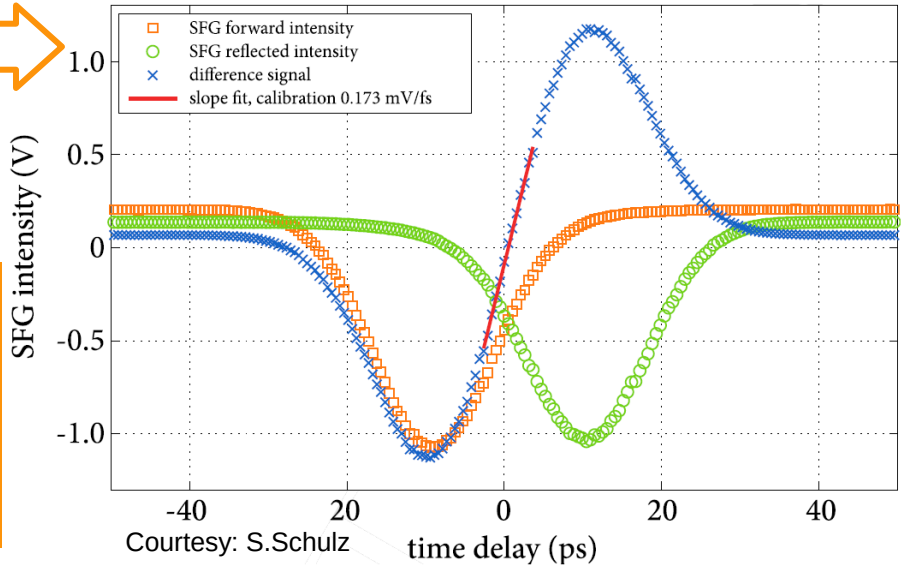
OXC Server – Introduction pt.2



Courtesy: S.Schulz

$$T_{arr} = K_{OXV} \bullet V_{OXC} = \frac{\partial V_{OXC}}{\partial t}|_{t=0} \bullet (V_{SFG,1} - V_{SFV,2})$$



Determine calibration coefficient methods:

A) scan the MLO VM

B) scan the PTO VM

C) scan motorized delay stage

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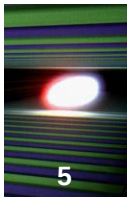
OXC Server – Current status



SlowPILOX (**Slow P**hoto **I**njector **L**aser **O**ptical **C**ross **C**orrelator) middle layer server:

- performs full range calibration
- performs periodical recalibration (keeps OXC within dynamic range)
- stabilizes the optical reference power
- calculates arrival time (mean, std. dev)
- held exceptions:
  - SFG signals missing
  - MLO VM setting change
  - MLO not lock or incorrect bucket
- auto-positioning of delay stage
- extensive logging and servers' status mechanism
- history of Koxc, 'zero-crossing', mean etc.

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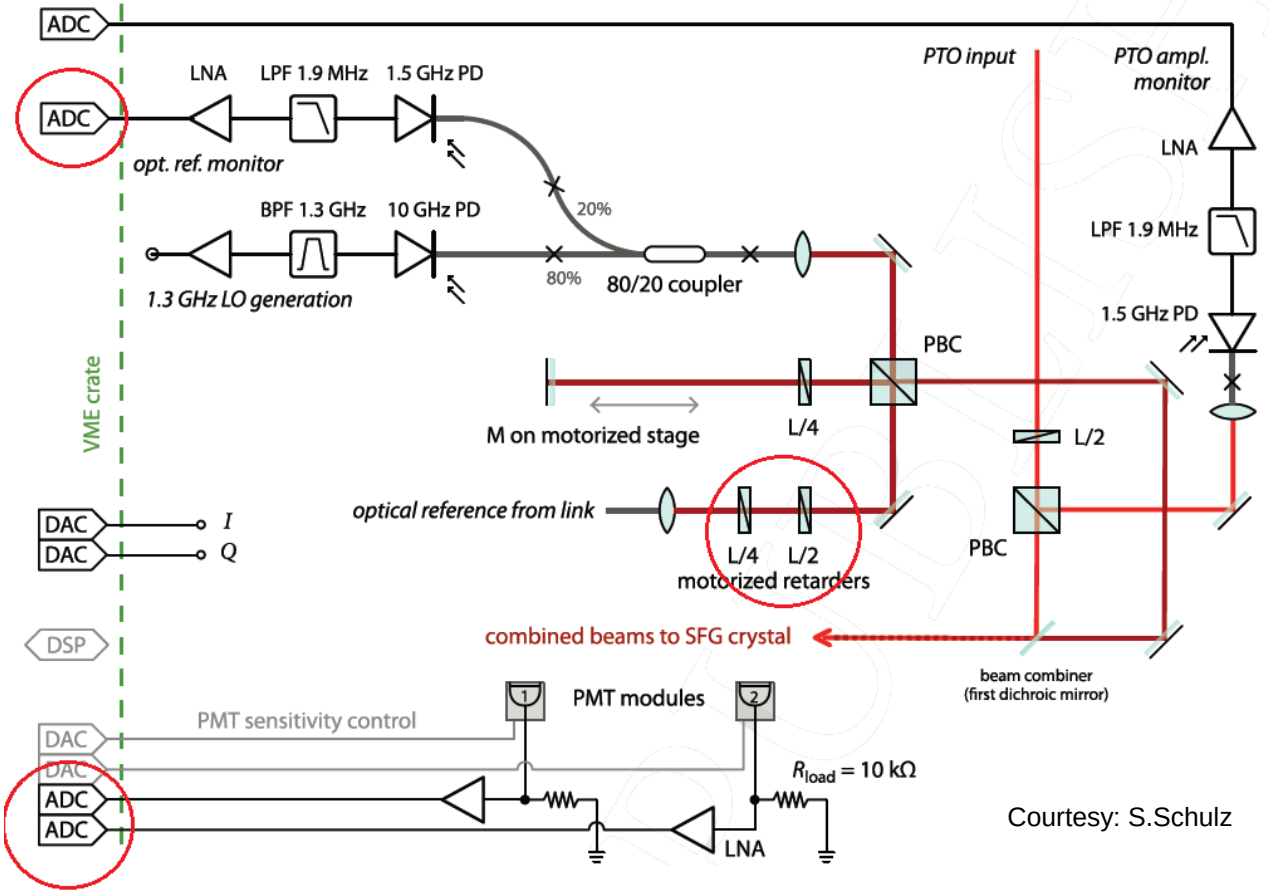
OXC Server – Current status pt.2

SlowPilox controls the motorized delay stage, motorized L2 and L4 retarders, cooperates with other DOOCS servers (e.g. RF Lock Server)



Courtesy: S.Schulz

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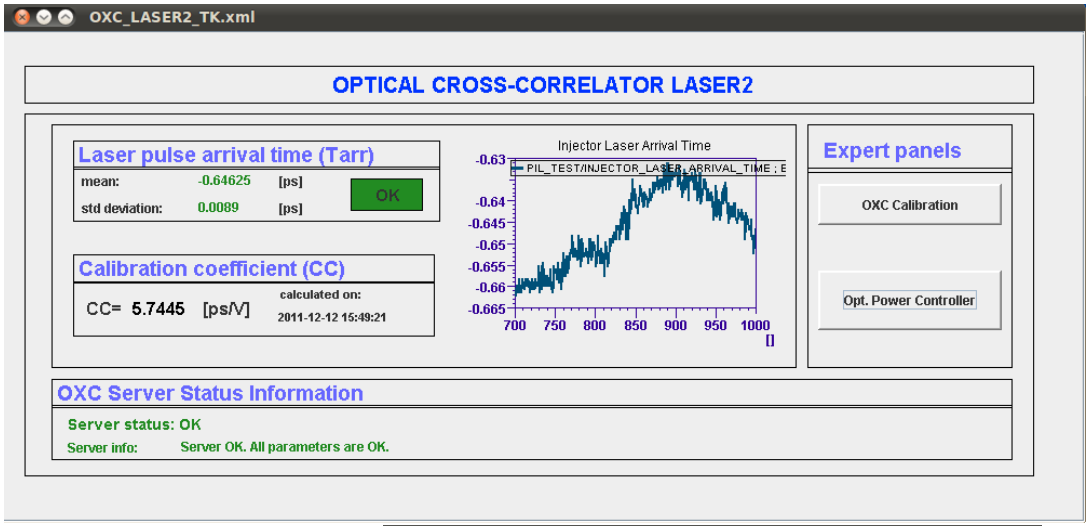
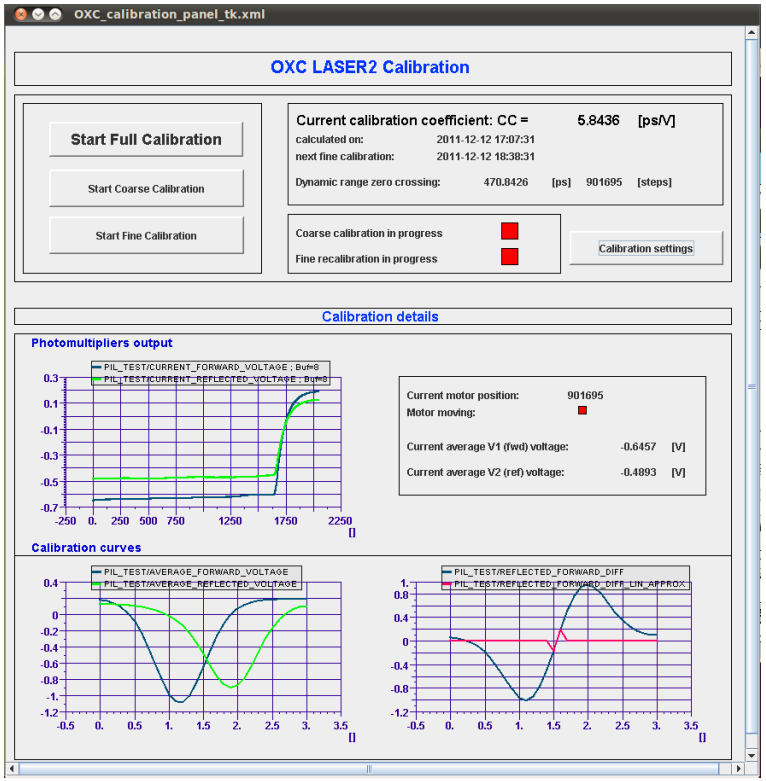
OXC Server – Current status pt.3

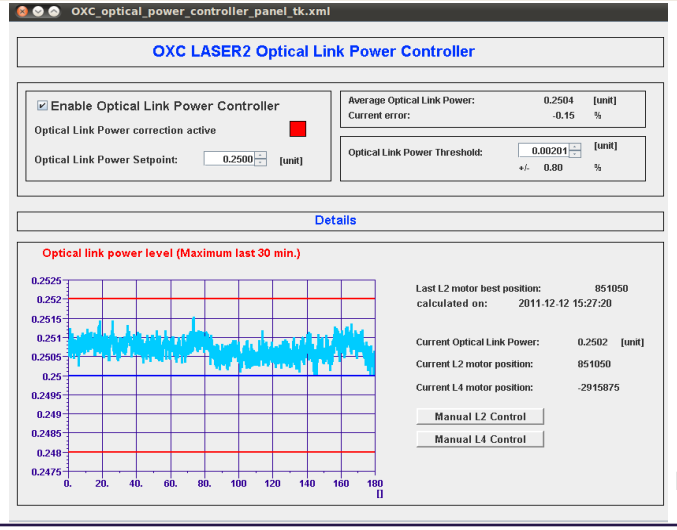
Set of JDDD pannels for the server.



Main OXC pannel



Main OXC callibration pannel



Main optical power pannel

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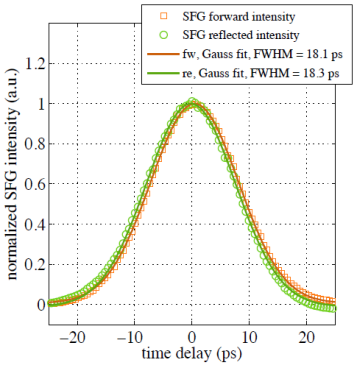
OXC Server – Future development

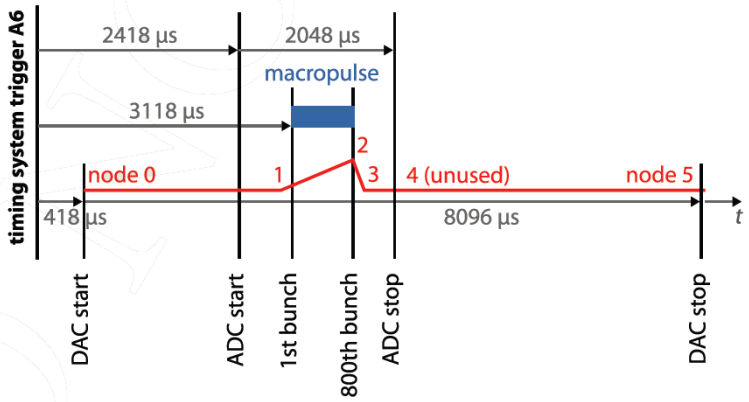
Future work for SlowPILOX:

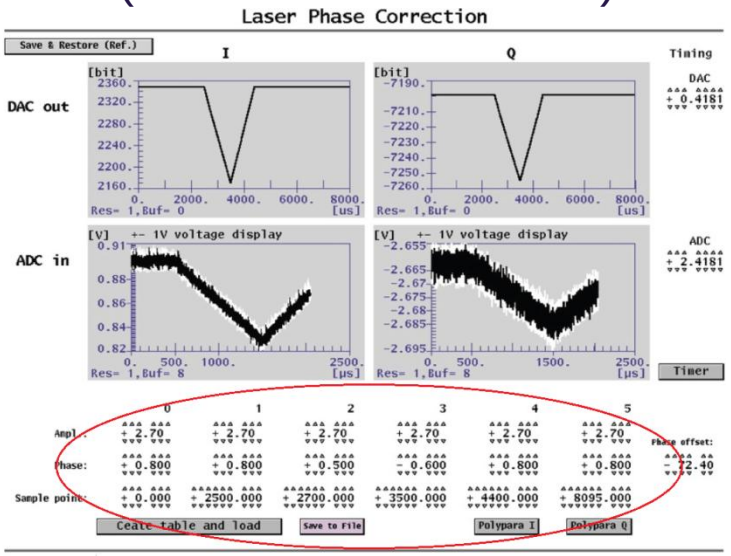
- Implemetation of pulse duration measurement by Gaussian fit of full range scan charasteristic.



Courtesy: S.Schulz

- Implementation of phase slope control for PTO VM (DAC8 server included)





- Timeline: finish these upgrades till end of 2011

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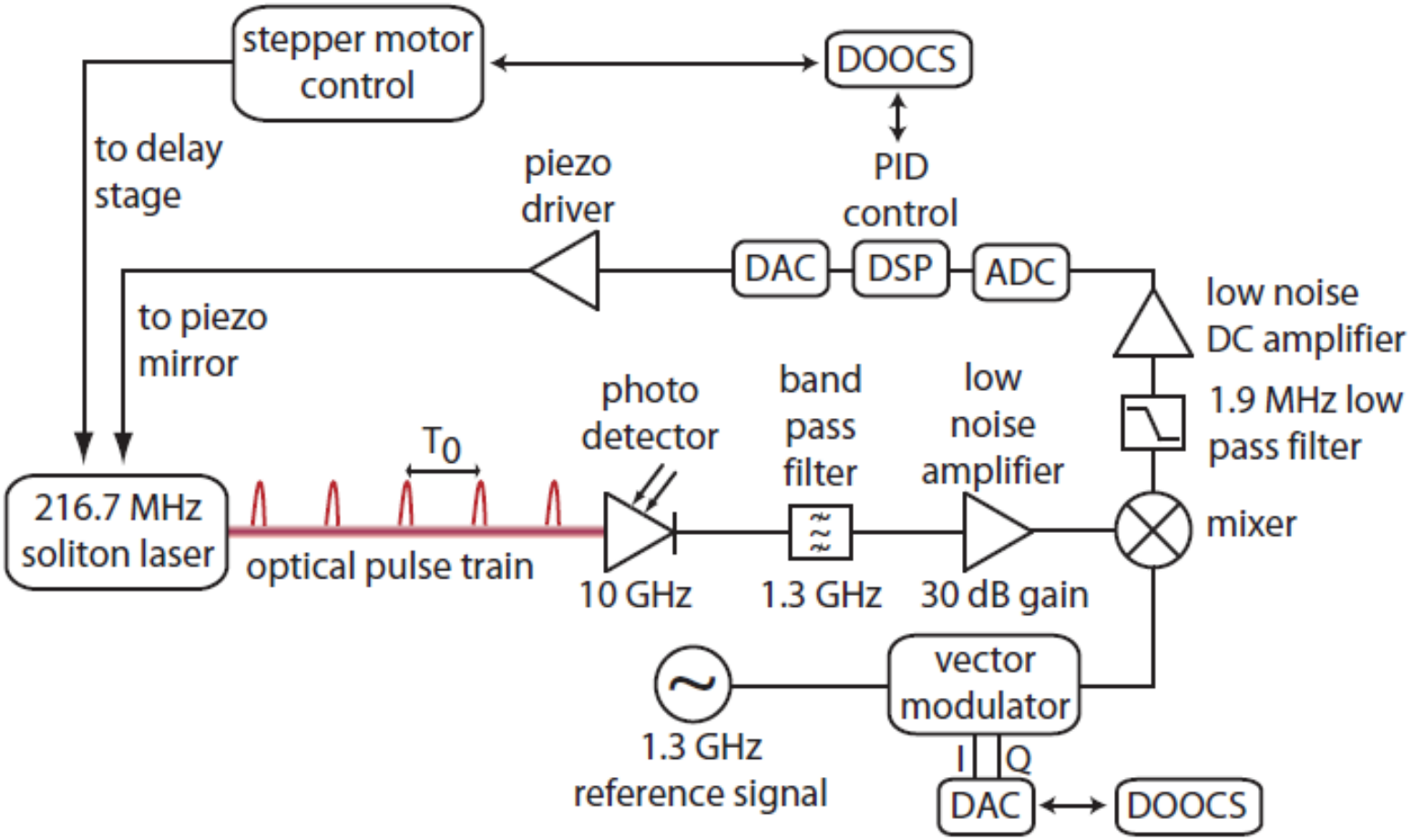
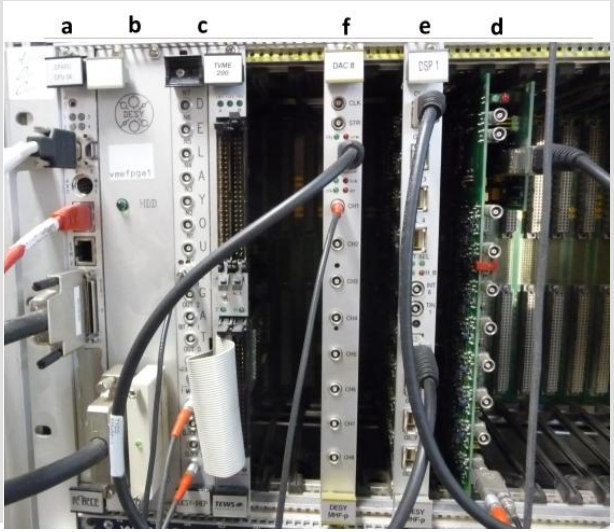
DSP Firmware and Software – Introduction



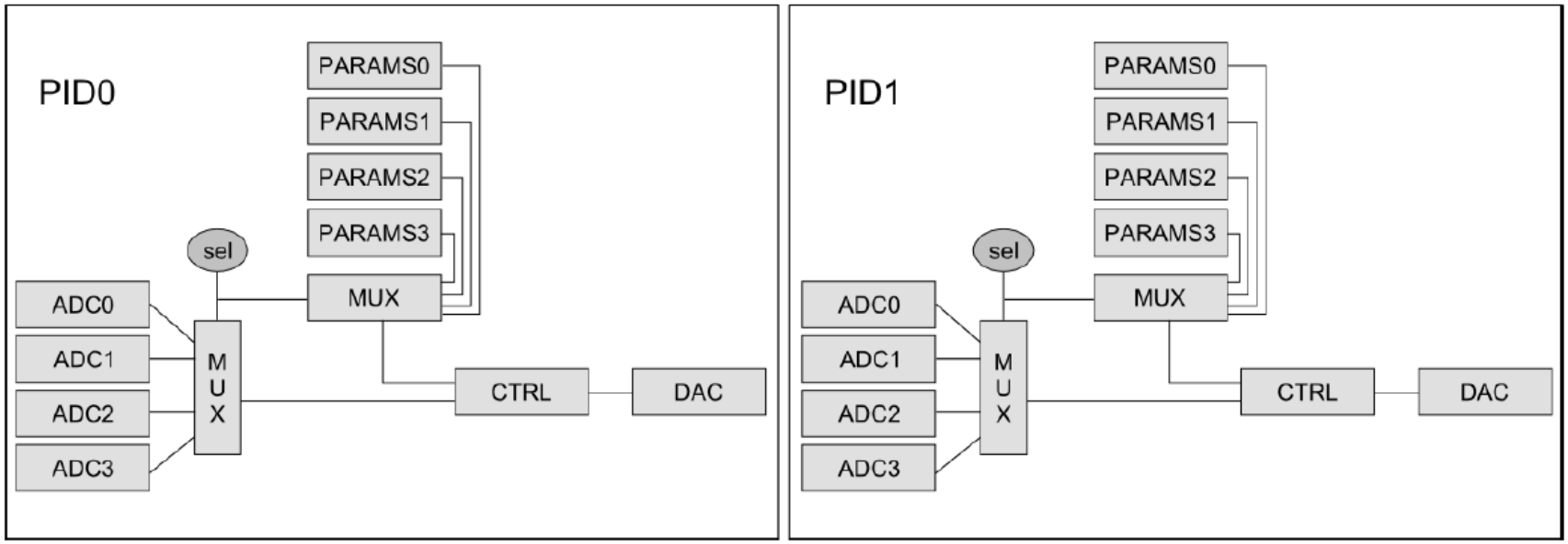
DSP Firmware and Software – Introduction

It is based on old hardware (VME):

- ADC board - 8-channel, 14-bit, up to 10 MSamples/s;
- All channels used in the system, 1 MHz clock used
- DAC board - 8-channel, 14-bit; Only two outputs available due to design flaws
- DSP - TMS320C6701 Texas Instruments chip, 164 MHz
- All boards are DESY-made - not available commercially

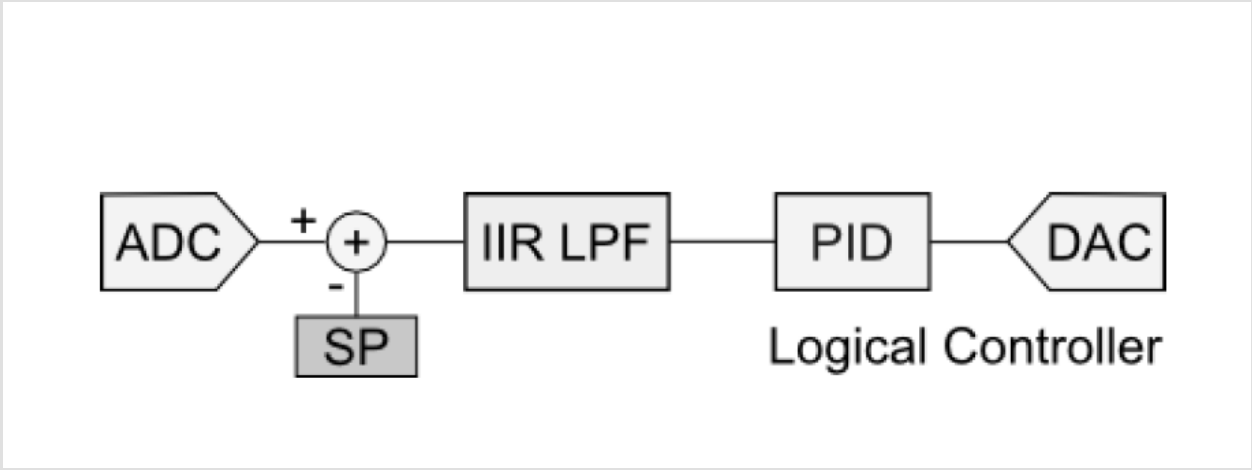


DSP Firmware and Software – Status



- Two 'logical' PID controllers in the DSP
- Each controller: Input selectable from up to 4 ADC channels; PID gains, set-points, separate for each input
- Simple switching between inputs - happens
- sample-to-sample
- One can be switched off to improve processing rate of the other one

DSP Firmware and Software – Status



- First-order IIR filter of the error signal
- Discrete PID controller
- Integrator anti-windup done by output back-calculation
- Output clipping to settable minimum / maximum values

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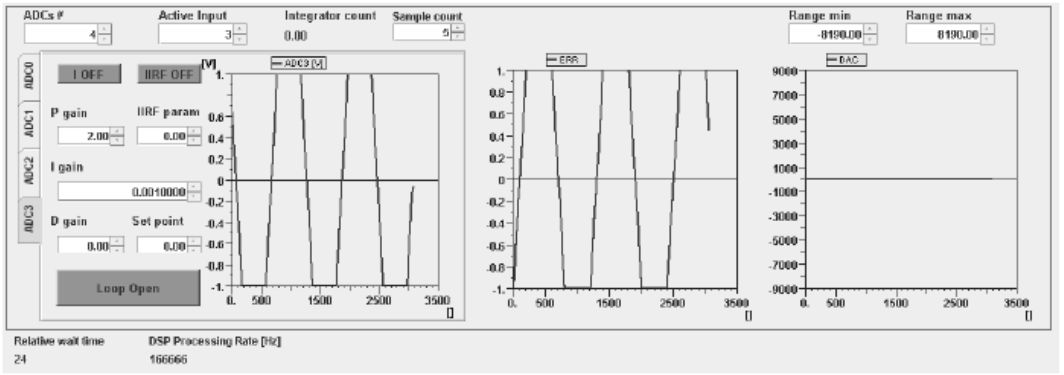
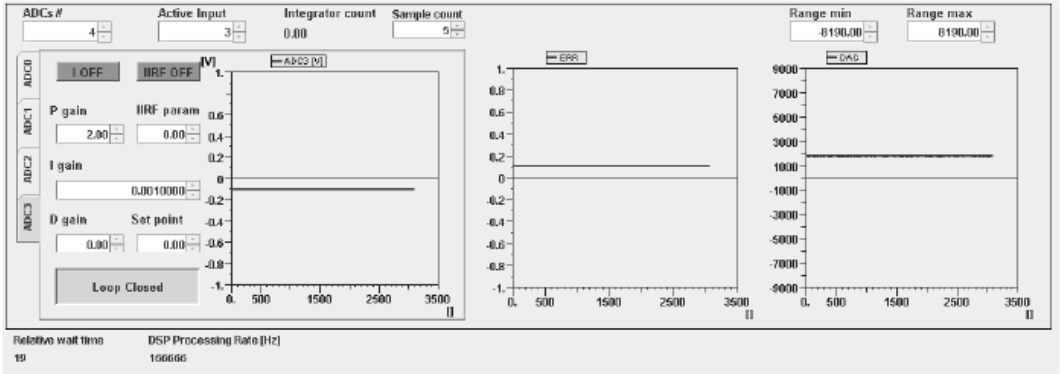
DSP Firmware and Software – Status



Control loop open - no control action taken (approx. 140 Hz mismatch)



Control loop closed - integrator disabled (phase mismatch)

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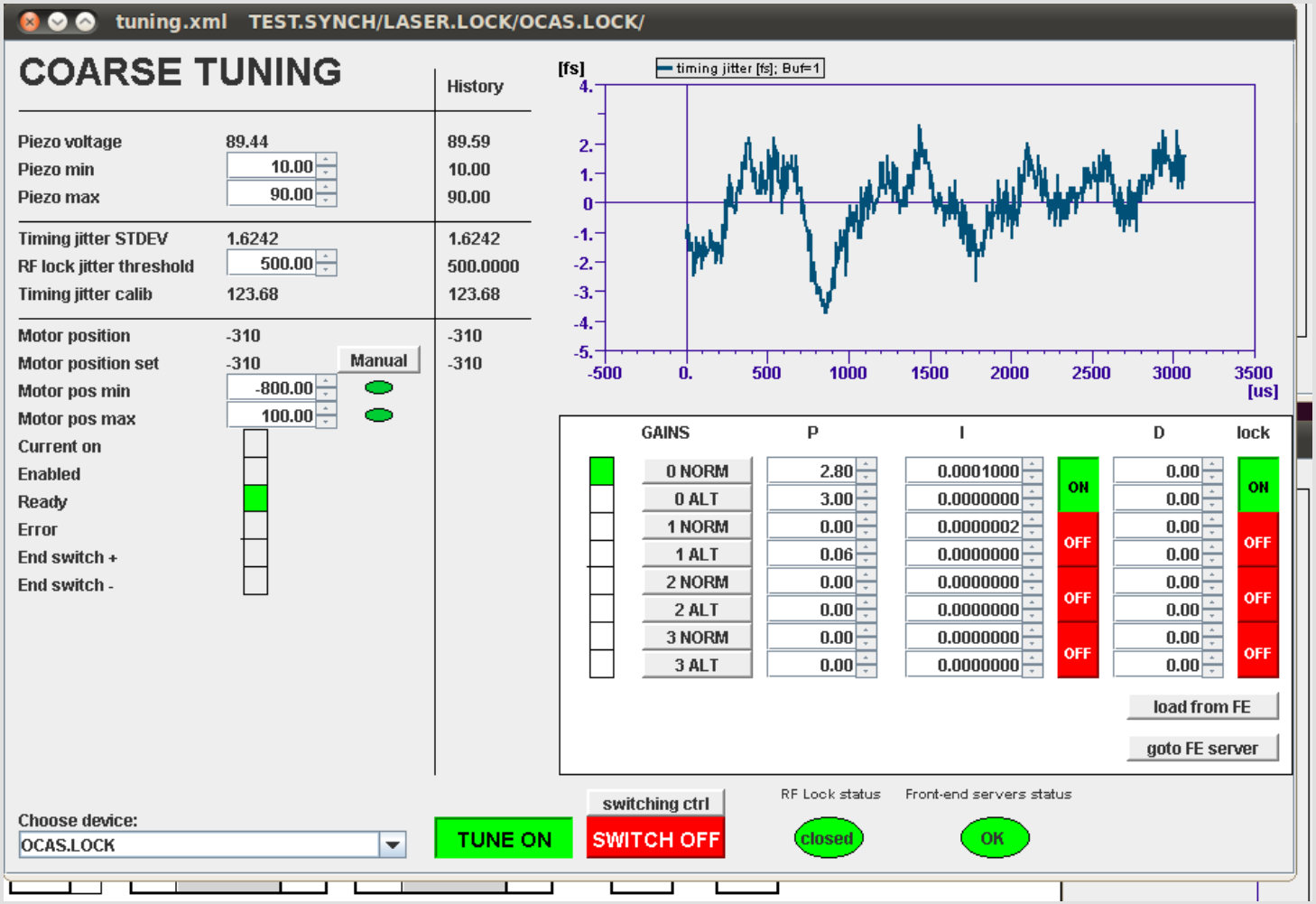
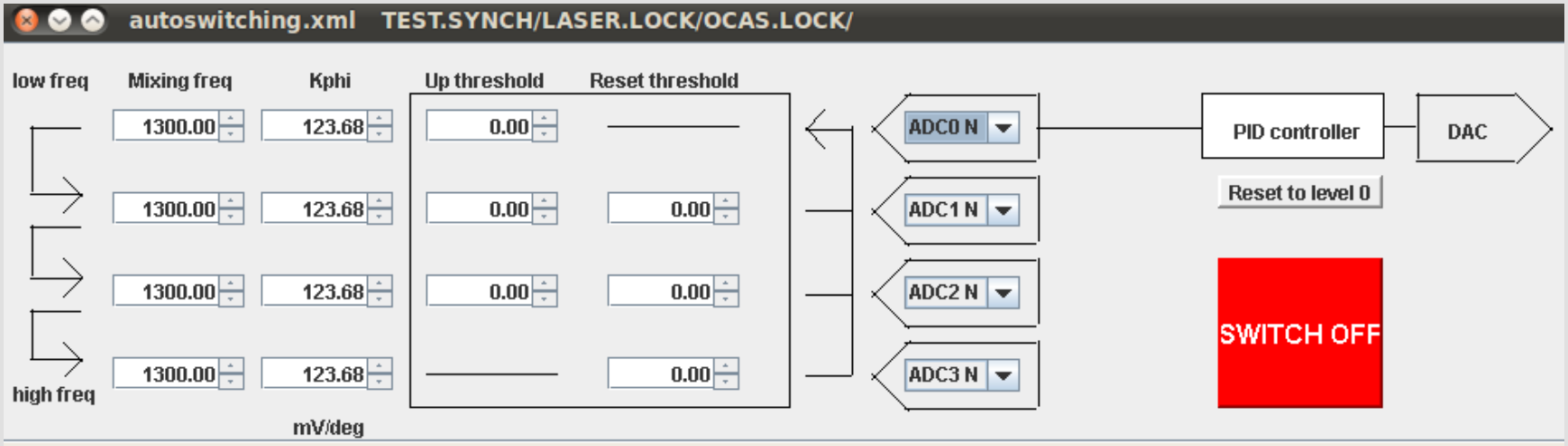
RF Lock Server for Laser Locking



RF Lock Server for Laser Locking – Status

Locking to diffrent frequencies:



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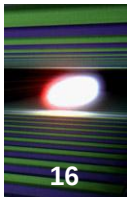
uTCA migration



The set of crates for LbSynch has been ordered

- A lot of work to be done with front-ends servers
- The special structure controller needs to be prepared (P.Predki)
- Needs to consider more IT engineering

Code	Device	PP Laser	Lab 28g EO Laser	INJ Laser	Synchr. Hutch	Lab 28g OCAS, BAM devel.	Lab 26a MLO laser	EOD
07	Crate	Powerbridge RackPak/M4-2	Schroff vertical, 12 slot, 9U	Schroff vertical, 12 slot, 9U	Powerbridge RackPak/M4-2		Schroff vertical, 12 slot, 9U	Schroff vertical, 12 slot, 9U
10	MCH	NMCH-Basic V3.4	NMCH-Basic V3.4	NMCH-Basic V3.4	NMCH-Basic V3.4		NMCH-Basic V3.4	NMCH-Basic V3.4
09	Power Supply	Vadatech	Vadatech	Vadatech	Vadatech		Vadatech	Vadatech
11	CPU	AMC-1000/7400/M2G	AMC-1000/7400/M2G	AMC-1000/7400/M2G	AMC-1000/7400/M2G		AMC-1000/7400/M2G	AMC-1000/7400/M2G
22	Storage	San Blaze	San Blaze	San Blaze	San Blaze		San Blaze	San Blaze
13	Timing	x1Timer	x1Timer	x1Timer	x1Timer		x1Timer	x1Timer
29	DAMC2	DAMC2	DAMC2	DAMC2 (x2)	DAMC2			DAMC2
30	RTM	DAMC2 RTM	DAMC2 RTM	DAMC2 RTM (x2)	DAMC2 RTM			DAMC2 RTM
21	TMCB				TMCB (x4) (TL)			
26	uRFB_In					uRFB Input Test Board		
27	uRFB_Out					uRFB Ouput Test Board		
28	FDCAR					Phase Drift Comp. Amp. Repeater		
23	PSM							PSM DESY
15	uADC							SIS8300 v 2.0
18	uDWC							DWC8300 v1.1 1.3GHz
	DEADLINE	ASAP	ASAP	ASAP	ASAP		III.2012	ASAP

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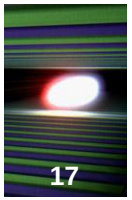
Main problems

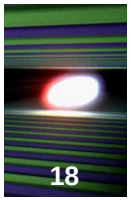


No good documentation

No block diagrams of all system

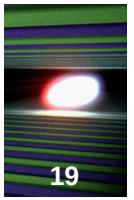
All knowledge from some experienced people (maily from PhD theses)

Thanks



Thank you for your attention

Clip board – copy and paste



Headline

- first level
  - second level
    - ➔ third level

Headline

Texttext texttext texttext texttext texttext texttext

Keyword

1. Keyword
2. Keyword

- keyword
- keyword

Result Headline

- result text
- result text

Result headline

Result text, result text, result text

Result headline

- result text
- result text
- result text