MIMO controller implementation for xTCA

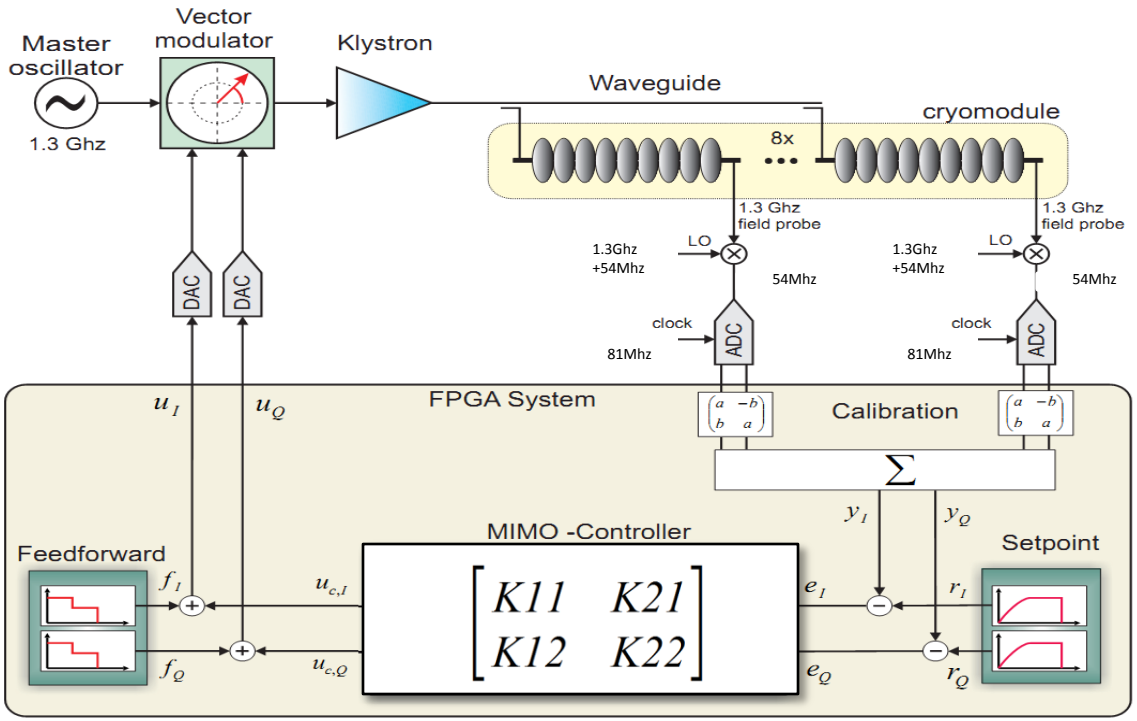
Lukasz Butkowski

Warsaw 16.12.2011

Outline

- Introduction
- MIMO architecture
- Filters architecture
- VHDL entity
- Test setup
- Test result
- Summary

Introduction



MIMO feedback control system

MIMO controller for xTCA should work for 9MHz sample rate.

Introduction

$$\begin{bmatrix} I_{out} \\ Q_{out} \end{bmatrix} = \begin{bmatrix} K11 & K21 \\ K12 & K22 \end{bmatrix} \cdot \begin{bmatrix} I_{in} \\ Q_{in} \end{bmatrix}$$

$$K11 = \frac{b_{0k11} + b_{1k11} \cdot z^{-1} + b_{2k11} \cdot z^{-2}}{1 + a_{1k11} \cdot z^{-1} + a_{2k11} \cdot z^{-2}}$$

$$K12 = \frac{b_{0k12} + b_{1k12} \cdot z^{-1} + b_{2k12} \cdot z^{-2} + b_{3k12} \cdot z^{-3} + b_{4k12} \cdot z^{-4}}{1 + a_{1k12} \cdot z^{-1} + a_{2k12} \cdot z^{-2} + a_{3k12} \cdot z^{-3} + a_{4k12} \cdot z^{-4}}$$

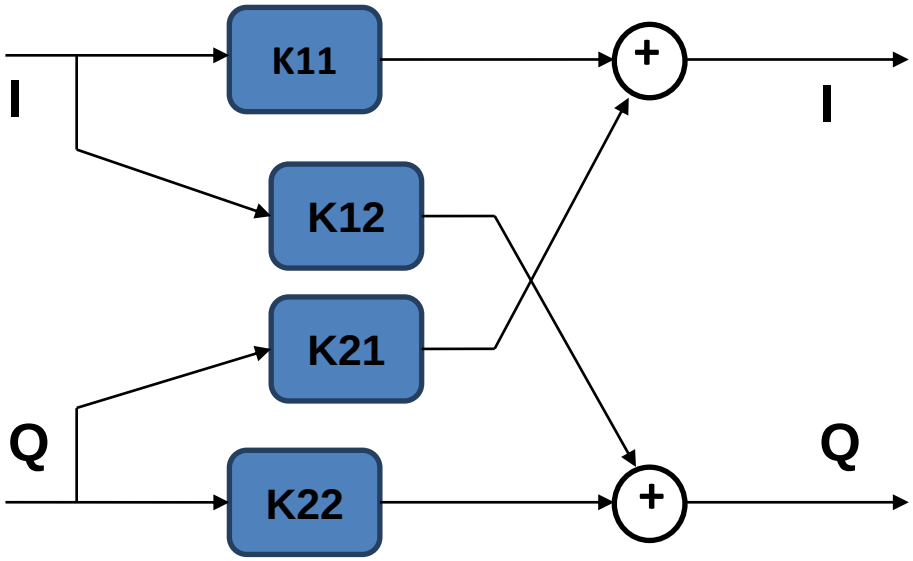
$$K21 = \frac{b_{0k21} + b_{1k21} \cdot z^{-1} + b_{2k21} \cdot z^{-2} + b_{3k21} \cdot z^{-3} + b_{4k21} \cdot z^{-4}}{1 + a_{1k21} \cdot z^{-1} + a_{2k21} \cdot z^{-2} + a_{3k21} \cdot z^{-3} + a_{4k21} \cdot z^{-4}}$$

$$K22 = \frac{b_{0k22} + b_{1k22} \cdot z^{-1} + b_{2k22} \cdot z^{-2}}{1 + a_{1k22} \cdot z^{-1} + a_{2k22} \cdot z^{-2}}$$

MIMO architecture

$$I_{out} = I_{in} \cdot K11 + Q_{in} \cdot K21$$

$$Q_{out} = I_{in} \cdot K12 + Q_{in} \cdot K22$$

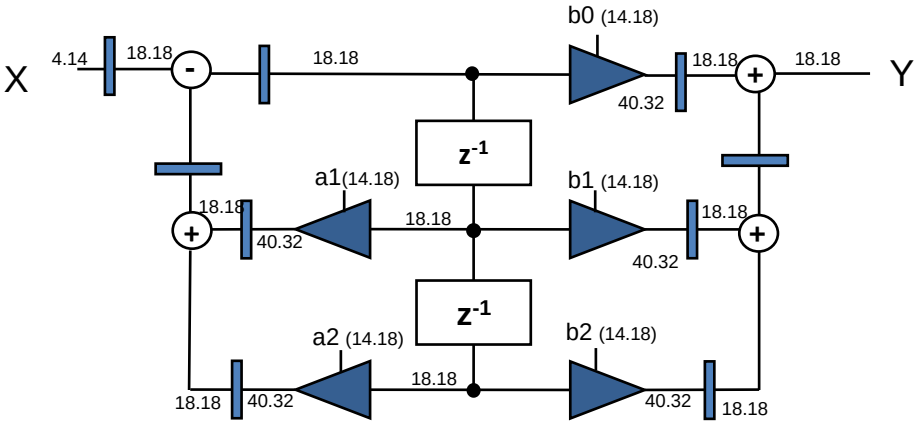


Block diagram of MIMO controller

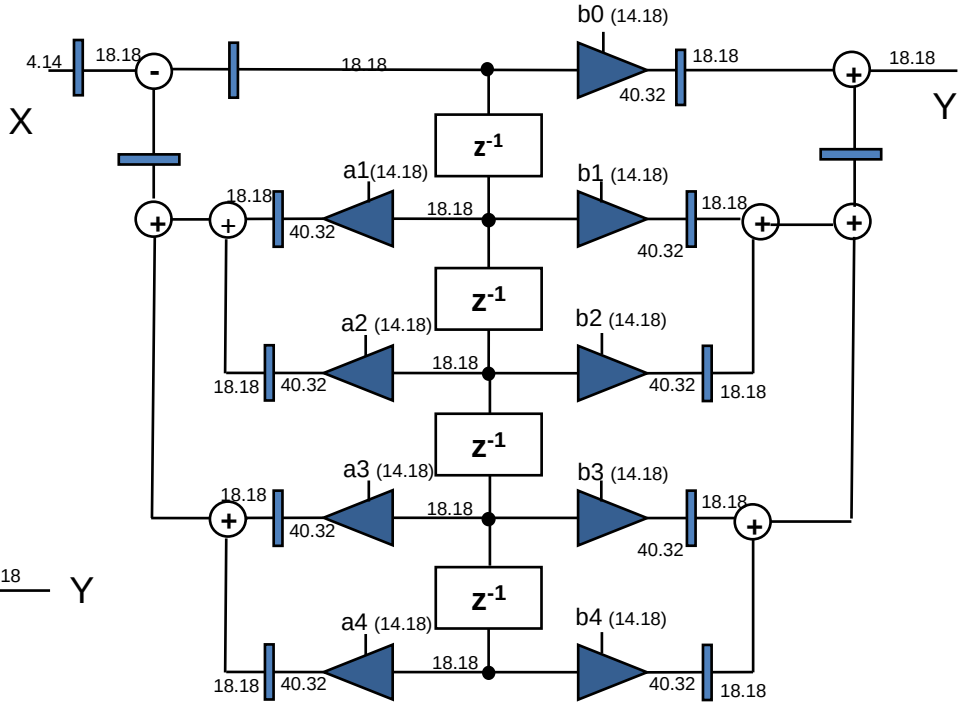
Filters architecture

Filters are implemented as Direct Form II structure IIR filter.

Current implementation has representation of the number:
-Coefficient: 32 bit number with 14bit integer and 18 bit fraction,
-Internal bus: 36 bit number with 18 bit integer and 18 bit fraction,
-Input/output signal: 18bit number with 4 bit integer and 14 bit fraction,



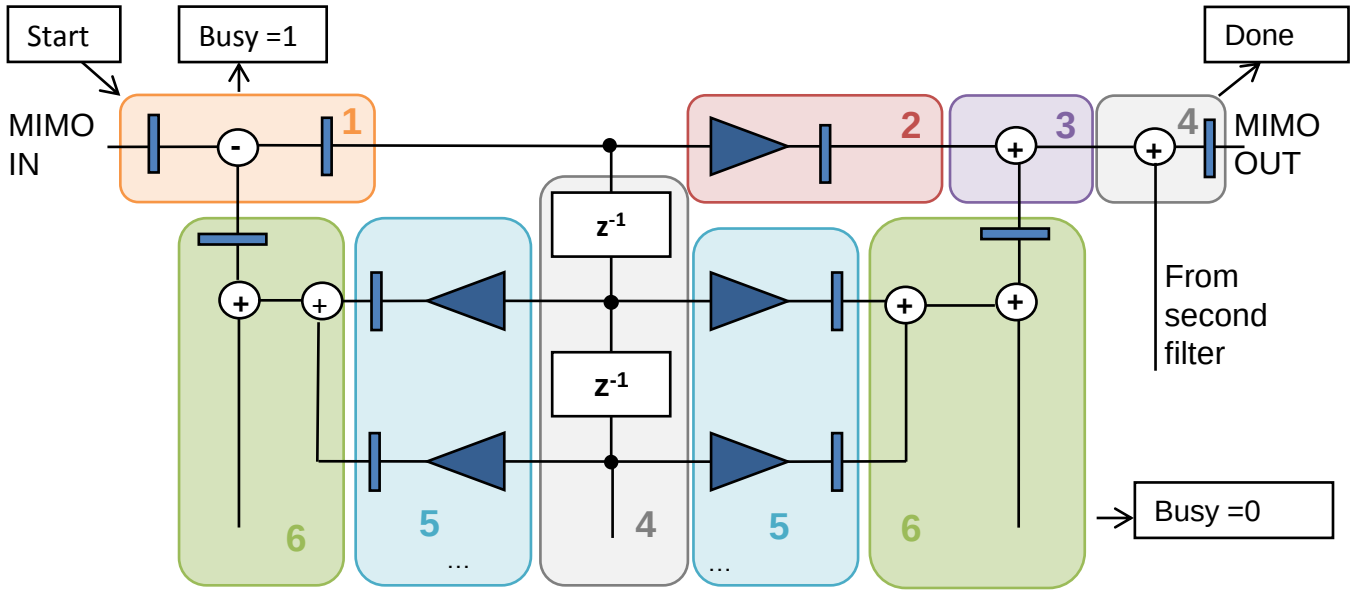
Block diagram of second order IIR filter



Block diagram of fourth order IIR filter

Filters architecture

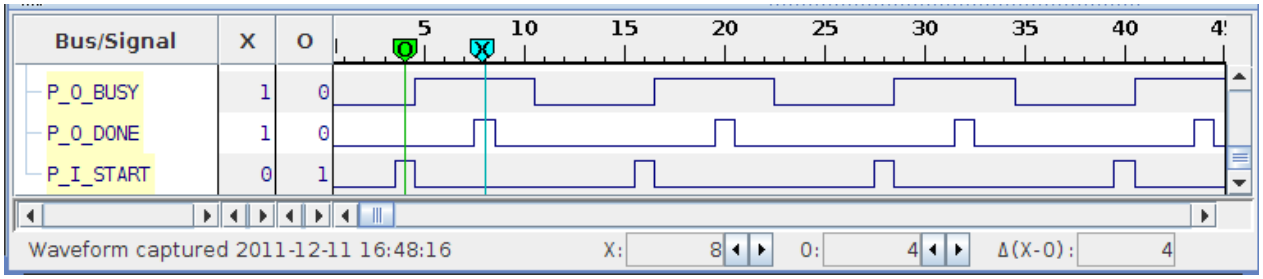
Filters are implemented separately.
All filters works in parallel mode.
Calculations in filter are done sequentially.



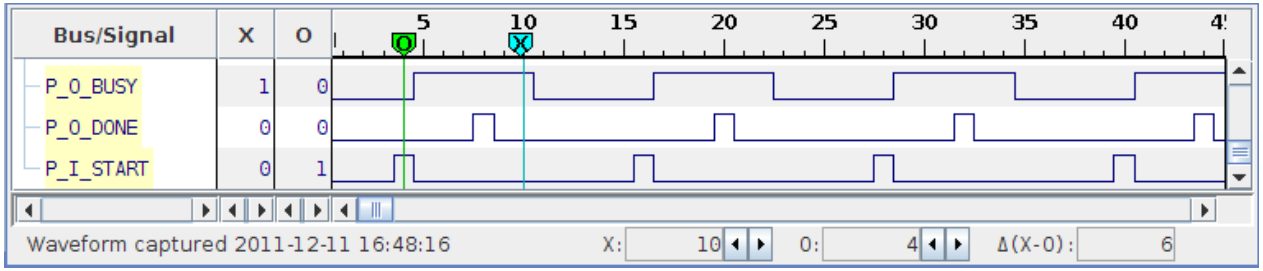
Filter calculation algorithm.

Calculation time

Delay time of calculation is 4 clock cycles and component is busy for next 2 cycles. For 81Mhz clock delay is 48ns and busy time is 72ns.



Delay time of MIMO calculation.



Busy time of MIMO controller.

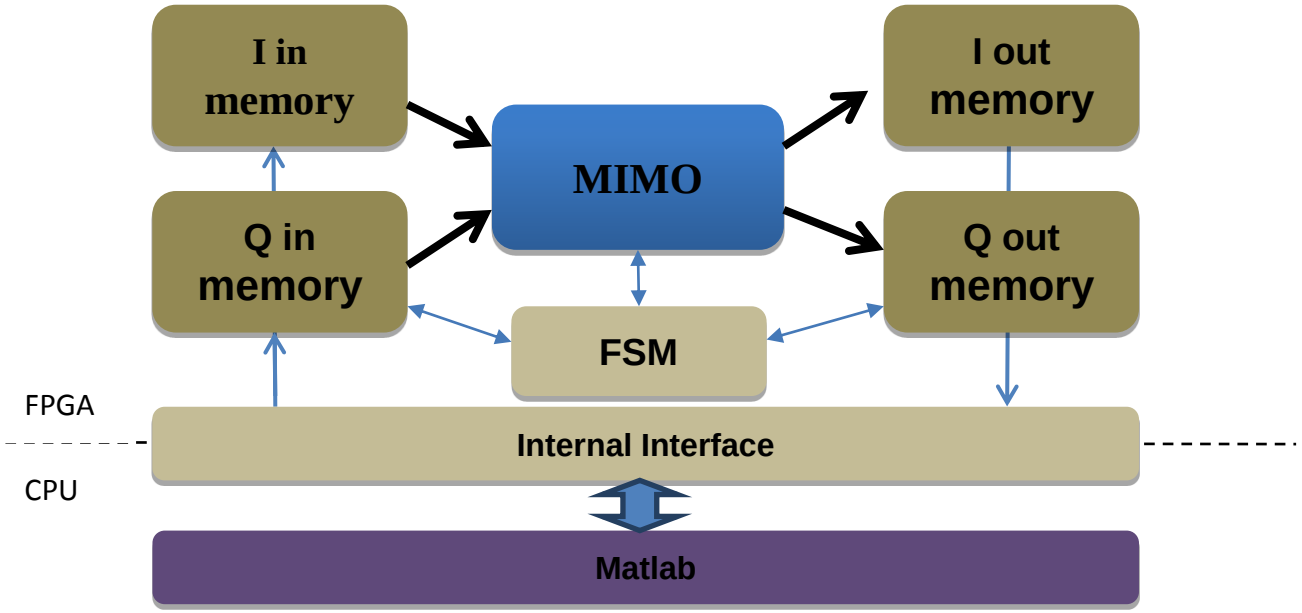
VHDL entity

```
entity ENT_MIMO is
    generic(
        GEN_DATA_WIDTH           : natural := 18; -- input/output data width
        GEN_COEF_FRACTION_LENGTH : natural := 18; -- fraction length of coefficient and internal data
        GEN_DATA_FRACTION_LENGTH : natural := 14; -- fraction length of input/output data
        GEN_DSP_DATA_WIDTH       : natural := 36  -- length of internal filters data width
    );
    port(
        P_I_CLK        : in std_logic;  -- clock input
        P_I_RESET_N    : in std_logic; -- reset input, active low

        P_I_START     : in std_logic; -- start sample calculation, active high
        P_I_I         : in std_logic_vector(GEN_DATA_WIDTH-1 downto 0); -- input I signal
        P_I_Q         : in std_logic_vector(GEN_DATA_WIDTH-1 downto 0); -- input Q signal
             -- coefficient inputs
        P_I_K11_COEF : T_32BitArray(4 downto 0); -- array of 32bits [b2 b1 b0 a2 a1]
        P_I_K12_COEF : T_32BitArray(8 downto 0); -- array of 32bits [b4 b3 b2 b1 b0 a4 a3 a2 a1]
        P_I_K21_COEF : T_32BitArray(8 downto 0); -- array of 32bits [b4 b3 b2 b1 b0 a4 a3 a2 a1]
        P_I_K22_COEF : T_32BitArray(4 downto 0); -- array of 32bits [b2 b1 b0 a2 a1]

        P_O_BUSY      : out std_logic; -- component busy out, active high
        P_O_DONE      : out std_logic; -- sample calculation done signal, active high
        P_O_I         : out std_logic_vector(GEN_DATA_WIDTH-1 downto 0); -- I out signal
        P_O_Q         : out std_logic_vector(GEN_DATA_WIDTH-1 downto 0)  -- Q out signal
    );
end ENT_MIMO;
```

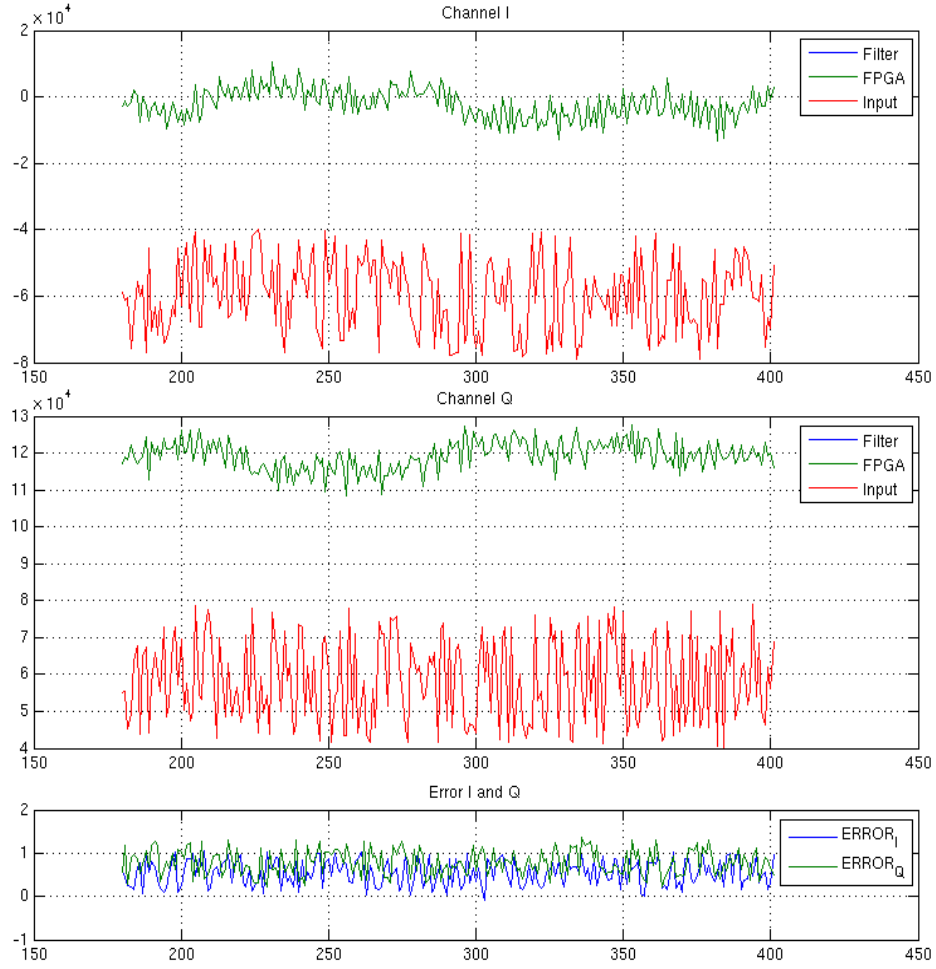
Test setup



Block diagram of MIMO test implementation

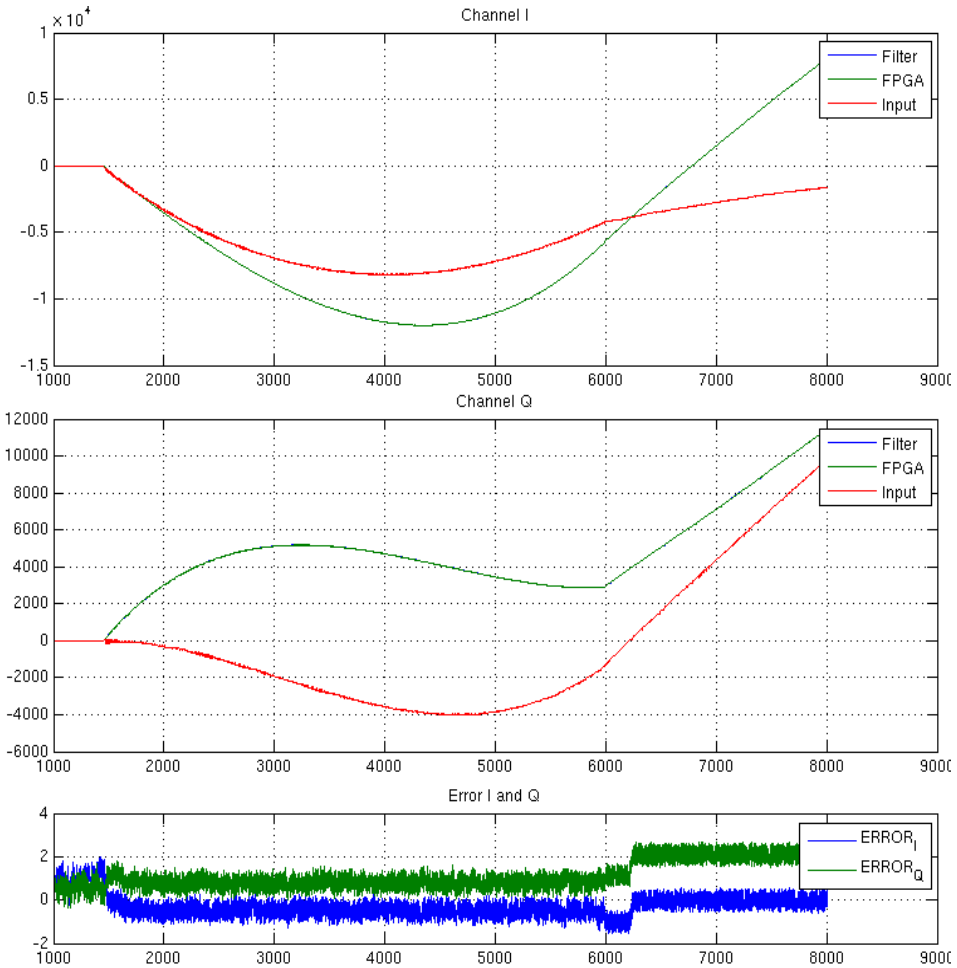
Test results

Filters error



Random signal

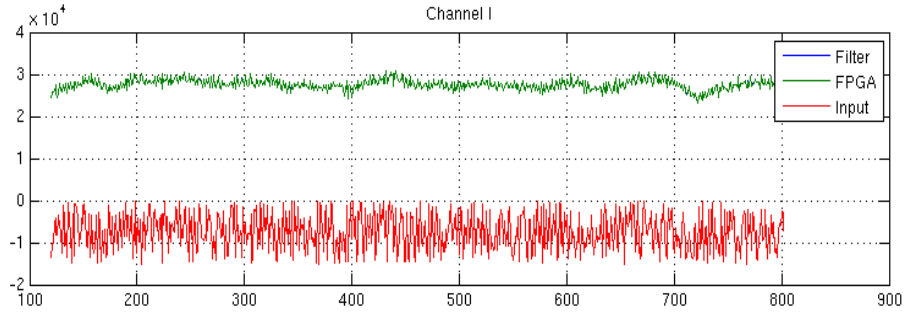
Quantized input, Quantized coefficients.

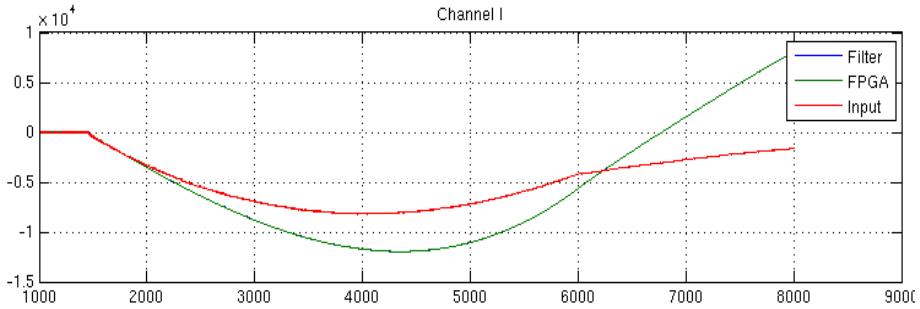


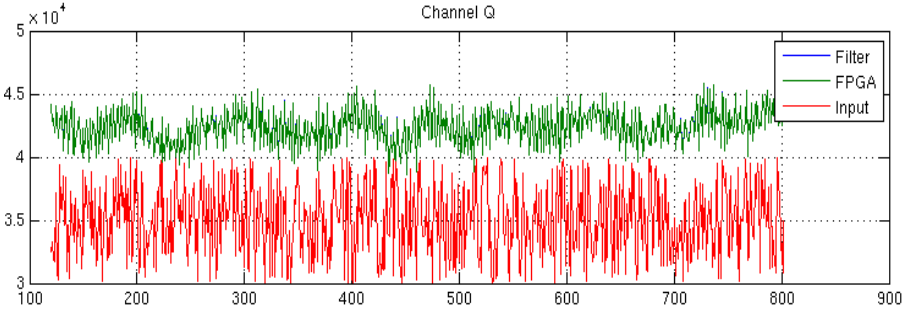
Example error signal from FLASH

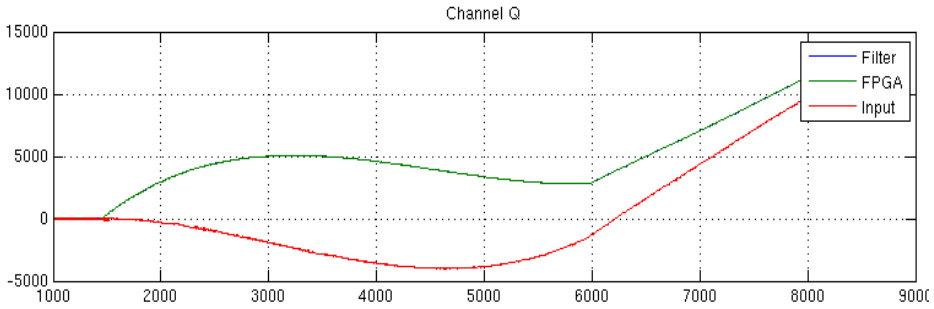
Test results

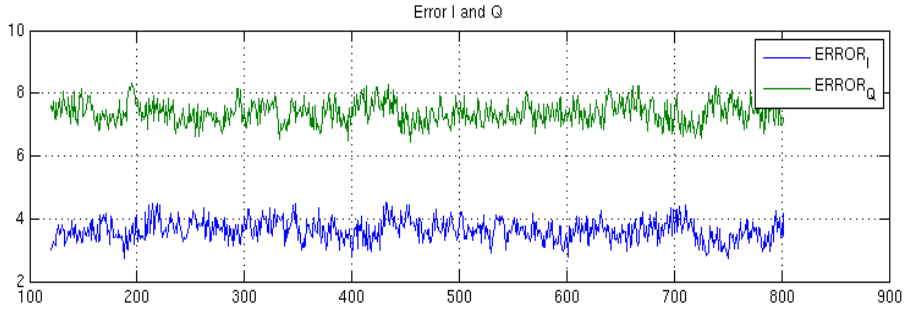
Coefficient quantization error Quantized input, non quantized coefficients.

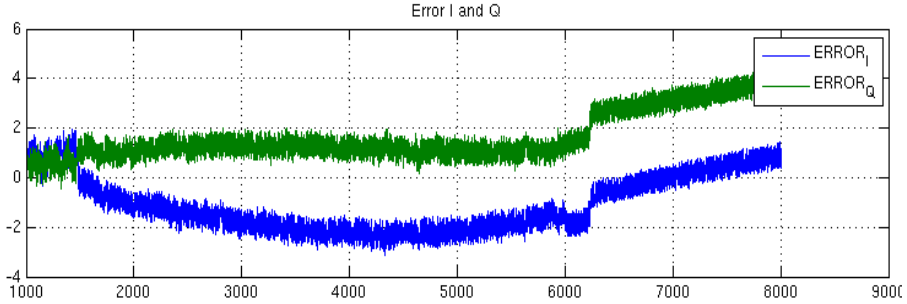






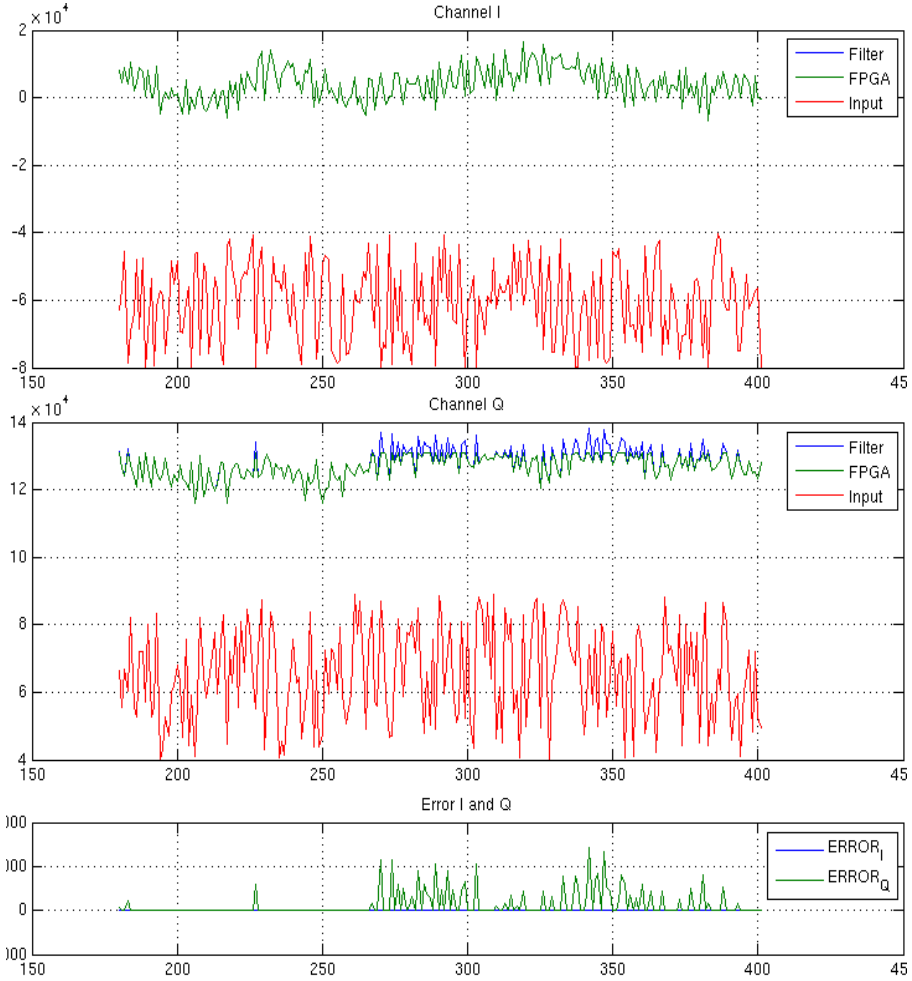




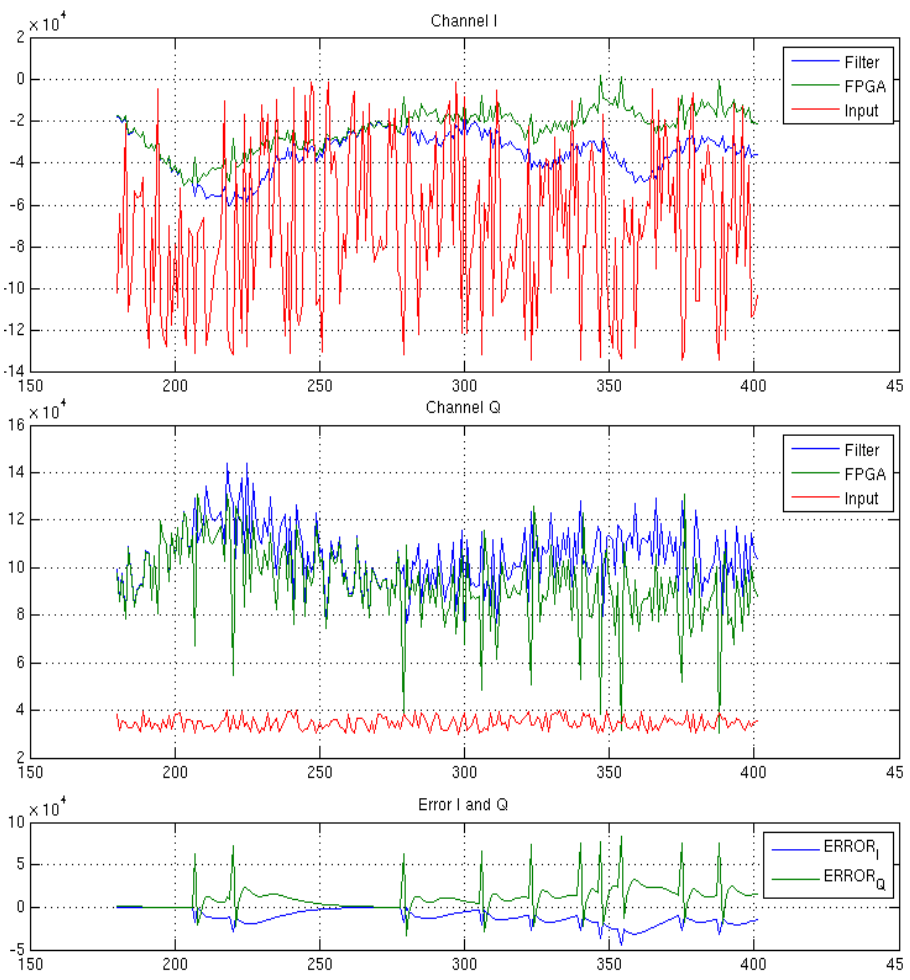


Test results

Overflows



Q output overflow



I input overflow (to high input level)

Summary

- **FPGA resources on uTC**

New MIMO implementation

			Old MIMO implementation(only second order filters)	
Registers:	**1985**	**3%**	**2234**	**3%**
LUTs:	**4779**	**8%**	**2281**	**3%**
DSP48Es:	**112**	**17%**	**80**	**12%**

- **MIMO works on 9MHz**
- **Second and fourth order filters are implemented**
- **Filters error is less then 2 bit**

Thank you for your attention