Working Group Hardware/ New SIS8300 Version

Group members: Frank, Samer, Uros

Split the development in two parallel activities

1. Activity (minor changes) – to be ready next year:
	1. Grounding and housing issues:
		1. Change layout around ADC-FE to be able to solder the housing/grounding for bypassing
		2. Do not mount SMAs and Harling on the front panel (no change on the layout there)
		3. Try to fit a metallic by-pass on the bottom of the board (talk to the layouter)
	2. CLK issues:
		1. Rearrange the clocks (1 chip feeds the ADCs the 2nd chip feeds the rest)
		2. Change the first clock with the first one
	3. ADC-FE:
		1. Change the transformers
	4. DC Regulators:
		1. Doesn’t change, except if there are GND chassis problems
	5. Miscellaneous:
		1. Other minor changes on the board defined by Frank’s list
2. Activity (Major Redesign):
	1. uTCA-pizza:
		1. Redesign of the zone 3 connector (diff. metallic shielded, connected to chassis ground)
		2. Repositioning of the ADCs, clock chips, DC power supplies, stack-up etc.
		3. Maybe remove DACs?
		4. Change placing on the DWCs
		5. Revision of all the components (obsolete?, better components? Etc.)
	2. Pizza (main idea is to see VS processing gain):
		1. Change of the form factor to a single PCB configuration – out of crate. More space to improve power dis., isolation, manipulation with return currents etc.