Progress in Chip Testing

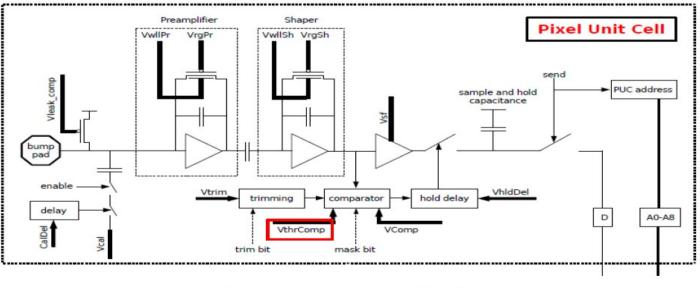
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CMS Tracker Upgrade 15.11.2011

- Threshold scan update
- Time walk
- Data buffer test
- Cross talk capacitance

Threshold Scan Procedure (reminder)

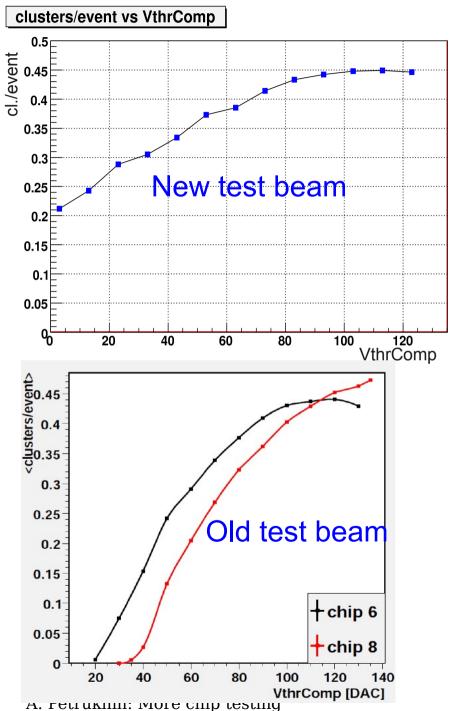
- DESY 2 test beam: 2 GeV e+, 5 kHz scintillator trigger, Vbias -90 V
- Chips 6, 8 (sensor), calibrated, trimmed, optimal DAC parameters
- 50 sec runs, 0 140 k clusters per run
- Change VthrComp from lowest to optimal DAC units. Large DAC = soft threshold



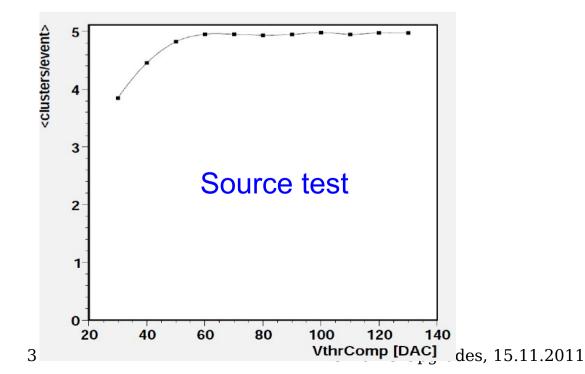
adjustable by programmable DAC, per ROC

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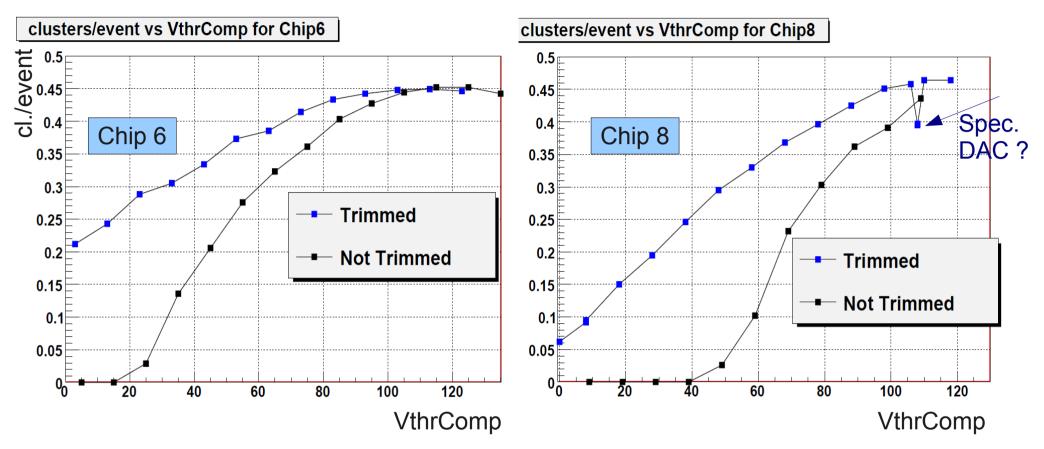
Threshold Scan Results (01.11.2011)



- Uniforming of pixel thresholds (trimming) makes an efficiency plateau visible
- More close to source test results now ?

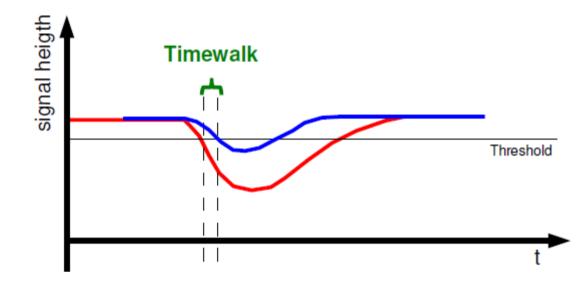


New Threshold Scan Results (03.11.2011)



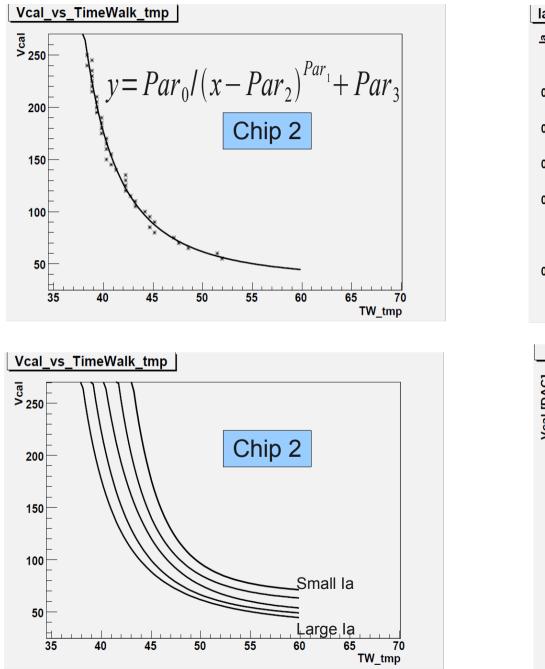
- Uniforming of thresholds brings more clusters per event
- Different chips show closer behavoiur after the trimming procedure
- Special DAC value found ?

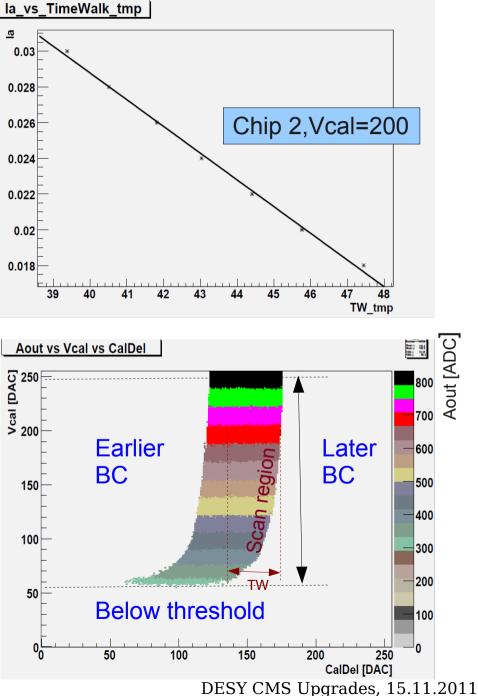
Time Walk Issue



- When a signal is compared to a threshold the time when it crosses this threshold depends on its amplitude Time Walk (TW)
- TW should be minimized to associate all hits to the same bunch crossing
- Fast optimization procedure by L.Wehrli (ETH'2007): PH is measured vs CalDel for Vcal=50 → 250. The signal appears at a lower value of CalDel for the lower Vcal value than for the higher one. This difference in CalDel DAC units can be converted into a time difference – TW

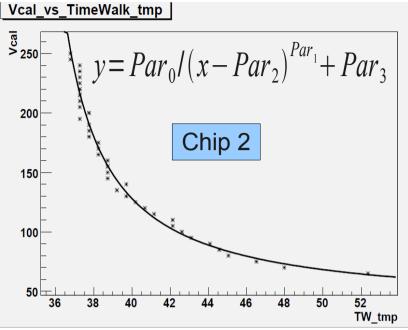
Control plots for TW (low Ia)

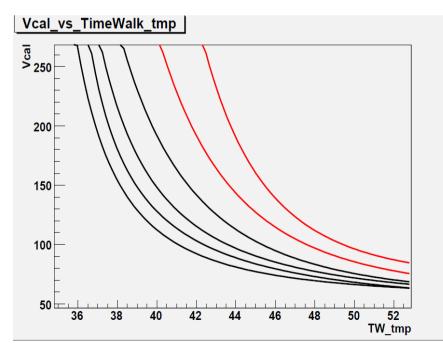


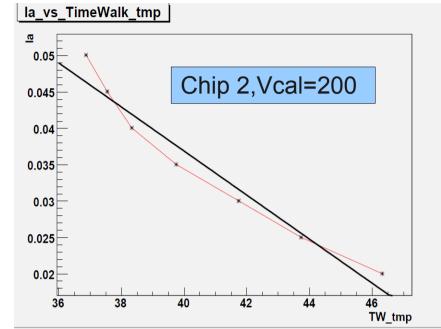


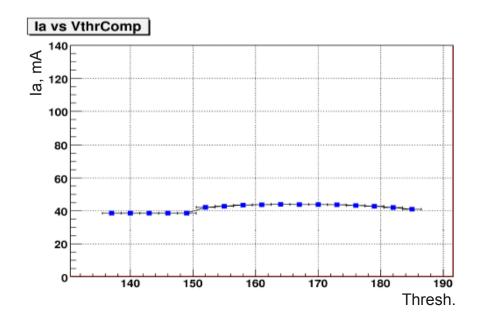
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Control plots for TW







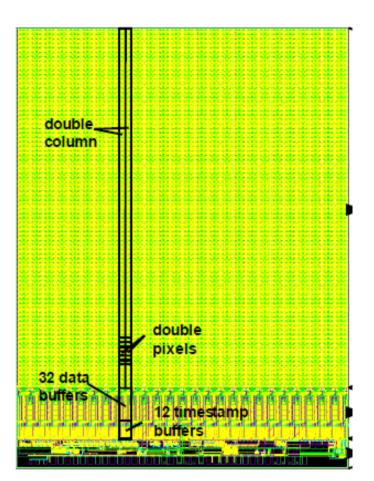


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Time walk conclusions

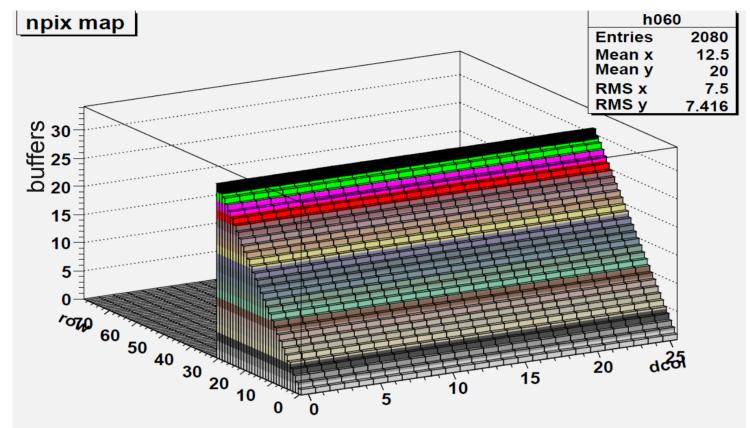
- TW is calculated after optimization of Ia, Vana, VthrComp, Vcal and Vtrim
- Fast procedure: it takes ~ 1.5 min.
- Chips with sensor need higher goal currents for scan
- TW = 20 25 ns (4 chips tested) for low Ia, reduces to 15 ns if high Ia included
- Non-linear Power distribution for Ia > 30 mA
- Similar behaviour for sensor chips

Data buffering



- CMS chip is organized in 26 dcolumns and 80 rows
- Each dcol. has in its perifery 12 time stamp buffers and 32 data buffers
- The corresponding time stamp (bunch crossing number) is written into the time stamp buffer → data are written into the next free data buffers (one data buffer per pixel)
- Hit recording runs autonomously in each dcol

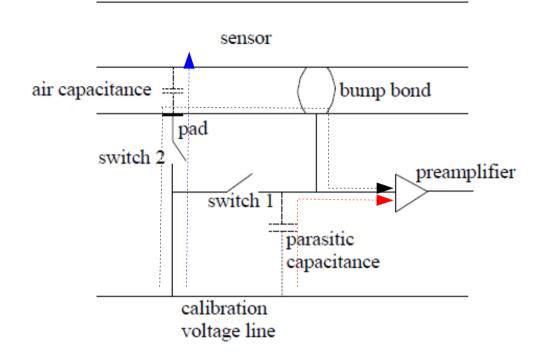
Arm Rows



- Enable rows for each double column and count pixels
- Expect one pixel per activated row until the data buffer is filled
- Up to 31 data bufferes for each double column are filled OK
- SLOW procedure: 3.5 min.

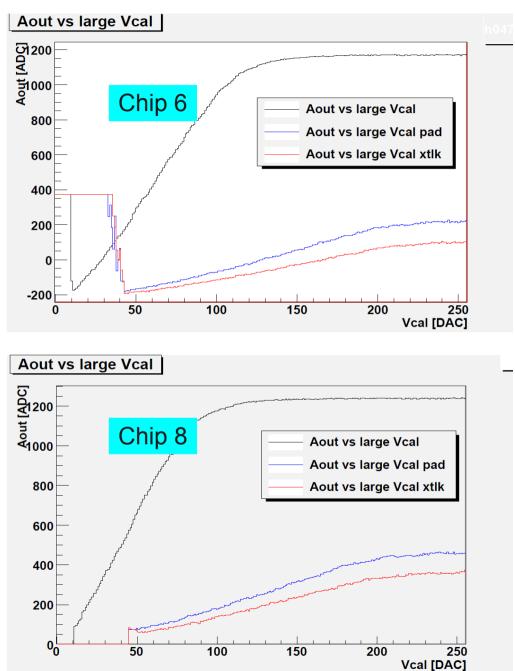
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Arm Pad, Xtalk



- Three ways to activate pixel activity: <u>Standard</u> (used so far), via '<u>pad</u>' and through '<u>Xtalk</u>'
- Different signals can be used for bump bonding test of modules, cross calibration of ROCs and some other purposes ?

Arm Results



 Use three different capacitances to inject charge: direct, via sensor, and crosstalk:

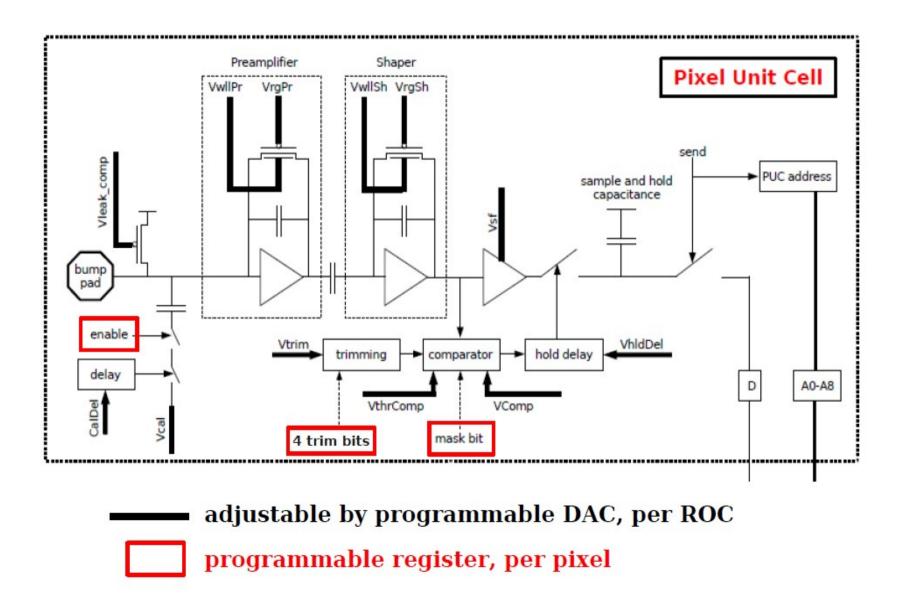
• $Q = C_x \cdot Vcal$

- One pixel activated.
- Draw PH [ADC] vs calibrate amplitude for large Vcal (450 e/DAC)
- Use sensor type ROCs
- Chips 6, 8 show similar behaviour but PHs are different (different config. parameters for analog gain and offset)
- Test takes a few seconds only (for one pixel).
- Capacitance via sensor depends on bump bond height (bigger bonds – smaller capacitance).

Summary

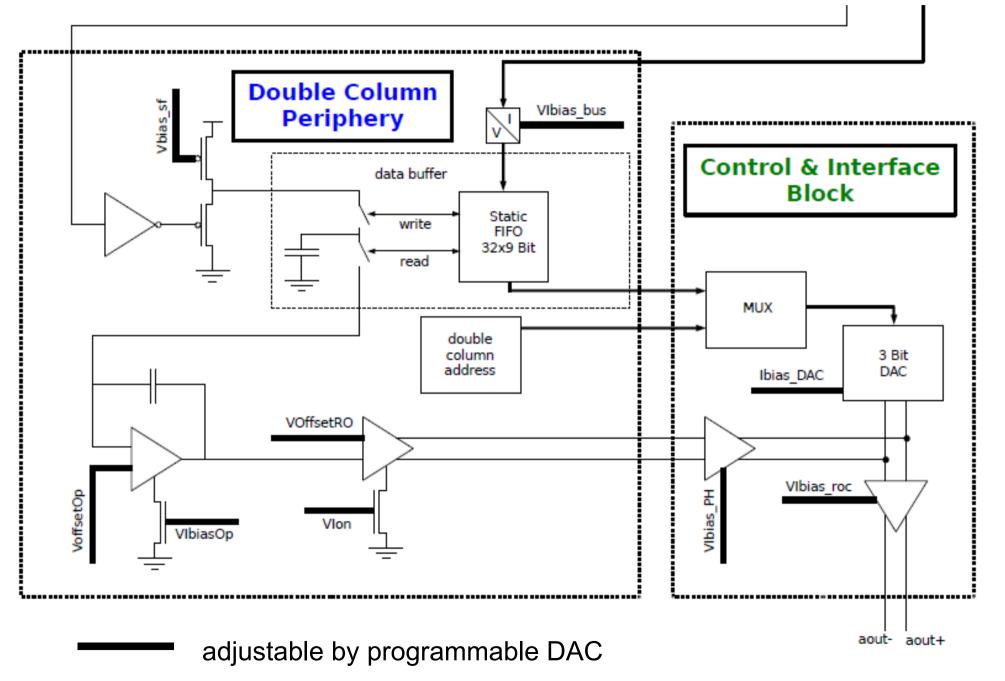
- New threshold scan confirms increasing of efficiency plateau after chip parameters optimization. Uniforming of different chips behaviour is visible after the trimming procedure
- Fast time walk study procedure shows values of ~ 20 ns
- Data buffer check procedure is developed
- New procedure of calibrate signal injection is introduced can be useful for farther tests

Psi46 Pixel Readout Chip



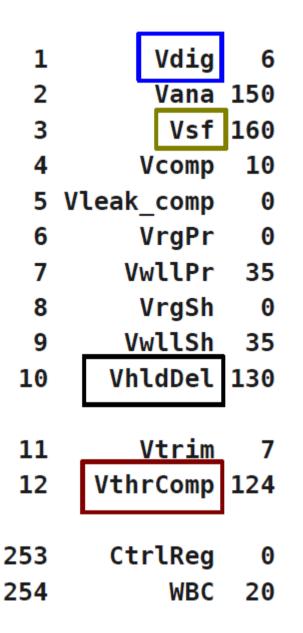
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psi46 pixel readout chip



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psi46 DACs



13	VIBias_Bus	30
14	Vbias_sf	10
15	Voffset0p	55
16	VIbias0p	115
17	V0ffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VICol0r	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	L25
27	RangeTemp	0

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Time Walk Calc. Procedure

- Read Config & Test parameters and init pixel from the lower half of the chip
- Apply Trim parameters from associated file
- Scan CalDel DAC from 0 to 255 with 10 trig for each point. Determine $\Delta T(CalDel) = ScanAdac(counts) / nTrig$
- Measure actual Ia, compare to goal Ia and determine <u>Vana</u> iterative procedure. Done for 7 goal Ia points in AdjustVana
- Scan different WBC and take smallest threshold <u>VthrComp</u>. Set <u>Vtrim</u> according to new threshold. Measure threshold with a new Vtrim
- TimeWalk(Vcal): draw (and fit) Vcal vs TimeWalk_tmp for given WBC range and calculated CalDel
 - Defines new values of <u>WBC</u>, <u>Vcal</u> and <u>CalDel</u>: 'CalDel' steps inside of 'Vcal' loop which is inside of 'WBC' loop - 3d procedure
 - Draw and fit Vcal vs TimeWalk_tmp (TW_tmp)

$$TW_{tmp} = (102 - WBC + 1) * 25 - \frac{25}{\Delta T (CalDel)} * CalDel + 0.5$$

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Time walk calc. procedure

• Fit function is
$$y = Par_0/(x - Par_2)^{Par_1} + Par_3$$

• Calculate value of <u>TimeWalk</u> for meanShift in time taken from testParameters file

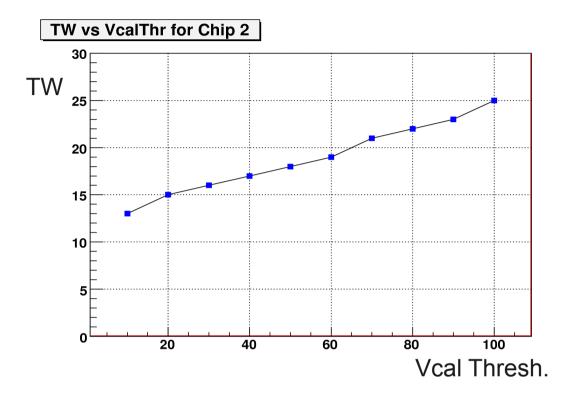
$$TW = meanShift - (Par_0/(200 - Par_3))^{1/Par_1} + Par_2$$

- Draw (meanShift TW) for 7 points of goal current Ia. Fit it by line and save Par_0
 → this is a PowerSlope of ~ 2 mA per DAC for Vcal=200
- Calculate a new Vana and optimize value of TimeWalk
 - Calculate <u>Vcal</u>, <u>Vtrim</u> and <u>VthrComp</u> ones again
 - Recalculate <u>TimeWalk</u> with new parameters, draw it
 - Measure new la, calculate a new goal current

new goal Ia=
$$I_{actual}$$
- I_0 + TW * *powerSlope*

- Find <u>Vana</u> for new goal la
- Recalculate and set new <u>threshold</u>, <u>Vcal</u> and <u>Vtrim</u>
- Calculate final **<u>TW</u>** and plot it

TW for different Thresholds



- Time Walk is measured for different values of Threshold
- Linear dependence. A similar behaviour is observed by PSI [Nuclear Instruments and Methods in Physics Research A 565 (2006) 188–194]