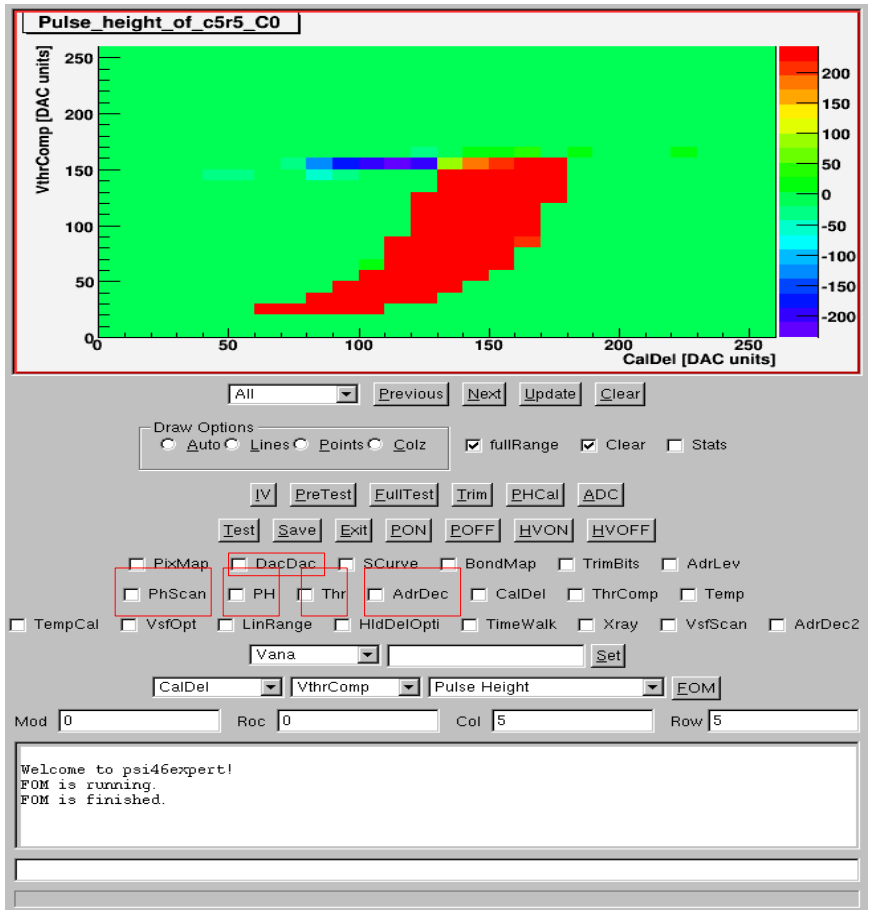
More ROC Tests

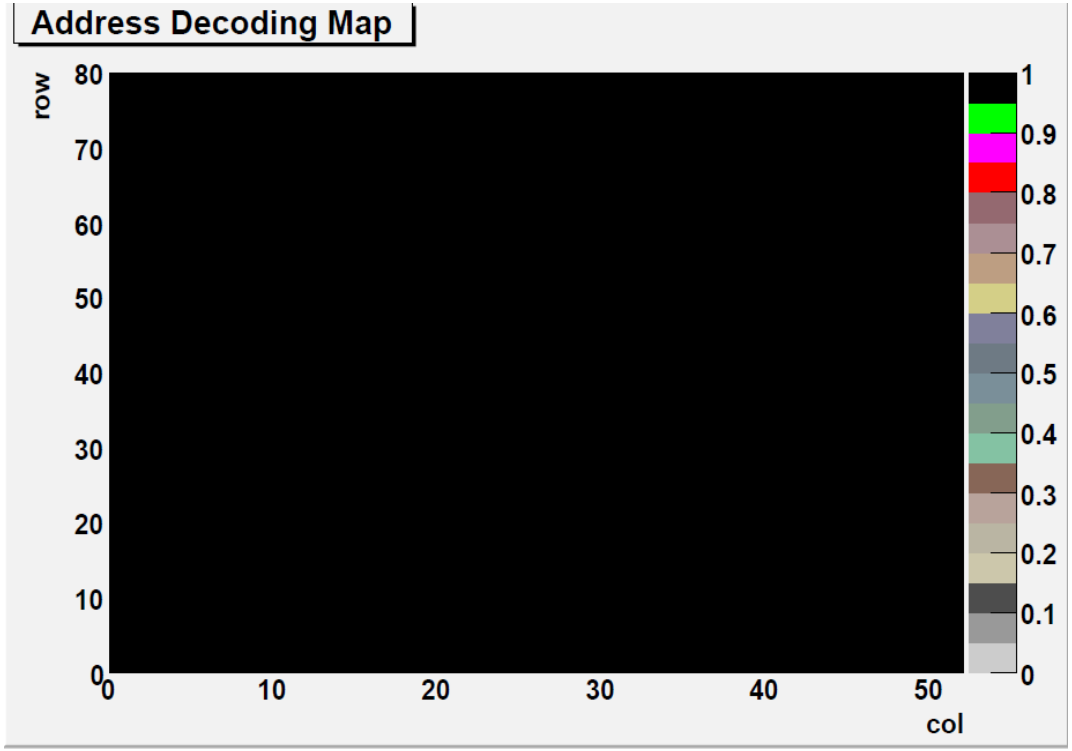
Alexey Petrukhin, DESY
Daniel Pitzl, DESY

CMS Tracker Upgrade 29.11.2011



- ROC functionality
- DAC correlations
- Trimming and Time walk
- PH for different DACs
- Control plots for charge injection

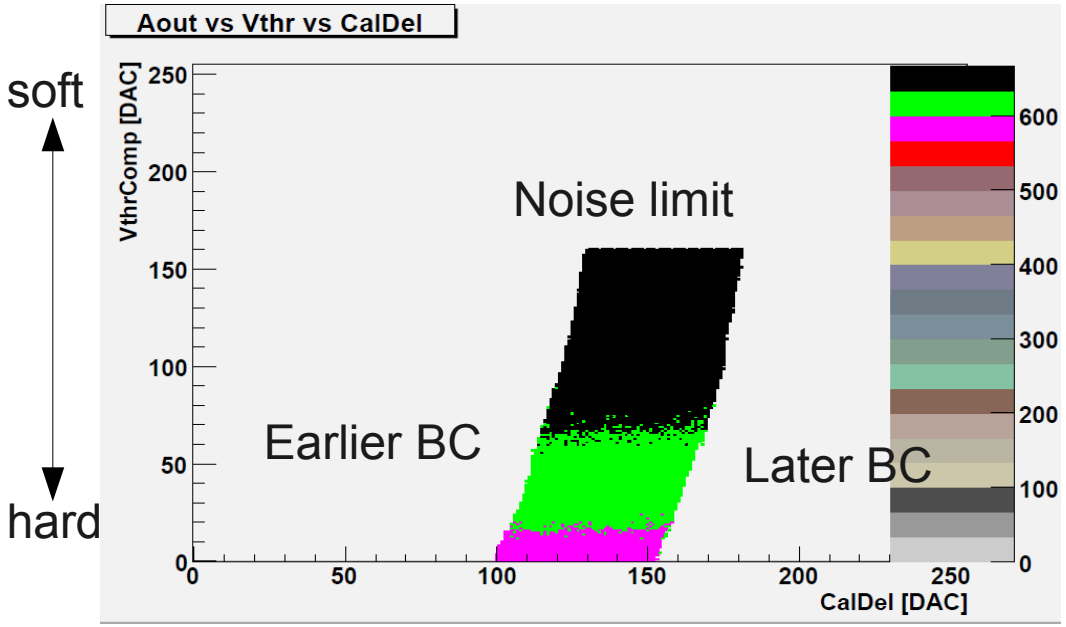
ROC functionality [AdrDec]

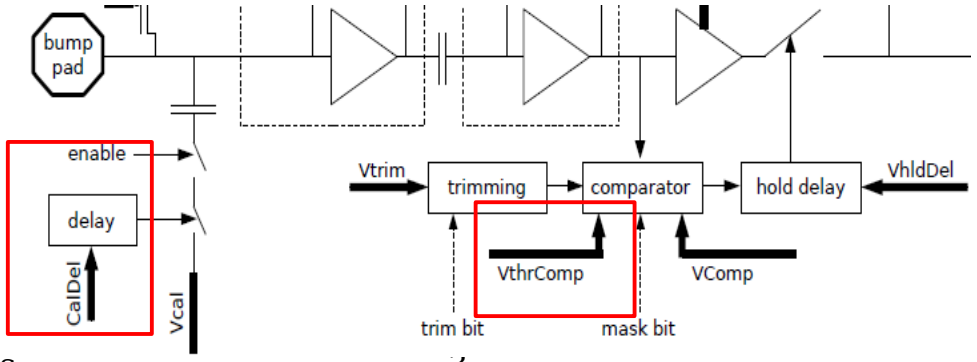


- Pulse each pixel and count number of data words. Fill a pixel word map if nwords = 25 (chip Header + pixel Address + analog Pulse Height). Normalize it to 1
- Not fast procedure – 8 min. in total

DAC correlations

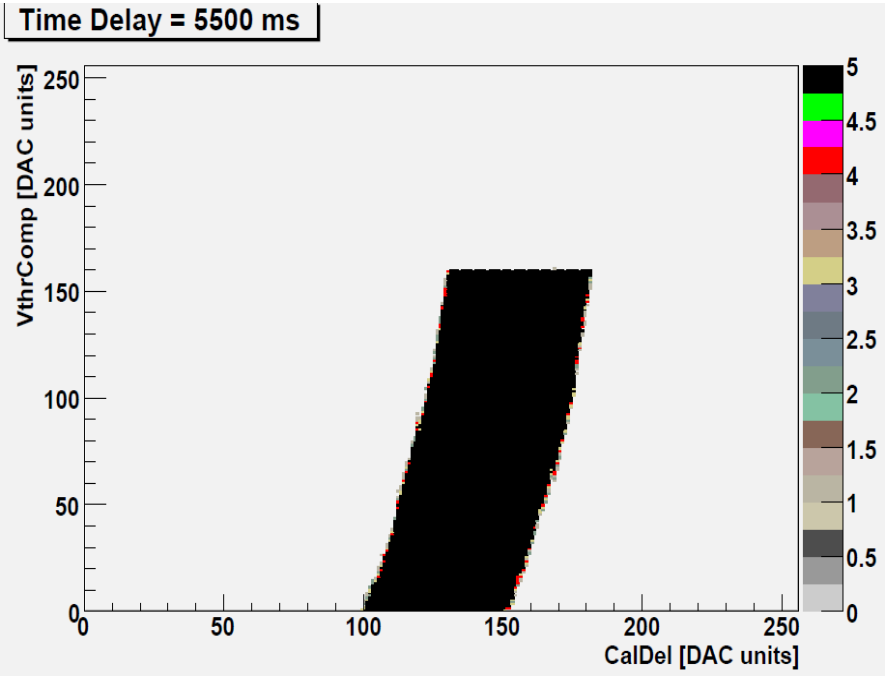
- Standard way at DESY:
  - activate one pixel
  - send 9 triggers
  - scan CalDel DAC for each value of VthrComp
  - measure PH for each bin in VthrComp and CalDel space
  - scanning time = 2 min. / chip → Not too fast





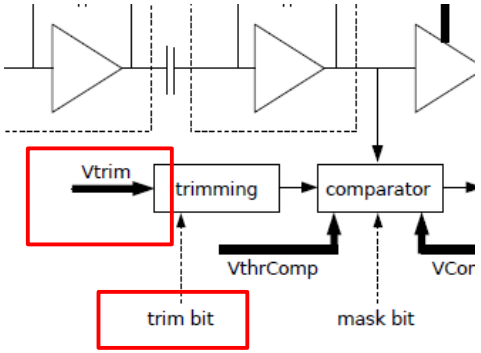
DAC correlations and delay [DacDac]

- Standard way at PSI:
  - activate one pixel
  - send 5 triggers
  - read FPGA data: count number of readouts for each bin. Data are transferred in blocks = 19999 words each → needs a time delay between FPGA and USB before transferring to PC. Bigger data block size → corrupt data starting
  - this time delay affects the DAC correlations (i.e BC)
- Solution: use DESY way (delay independent sample) as reference to calibrate USB timing
  - New delay = 5.5 sec. Total PSI procedure time = 0.5 min. → still 4 times faster than DESY procedure

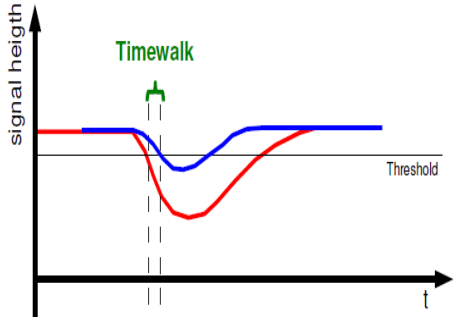


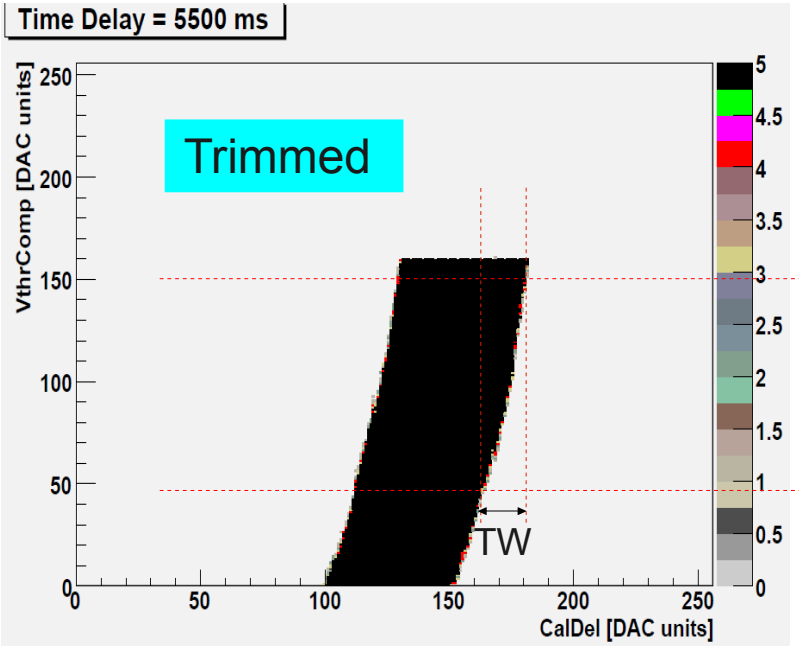
Trimming and Time walk

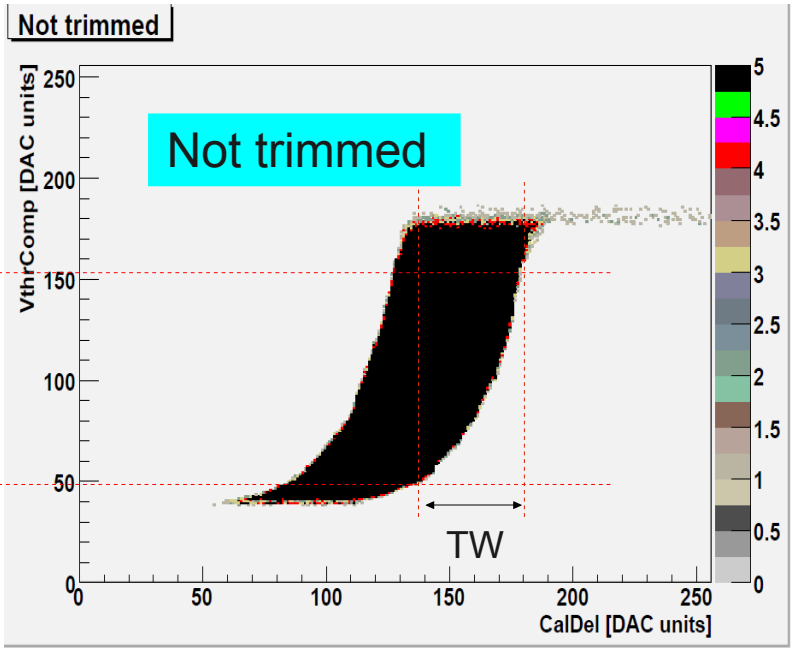
- Trimming procedure: unify individual pixel thresholds by 4 trim bits and scale with Vtrim DAC. Threshold variation reduced from ~300 → 80 e (chip 8). Good for chip efficiency (more clusters per event), unify different chip behavior.



- When a signal is compared to a threshold the time when it crosses this threshold depends on its amplitude – Time Walk (TW)
- TW should be minimized to associate all hits to the same bunch crossing

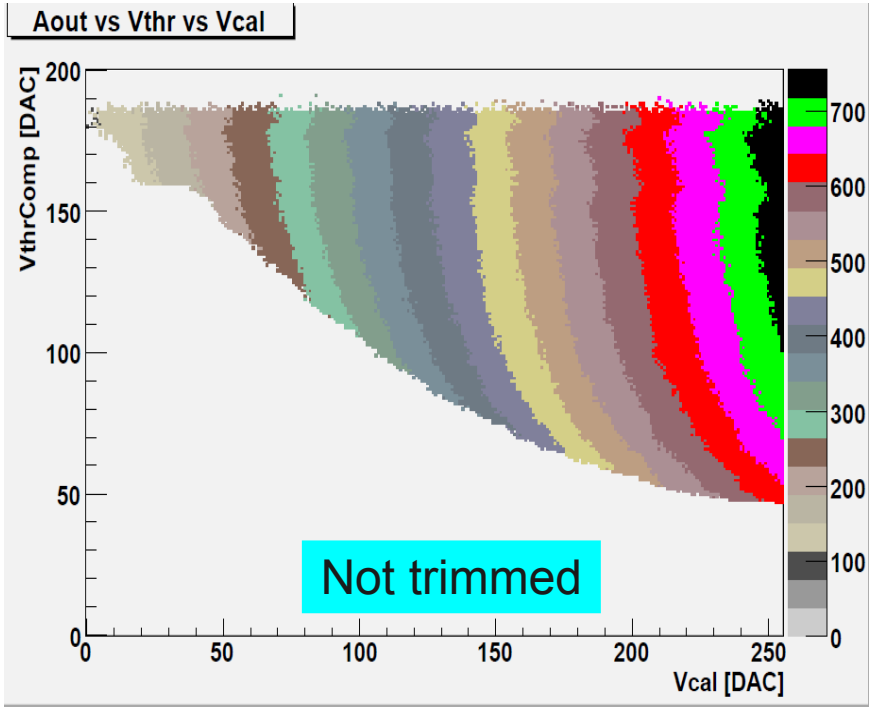


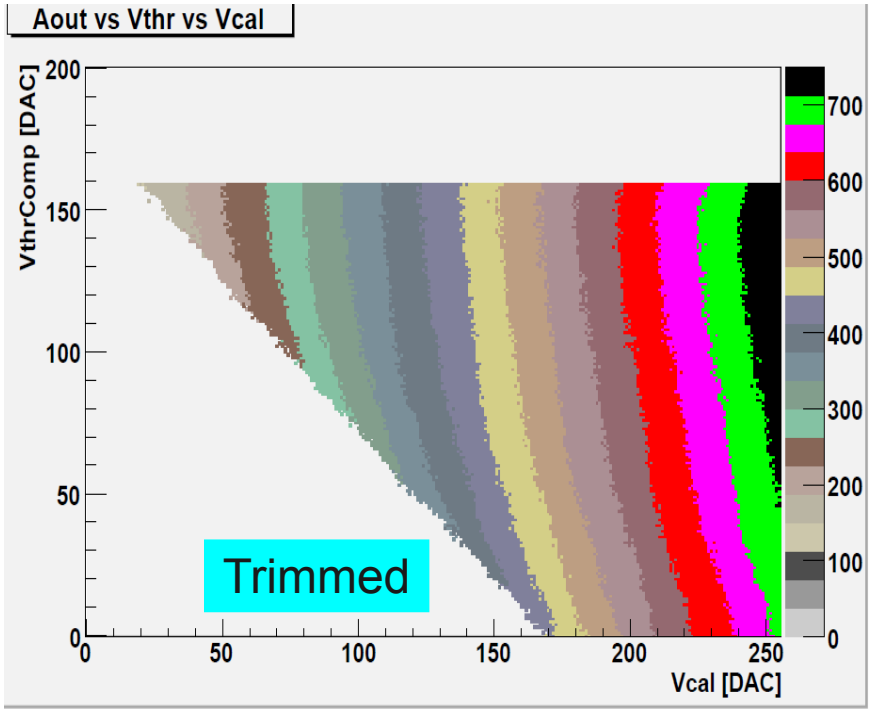




2.5 smaller TW after the trimming procedure !

Trimming and Time walk



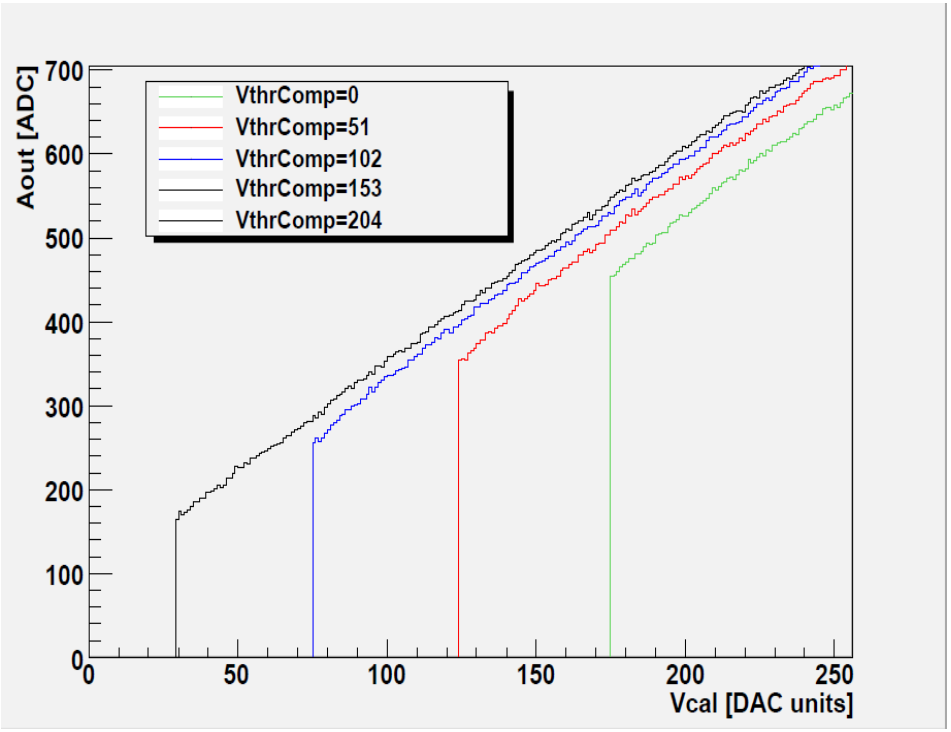


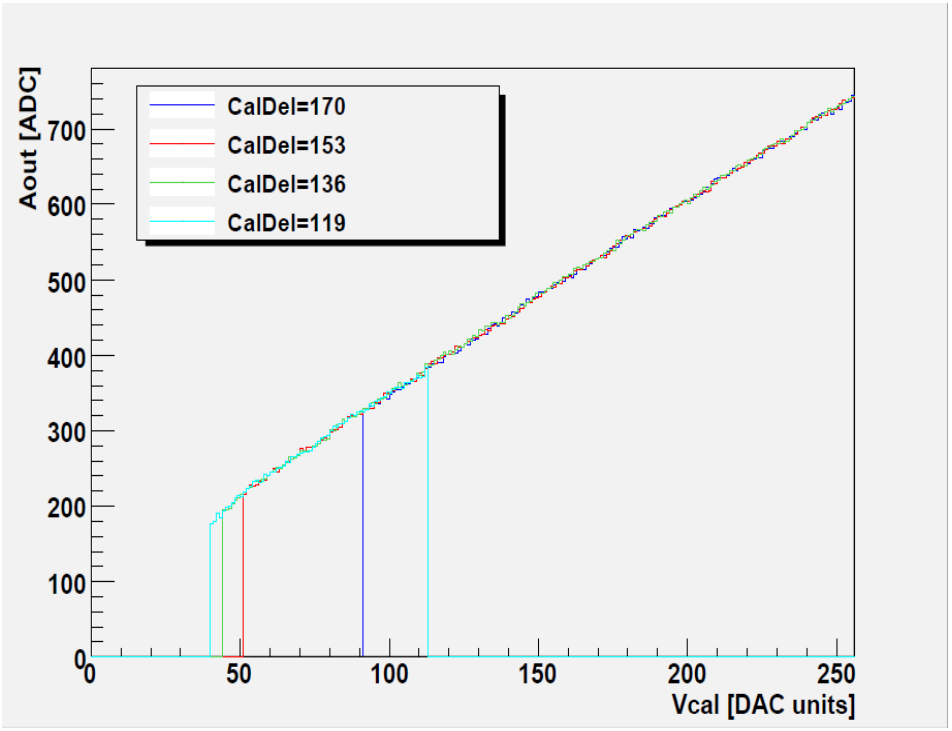
In VthrComp & Vcal space: Smaller TW after Trimming

PH vs Vcal vs different DACs [PhScan]

- New procedure to test Vcal DAC:
  - Activite one pixel
  - For 27 ROC DACs and 3 TBM DACs:
    - Change values of DACs with a given step
    - Scan Vcal from 0 to 256 for each given value of other DACs

Time consuming procedure: takes 4 min. per ROC. Can be used for cross check and final tuning of DAC parameters

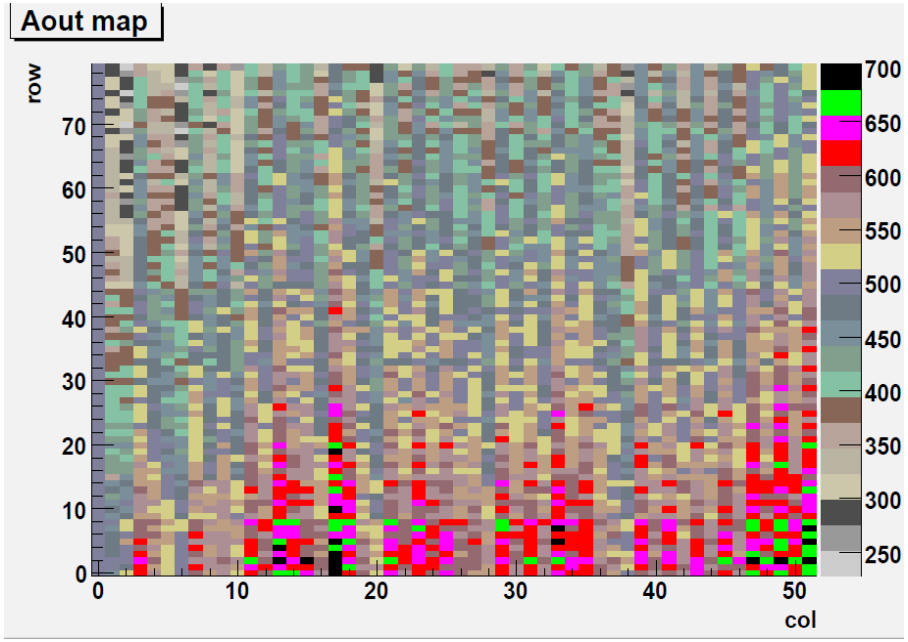


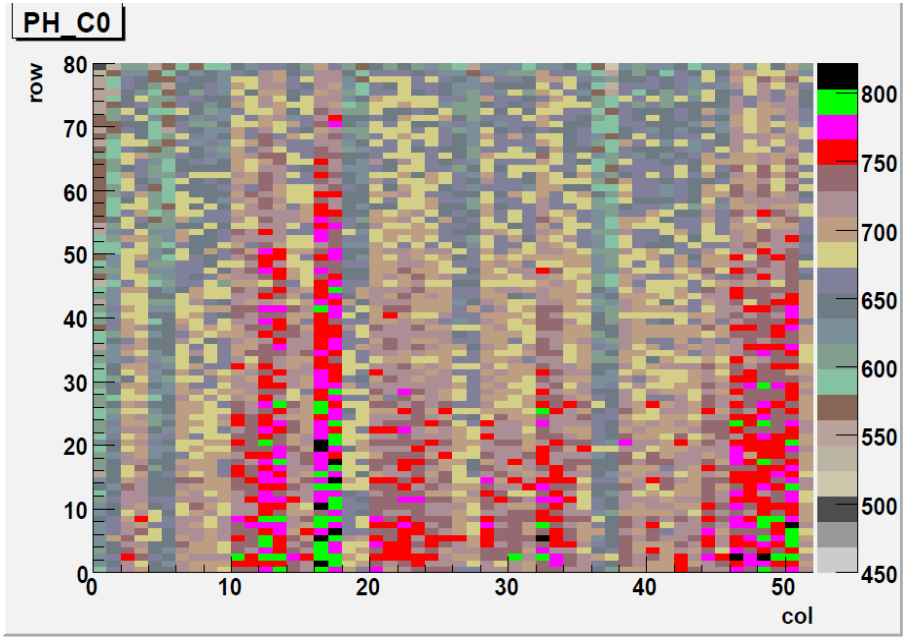


PH maps [PH]

- Standard way at DESY via USB:
  - Activate pixels in all dcolumns for the row
  - Measure PH for each pixel in dcolumns
  - Disable pixels and come to the next row
  - 6 sec. procedure

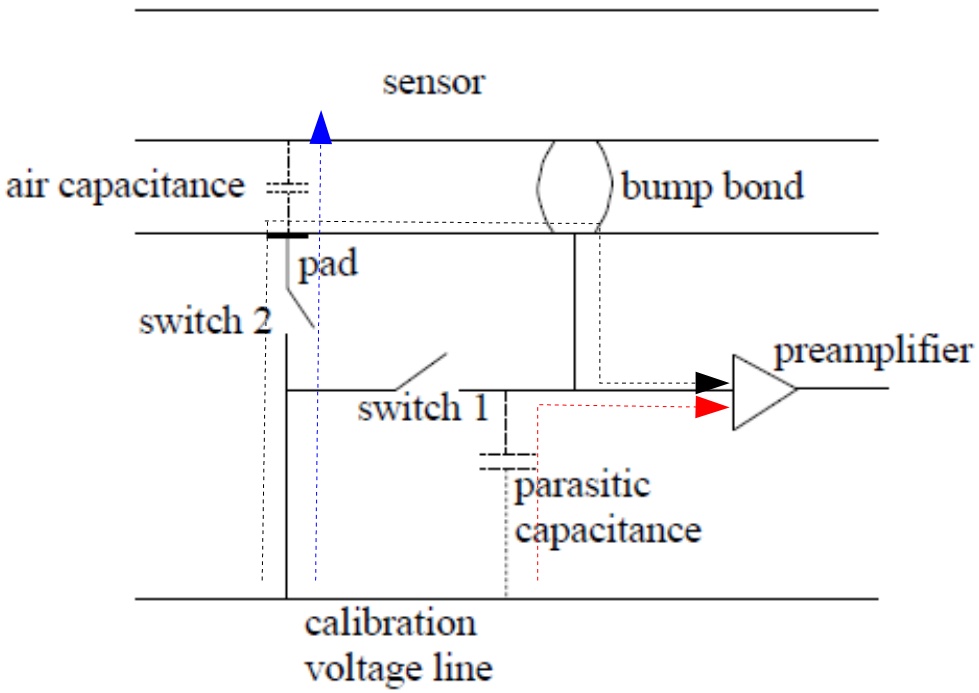
- Standard way at PSI via FPGA:
  - Pulse pixels 1 by 1 from FPGA
  - Measure PH for each pixel (fast reading of FPGA data)
  - 2 sec. procedure





Similar results, faster procedure via GUI (PSI)

Arm Pad, Xtalk (reminder)

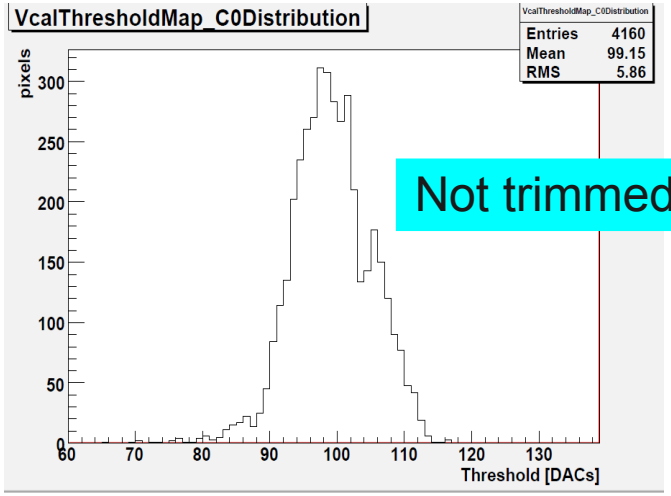


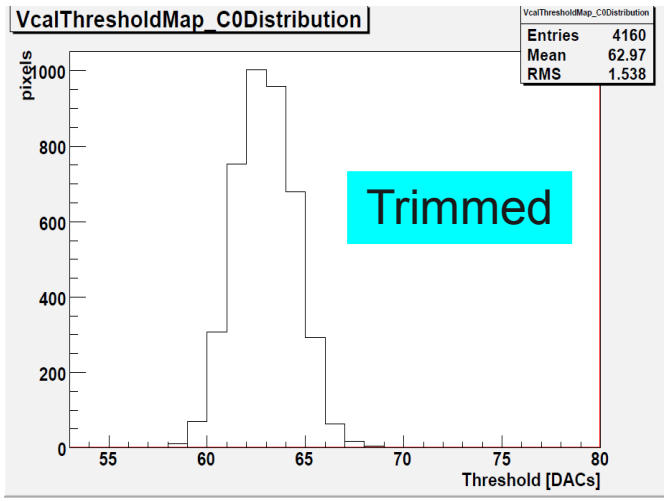
- Three ways to inject charge: Standard (used so far), via 'pad' and through 'Xtalk'
- Different signals can be used for bump bonding test of modules, cross calibration of ROCs and some other purposes ?

Control plots [Thr]

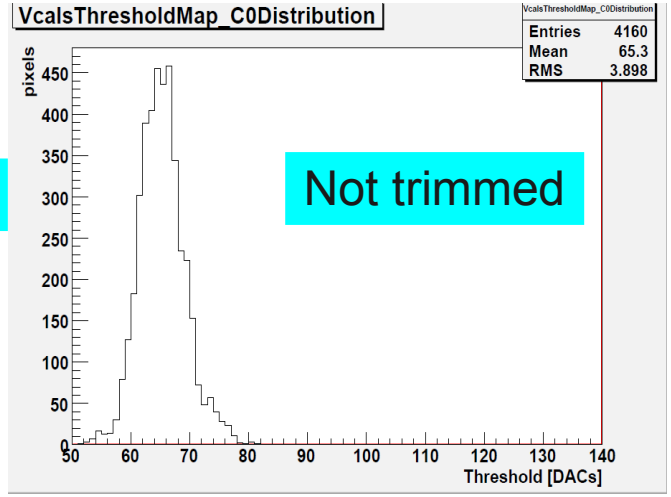
- Inject charge by 3 different ways and measure Vcal thresholds before and after trimming. One Vcal DAC = 65e (“Standard”)

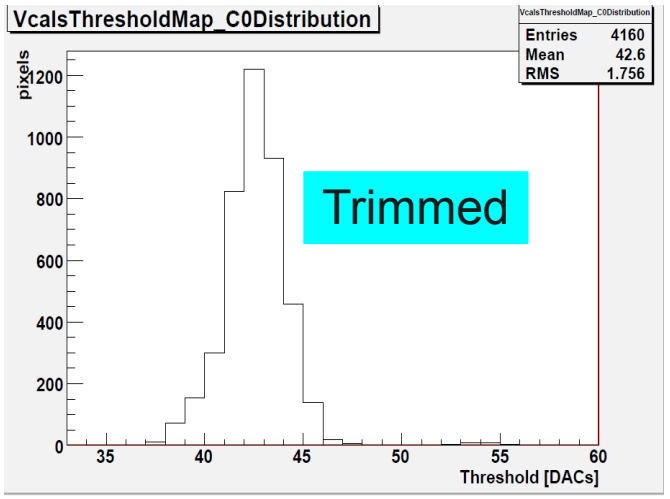
Standard



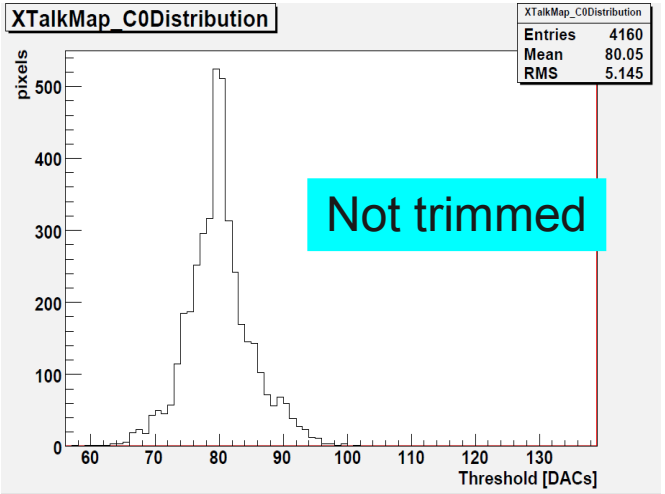


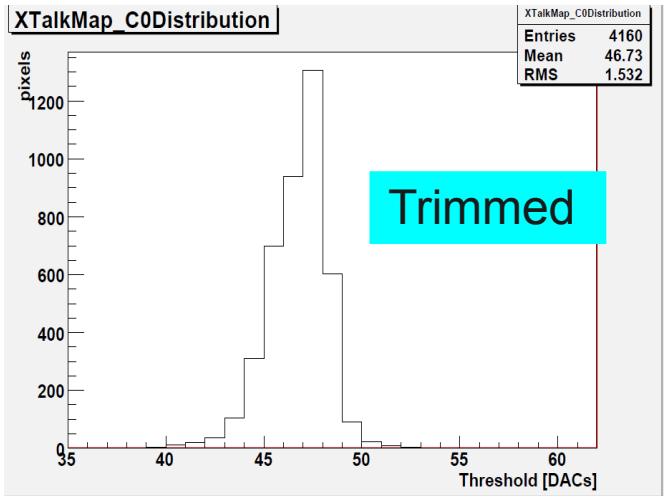
Pad





Xtalk



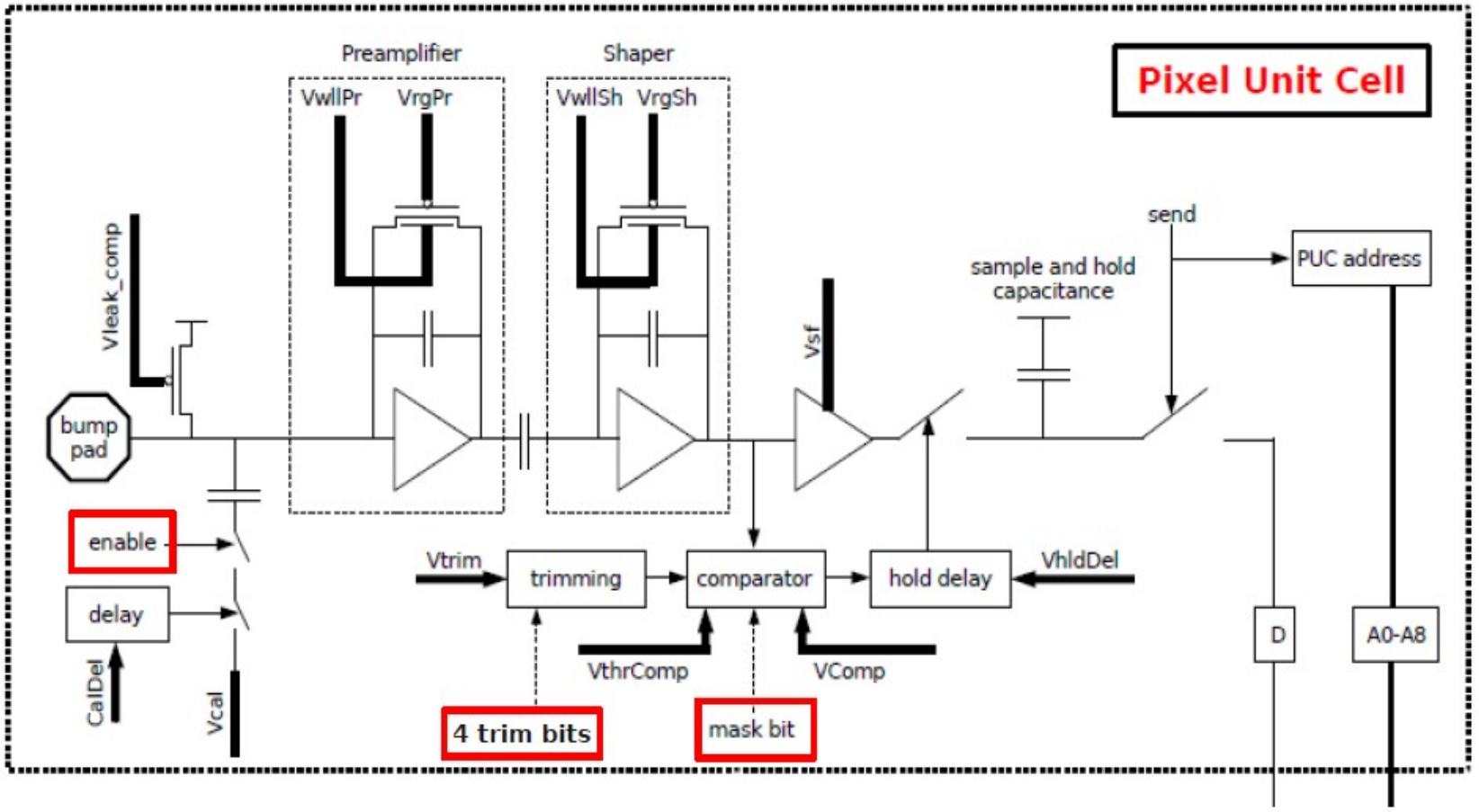


- All ways follow the trimming procedure
- “Standard” Mean=6400e before trim and 4000 after; RMS=380 before trim and 97 after (chip 6)

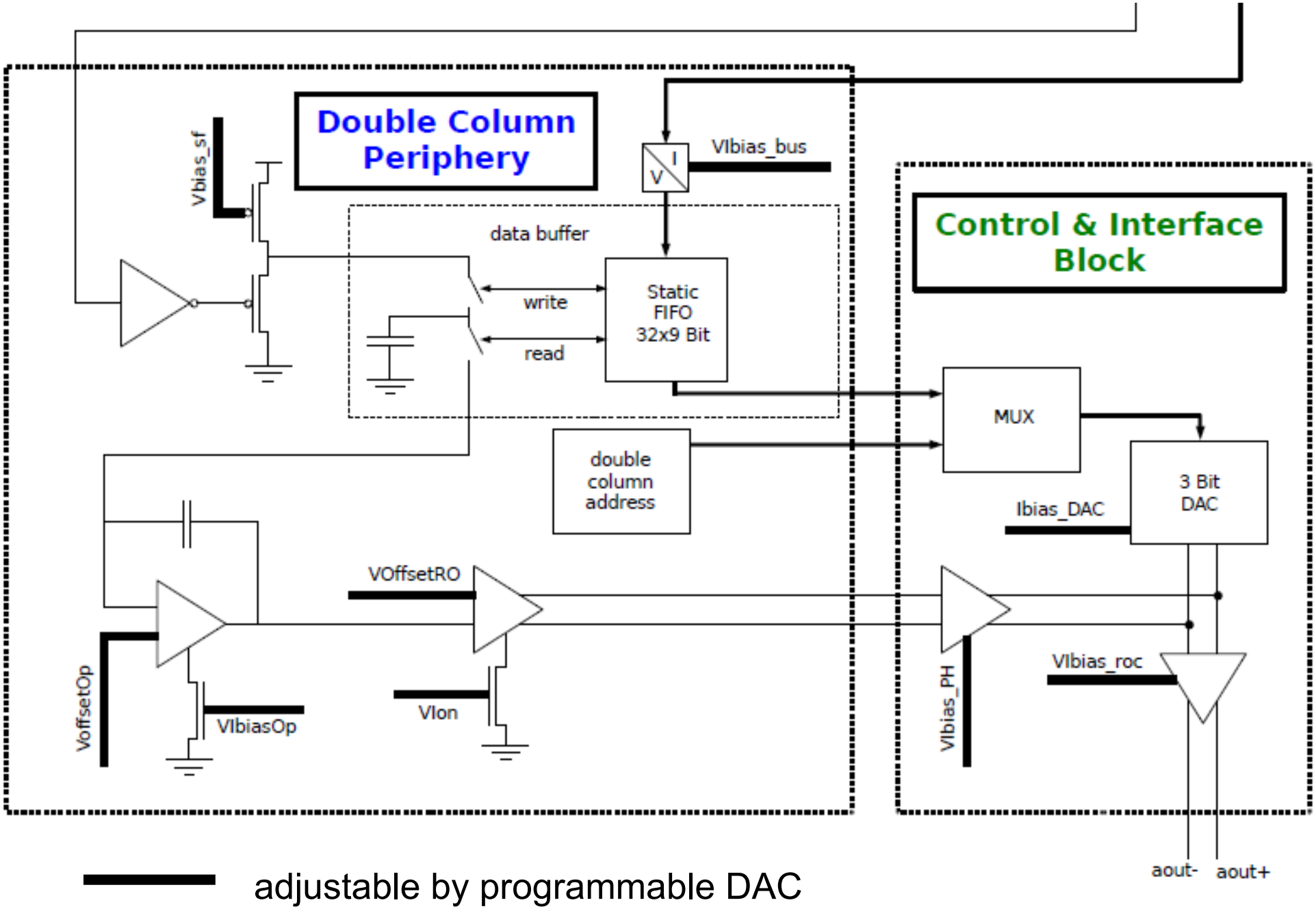
Summary

- New way of ROC functionality test is presented
- Fast GUI procedure for DAC parameters optimization is adapted at DESY
- Time Walk is reduced after Trimming procedure by factor of 2.5
- New PH test can be used for optimization of DACs
- Different PH mapping procedures show the similar results
- Control plots for different ways of charge injection confirm utility of Trimming procedure

Psi46 Pixel Readout Chip



psi46 pixel readout chip



adjustable by programmable DAC

psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

DAC correlations and delay

- Standard way at PSI:
  - activate one pixel
  - send 5 triggers
  - read FPGA data: count number of readouts for each bin. Data are transferred in blocks = 19999 words each → needs a time delay between FPGA and USB before transferring to PC. Bigger data block size → corrupt data starting
  - This time delay affects the DAC correlation (i.e BC)
- Solution: use DESY way (delay independent sample) as reference to calibrate USB timing
  - New delay = 5.5 sec. Total PSI procedure time = 0.5 min. → still 4 times faster than DESY procedure