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Dedicated front-end electronics and data preprocessing for a granular electromagnetic calorimeter

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on behalf of FCAL-LUXE collaboration

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Outline

- Background and motivation
- FLAME readout ASIC
- Readout architecture and components
- Data processing

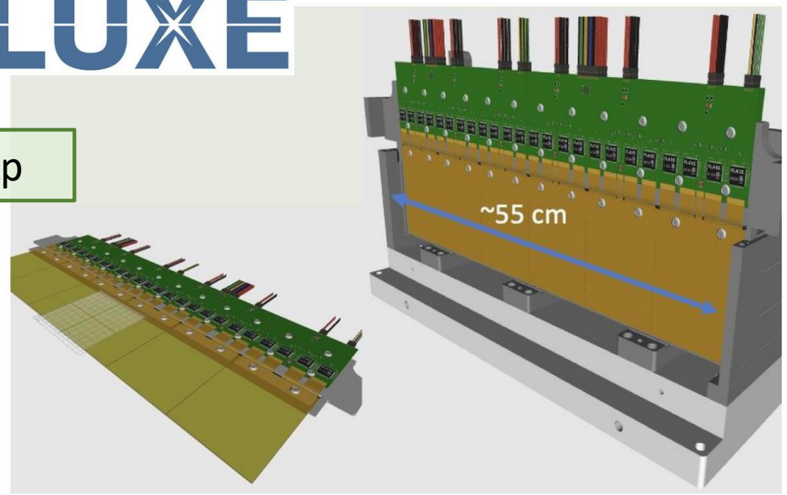
Background

- ECALp inherits from **LumiCal** – compact electromagnetic calorimeter with small Moliere radius developed for luminosity measurement at ILC (and, later, CLIC) by FCAL
- Barrel-shaped sampling calorimeter with 20 layers (30 for CLIC) of 3.5mm thick tungsten absorbers interspersed with silicon sensors placed in 1mm gap

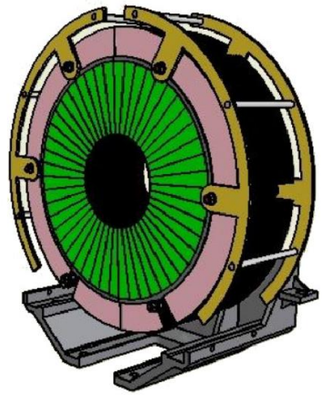
- With not-so-bright future of ILC (and before LUXE), FCAL switched to general R&D on compact electromagnetic calorimeter with the need of new readout

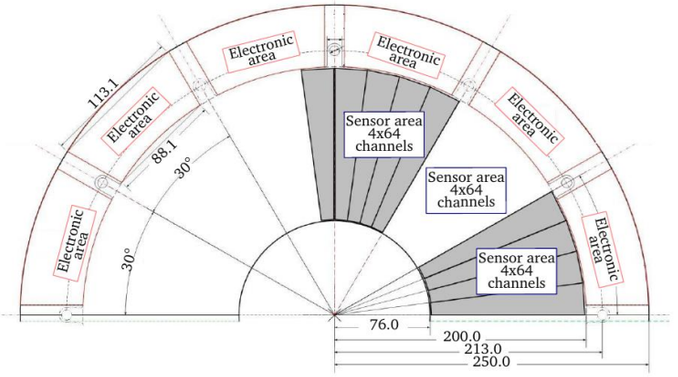
LUXE

ECALp



LumiCal





Motivation

Requirements for the readout dedicated to the R&D on compact calorimeter:

- DESY test beam line (up to 5 GeV electrons) or cosmic muons as sources
  - Triggered or triggerless operation
- Fast, with event rate in range of several thousand events per second
- As flexible (experiment-agnostic) as possible:
  - No data processing, triggering or buffering in ASIC
  - All triggering and processing done in FPGA, to allow for easy reconfiguration of the system

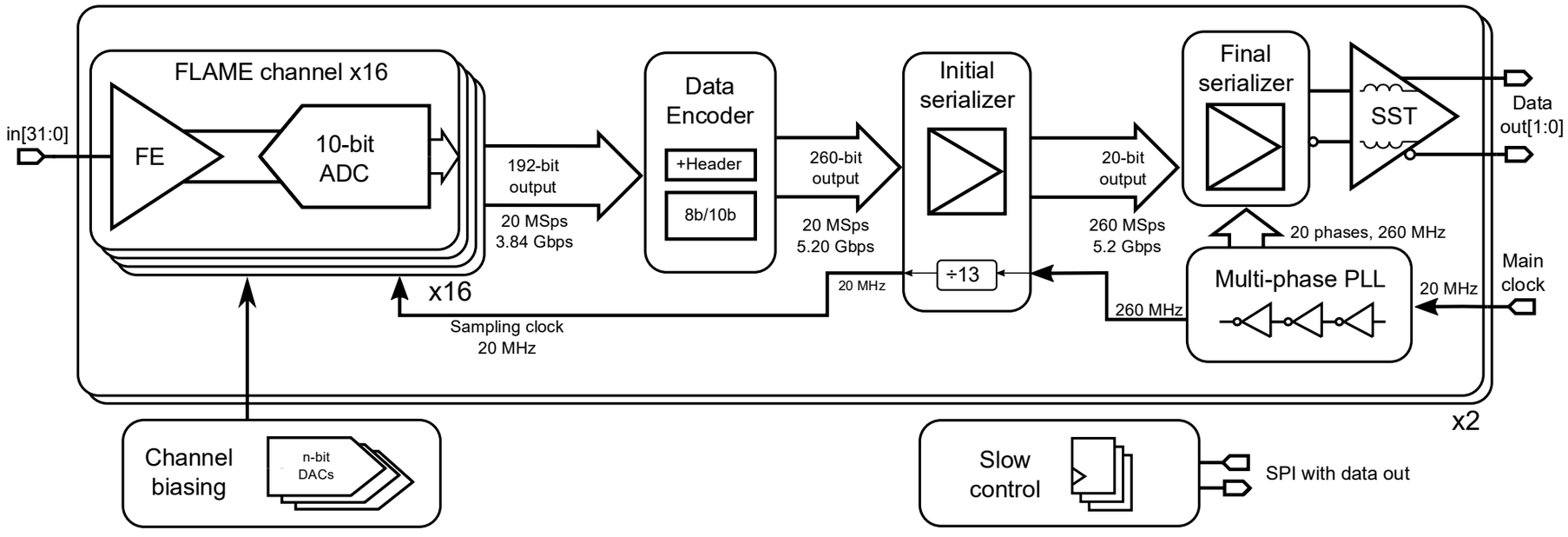
For this purposes a new readout ASIC, called **FLAME** (FcaL Asic for Multiplane rEadout) developed in 2018 by AGH.

Complete DAQ system, based on Zynq UltraScale+ FPGA developed in 2019.

FLAME ASIC

FLAME is a 32-channel readout ASIC for silicon sensors, working as a waveform digitizer.

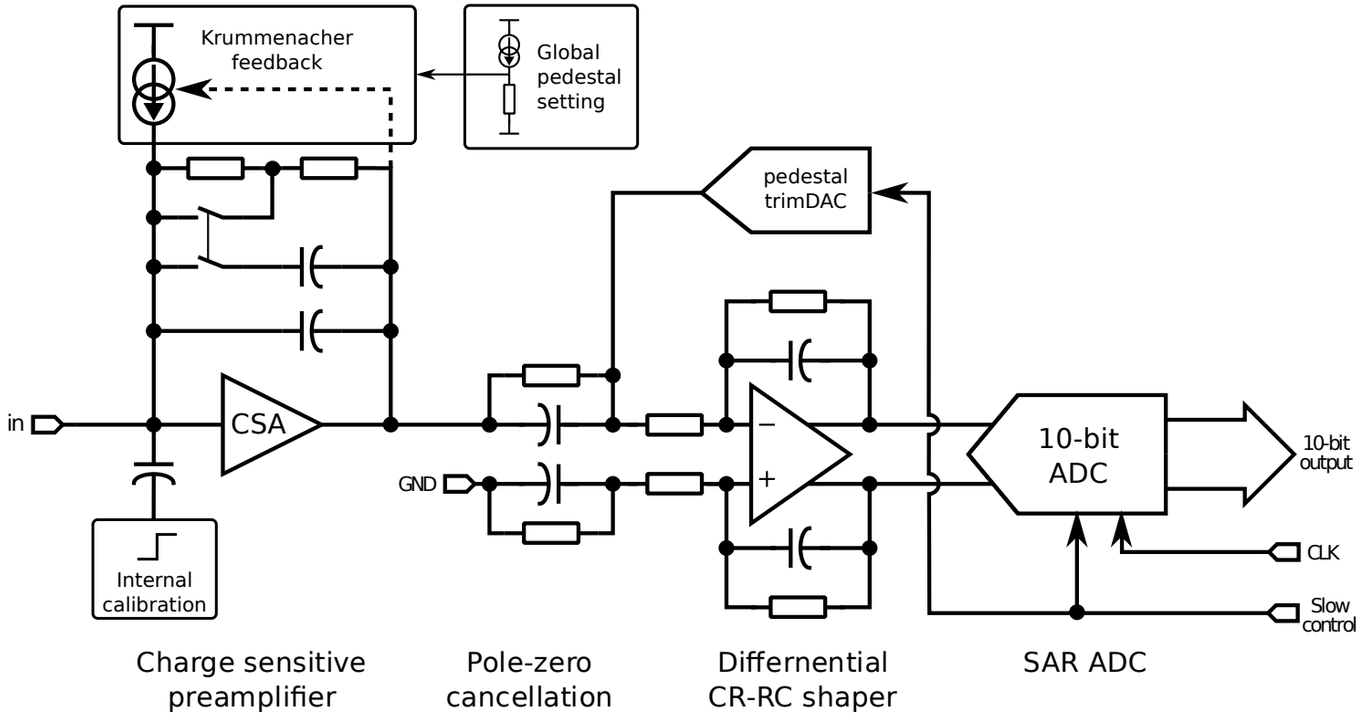
- Two 16 readout channel blocks (almost two ASICs on one die) sharing common biasing and slow control circuitries
- Each readout channel equipped with front-end and 10b SAR ADC
- Two 5.2 Gbps serializers, one per each 16 channels block, with:
  - 8/10b encoding
  - Multi-phase PLL for fast clock generation
  - SST driver



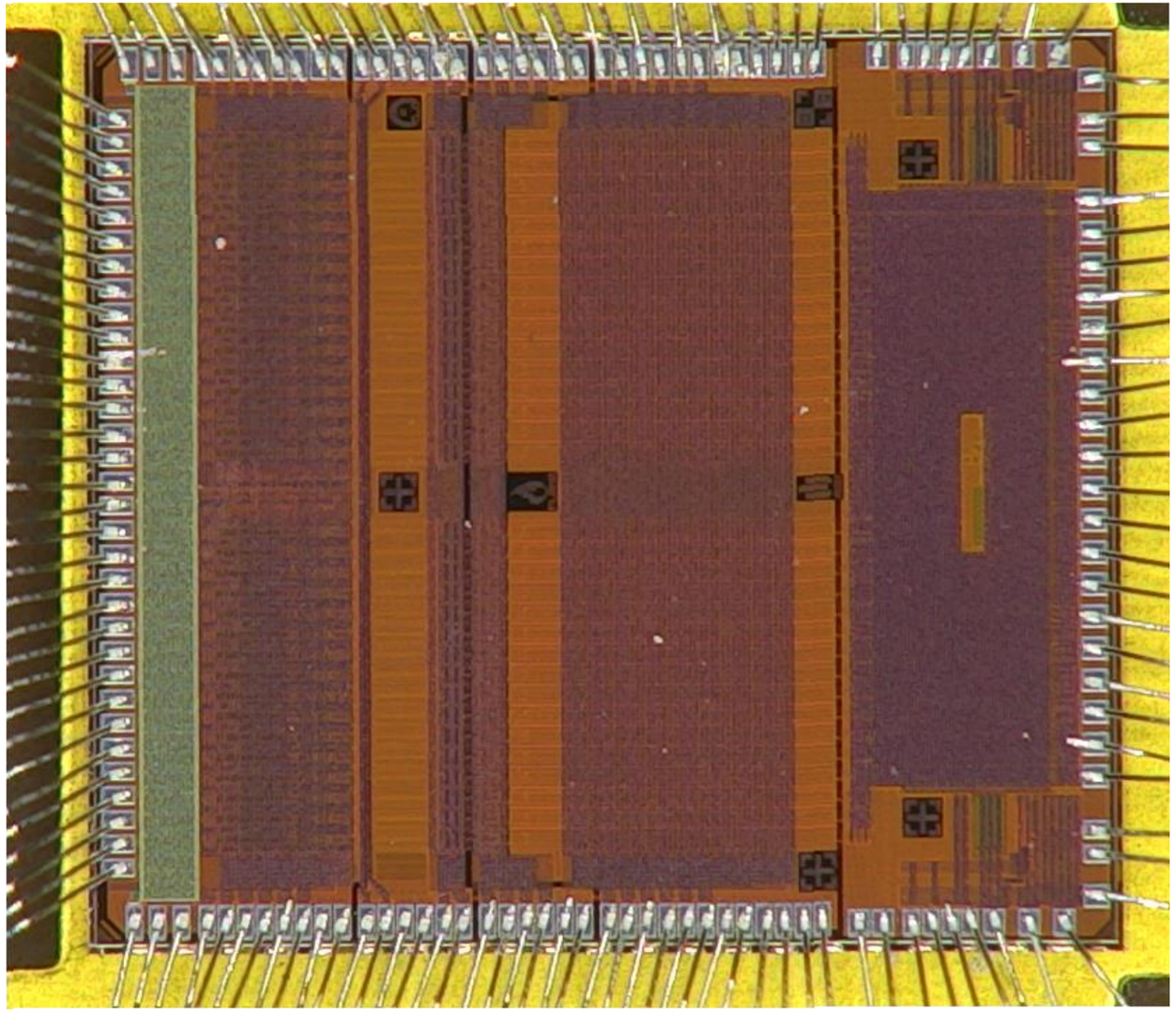
FLAME channel

- Charge sensitive preamplifier with two switchable gains:
  - High gain – up to 200 fC with MIP sensitivity, dedicated for 5 GeV electrons at DESY
  - Low gain – up to 6 pC for electromagnetic shower core
- Fully differential CR-RC shaper with 50 ns peaking time
- Krummenacher feedback
- Pedestal trim-DAC
- Internal calibration

- 10b SAR ADC
  - Sampling rate up to 50 MSps
  - DNL, INL < 0.5 LSB
  - ENOB > 9.5
  - Ultra low power consumption, below 1mW at 50 MSps
  - Nominal sampling rate – 20 MSps



FLAME ASIC



ASIC fabricated in 130nm CMOS in two runs, 2019 and 2021

Die size:
3.7 x 4.3 mm²

In total more than 100 ASICs tested and used for testbeams and laboratory measurements

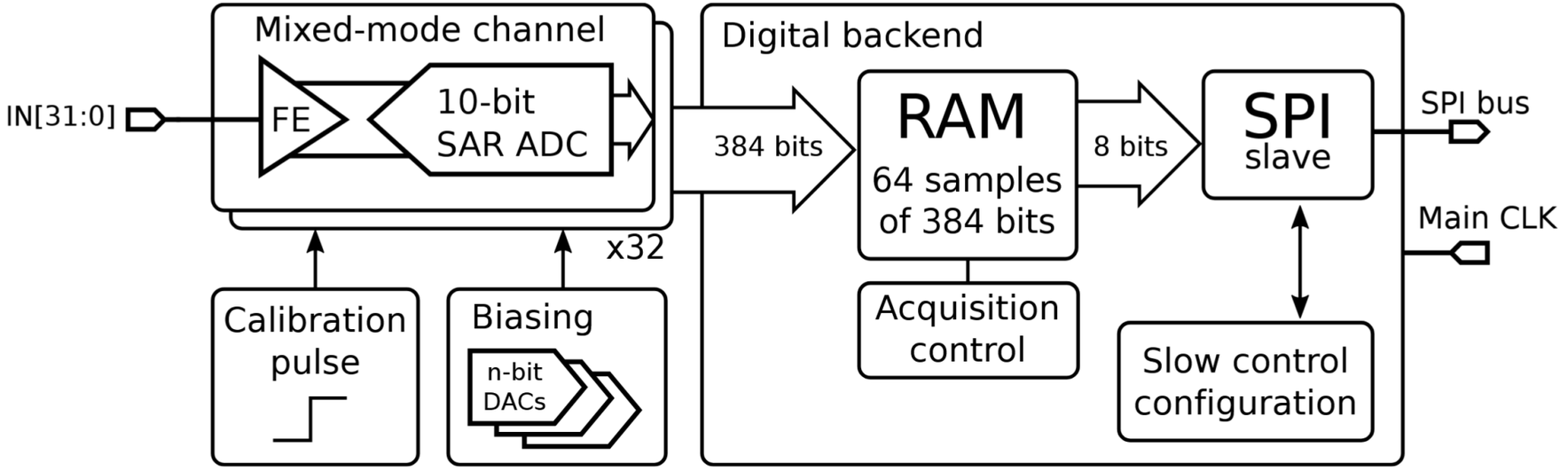
FLAXE ASIC – FLAME for LUXE

FLAXE – FLAME for LUXE experiment, with completely new digital backend matching the beam structure – only 10 bunch crossings per second

- Build-in DAQ memory for 64 ADC samples from all 32 channels
- Triggered by the BX clock of the experiment, with data readout through SPI bus

1000 ASICs fabricated in 2024 – production failed due to manufacturing problems

- Only few ASICs working, 99% suffering from excessively large power consumption



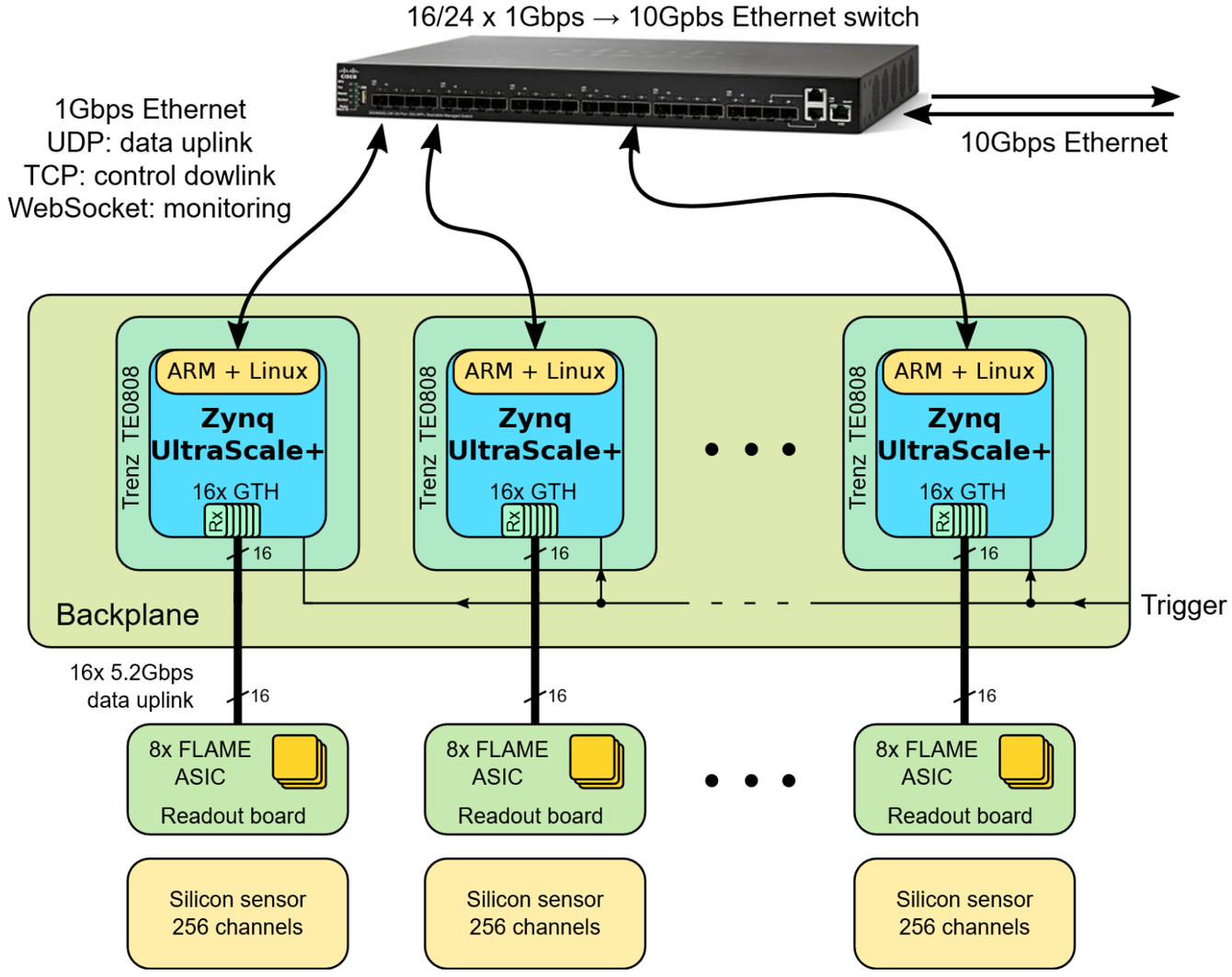
Readout architecture

One readout board (FEB) per each LumiCal (or ECALp) sensor:

- 256 pads (channels)
- 8 FLAME ASICs / FEB
- 16 serial data links / FEB
- **83.2 Gbps / FEB** of data stream

DAQ system based on Zynq UltraScale+ FPGAs, hosted on COTS Trenz TE0808 modules

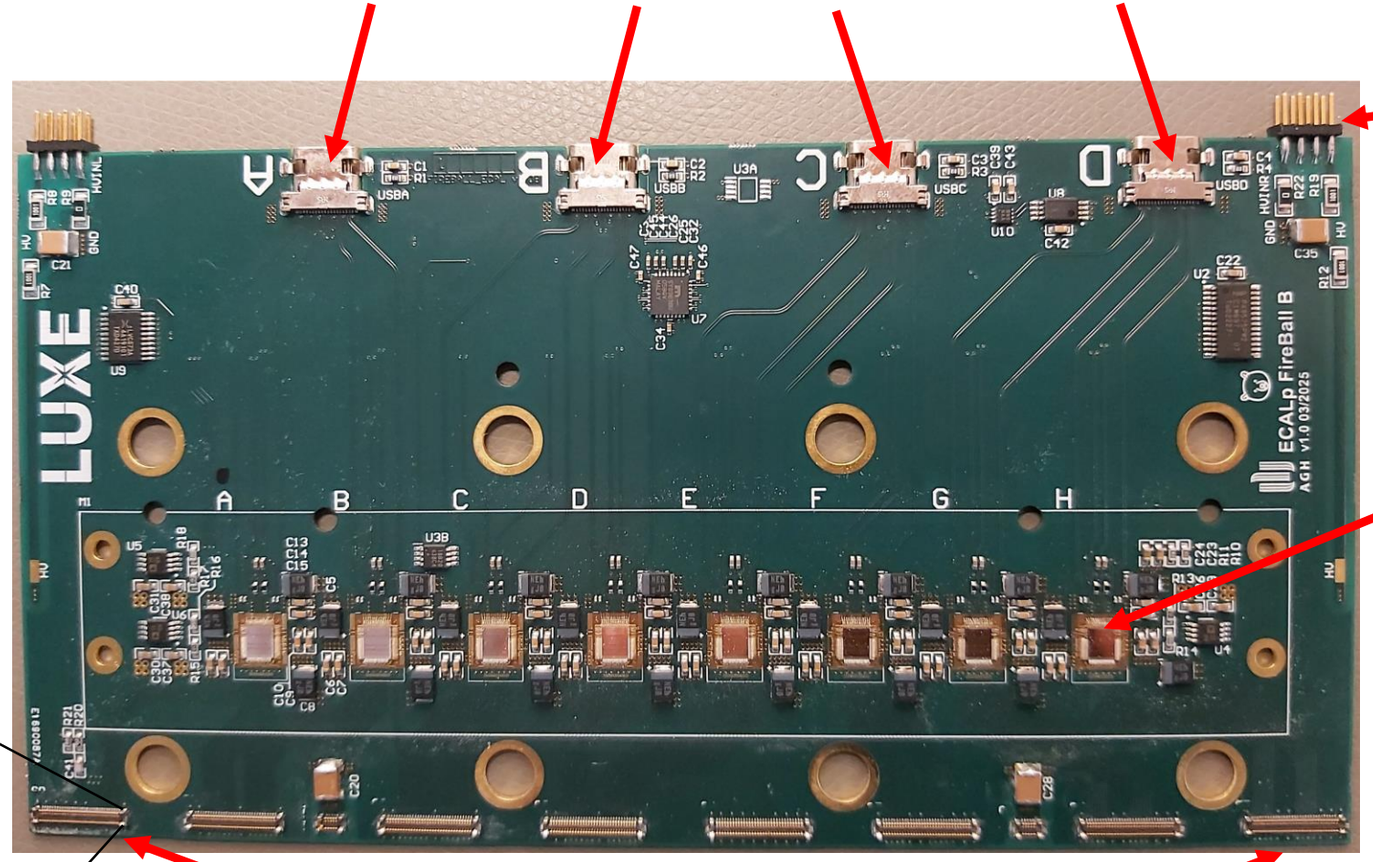
- One FPGA module / FEB
- Embedded Linux for system control and data uplink through 1 Gbps UDP Ethernet
- 10 Gbps uplink to DAQ PC



FEB – front end board

USB-C connectors: 16 x 5 Gbps data uplink, power supply, slow control

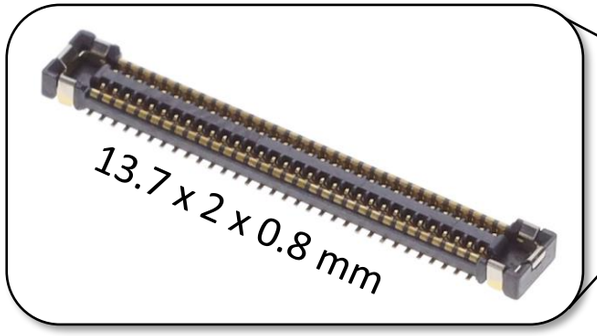
Similar FEB developed previously for LumiCal



Sensor bias

8 FLAME ASICs

Bare die wire-bonded to PCB



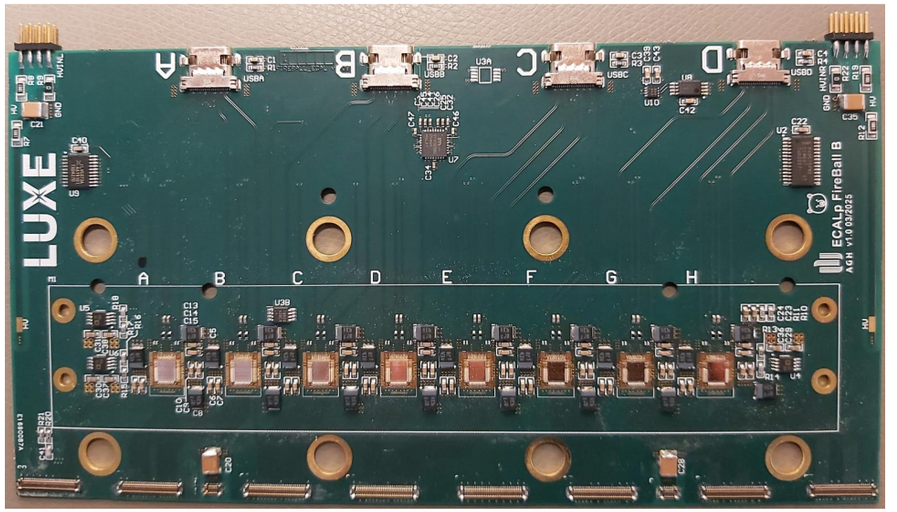
Sensor connectors

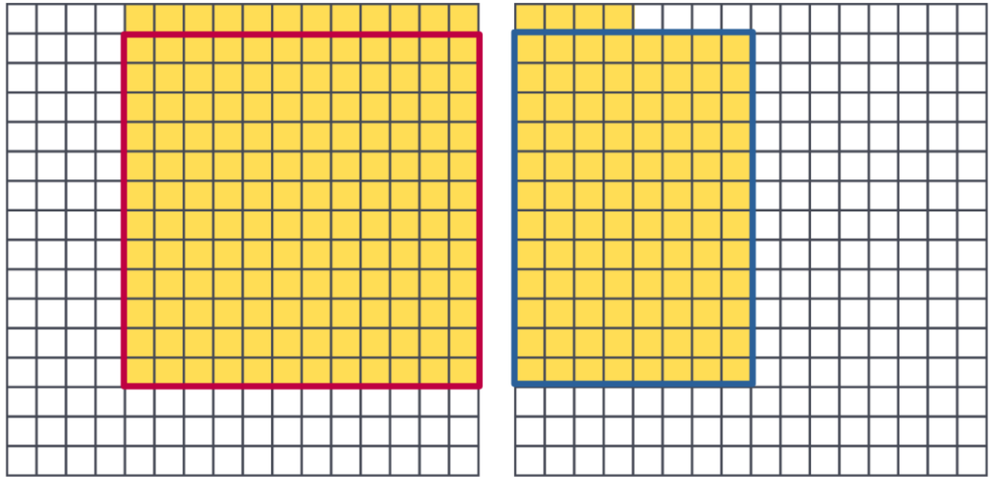
FEB – front end board

For 2025 LUXE testbeam, 256 FEB channels distributed between two sensors

- 12 columns x 13 rows one left sensor
- 8 columns x 12 rows on right sensor (+4 pads)

Main motivation – to test how the gap between sensors influence energy and spatial resolution of the ECALp

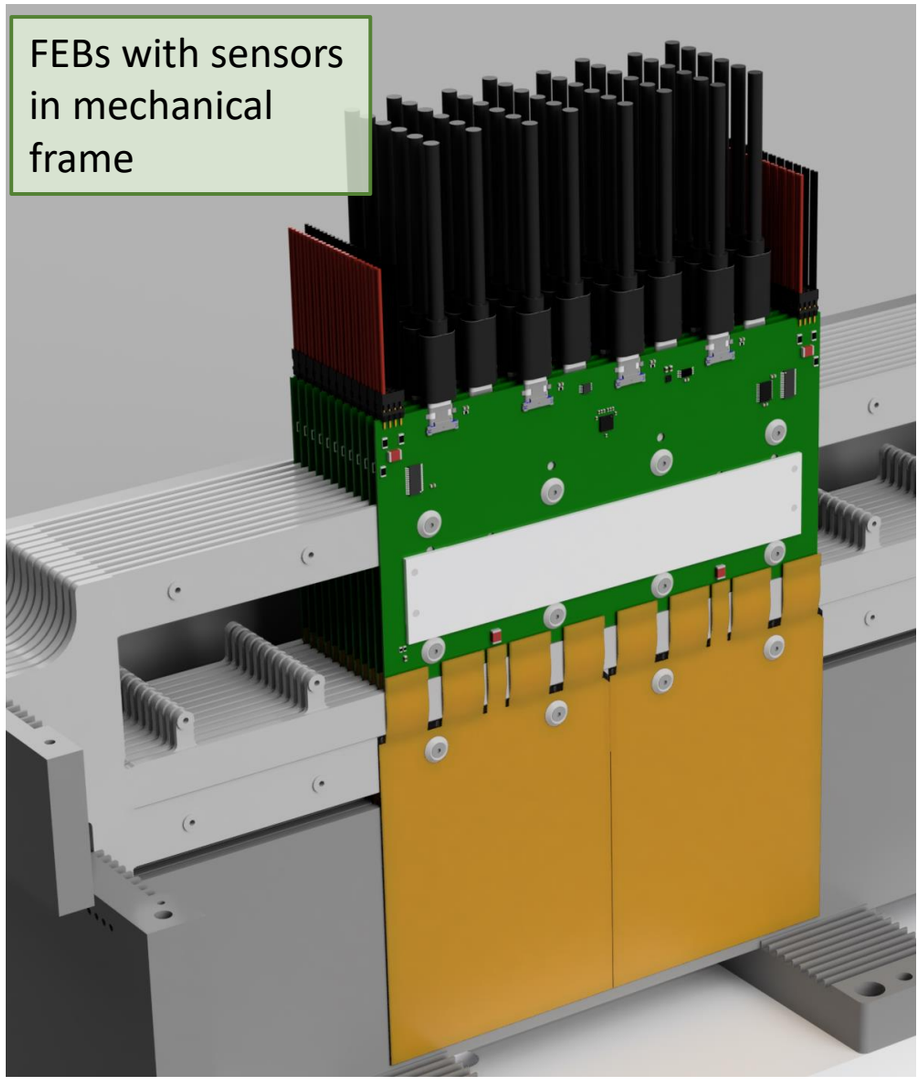




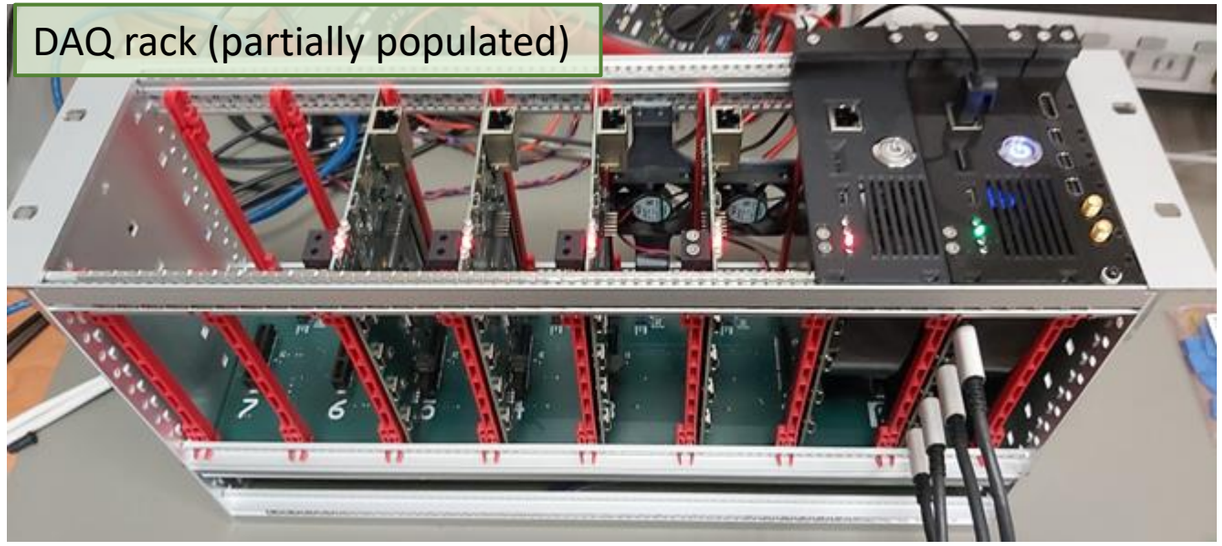
Not in scale

TB2025 readout hardware

FEBs with sensors in mechanical frame



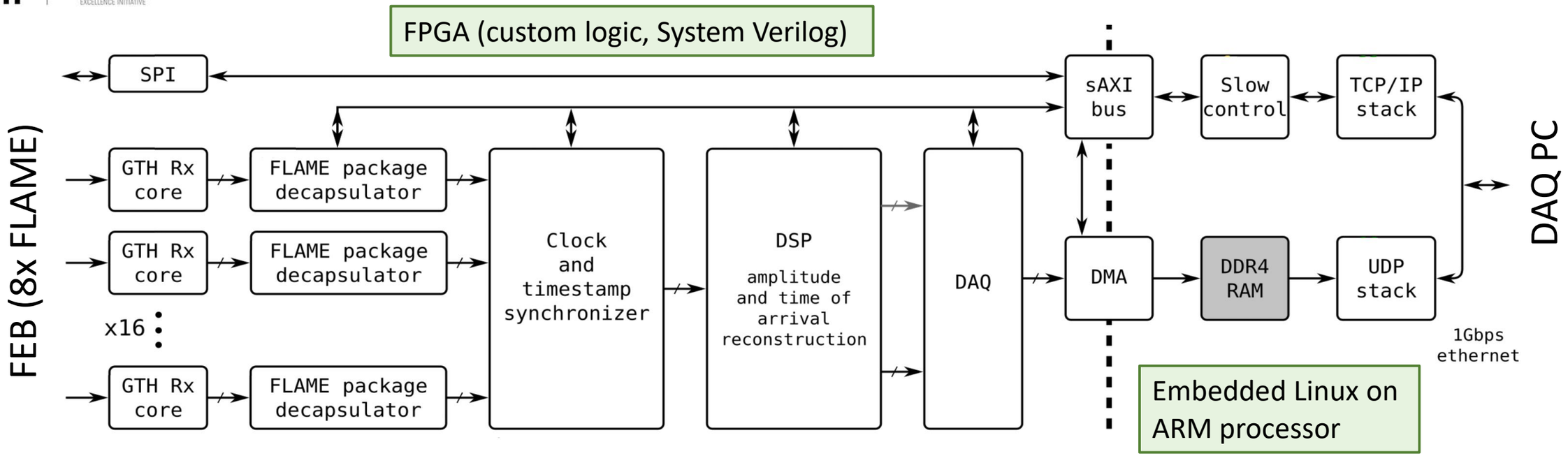
DAQ rack (partially populated)



DAQ card (single FPGA)

NICER PICTURE NEEDED!

DAQ – FPGA architecture

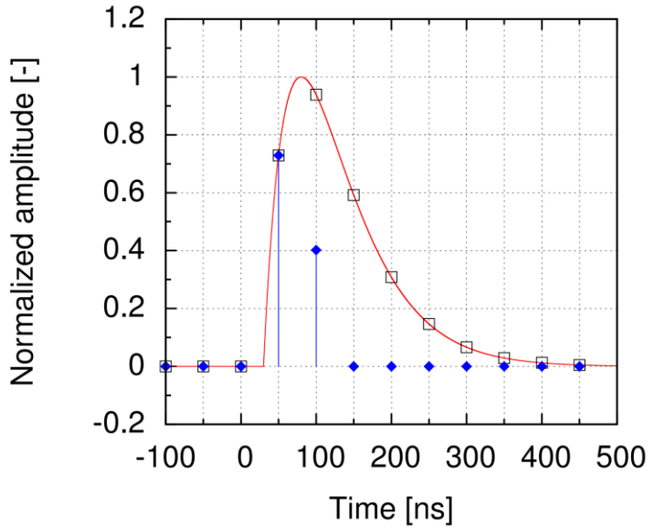


Zynq architecture – “regular” FPGA combined with quad-core ARM Cortex–A53

- FPGA part responsible for receiving FLAME data, decapsulating and aligning packages, data preprocessing (DSP) and online reconstruction using deconvolution
- Processed data passed to embedded Linux through DMA engine
- Embedded Linux for fast and effective development of UDP/TCP protocols, slow control and configuration

Deconvolution

Without beam clock (e.g. cosmic muons) ADC sampling is asynchronous with FE pulse



FE pulse

$$|V_{\text{front-end}}(t)| = \frac{q_{\text{in}}}{C_{\text{feed}}} \left(\frac{t}{\tau_{\text{sh}}} \right) e^{-\frac{t}{\tau_{\text{sh}}}}$$

- ADC samples
- Digital filter (FIR) samples d_i

$$d_i = v_i - 2e^{-\frac{T_{smp}}{\tau_{\text{sh}}}} v_{i-1} + e^{-\frac{2T_{smp}}{\tau_{\text{sh}}}} v_{i-2}$$

Amplitude A and time of arrival (TOA) t_0 reconstructed as, respectively, weighted sum and ratio of two non-zero d_i samples, output from FIR digital filter

Amplitude

$$A = (d_1 + d_2) \frac{\tau_{\text{sh}} e^{\frac{T_{smp} - t_0 - \tau_{\text{sh}}}{\tau_{\text{sh}}}}}{T_{smp} - t_0 \left(1 - e^{-\frac{T_{smp}}{\tau_{\text{sh}}}} \right)}$$

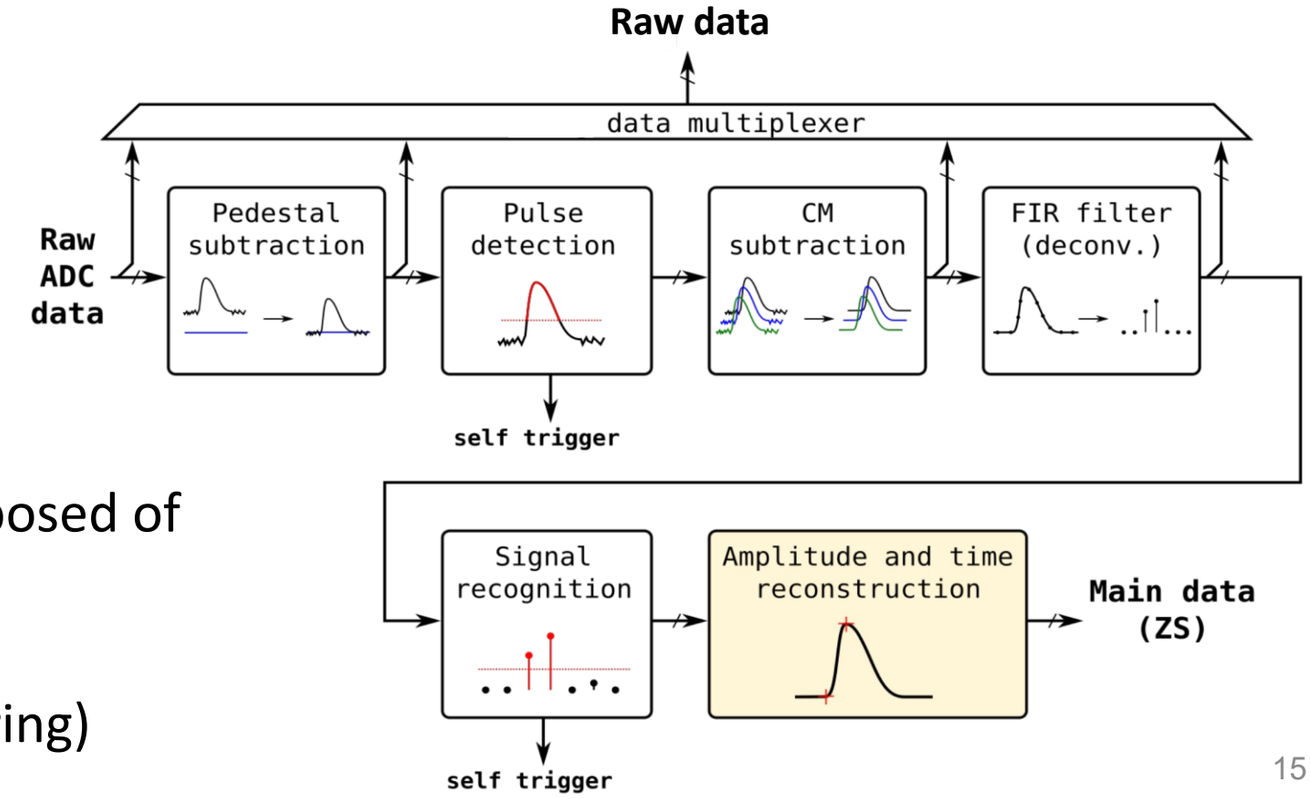
TOA

$$t_0 = \frac{\frac{d_2}{d_1} T_{smp}}{\frac{d_2}{d_1} + e^{-\frac{T_{smp}}{\tau_{\text{sh}}}}}$$

Data preprocessing and reconstruction

Data preprocessing and reconstruction performed online for all 256 channels:

- Pedestal subtraction (with procedure for pedestal calculation in embedded Linux)
- Rough pulse detection (to exclude from CM calculation channels with signal)
- Common mode calculation and subtraction
- FIR digital filtering
- Detailed signal detection for zero suppressing (ZS)
- Amplitude and TOA reconstruction using deconvolution

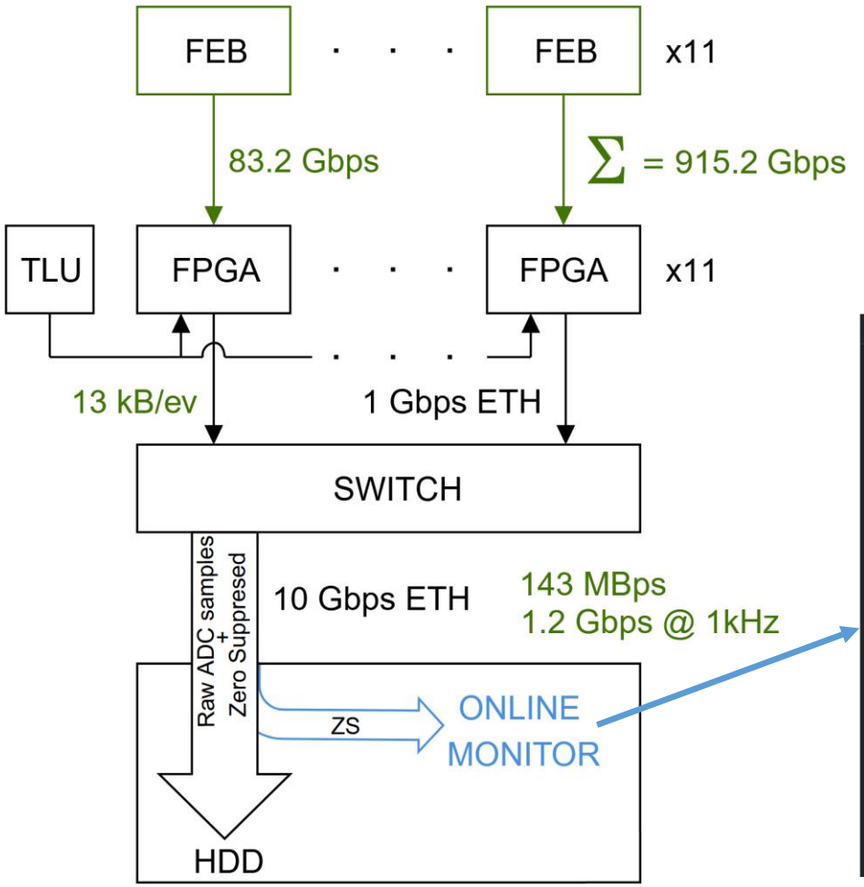


Outgoing data can be (on demand) composed of

- Raw ADC samples (default)
- Partially processed samples
- ZS reconstructed data (online monitoring)

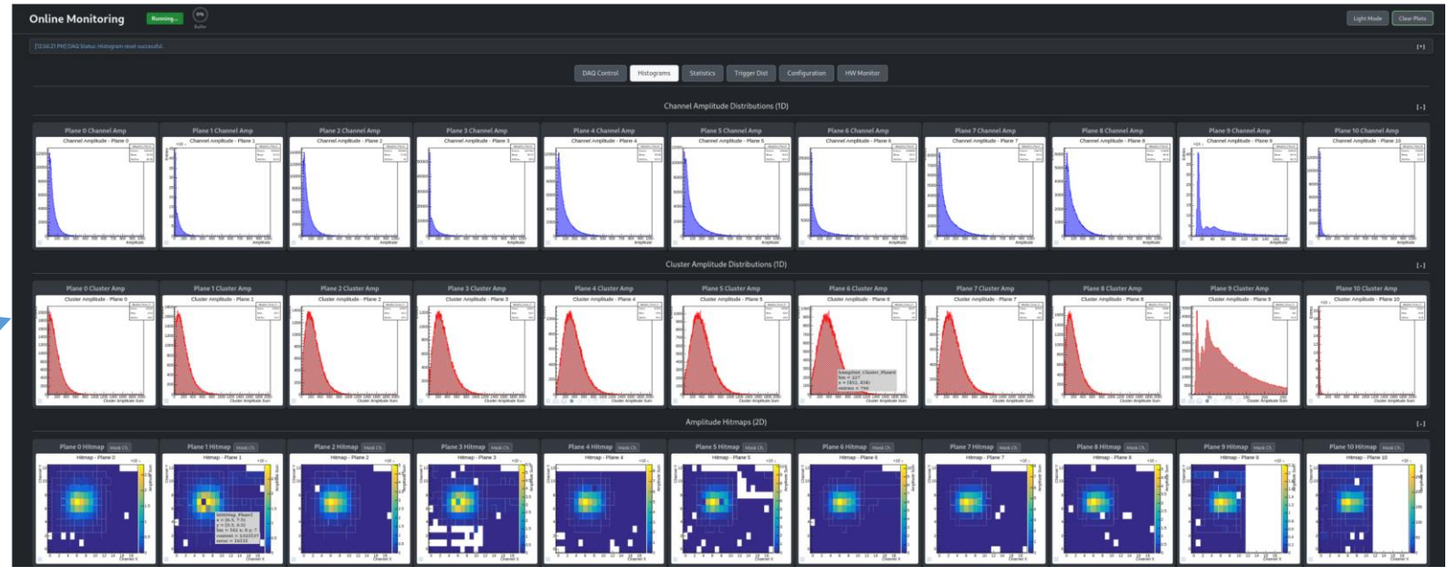
DAQ – software and bandwidth

Data from all FPGA boards collected using EUDAQ producer on a dedicated PC.
Raw ADC samples and ZS reconstructed data stored on HDDs, with ZS data extracted to webpage-based data quality online monitoring.



During 2025 testbeam 11 FEBs were instrumented

- 915.2 Gbps of continuous data stream from FLAMEs
- Reduced by FPGAs to 1.2 Gbps at 1 kHz event rate
- System stable up to 2 kHz (>2 Gbps of outgoing data)



References and acknowledgments

- FLAXE, a SoC readout ASIC for electromagnetic calorimeter at LUXE experiment, Jakub Moroń et al 2025, *JINST* 20 C01026 https://doi.org/10.1088/1748-0221/20/01/C01026
- An ultra-low power 10-bit, 50 MSps SAR ADC for multi-channel readout ASICs, Mirosław Firlej *et al* 2023, *JINST* 18 P11013 https://doi.org/10.1088/1748-0221/18/11/P11013
- FLAME SoC readout ASIC for electromagnetic calorimeter, Jakub Moroń et al, TWEPP 2022 Topical Workshop on Electronics for Particle Physics, https://indico.cern.ch/event/1127562/contributions/4904506/
- The FLAME and FLAXE ASICs, Marek Idzik et al, XII Front-End Electronics Workshop, https://agenda.infn.it/event/36206/contributions/202659/

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PLEASE SEND ME ANY ACKNOWLEDGMENTS YOU WANT TO PUT HERE!

Summary

- Complete readout system for compact electromagnetic calorimeter developed and successfully used in testbeam campaigns in last six years
  - 32-channel, low power FLAME readout ASIC, with 10b ADC in each channel and two 5.2 Gbps data serializers
  - FPGA-based DAQ system with online data processing and reconstruction

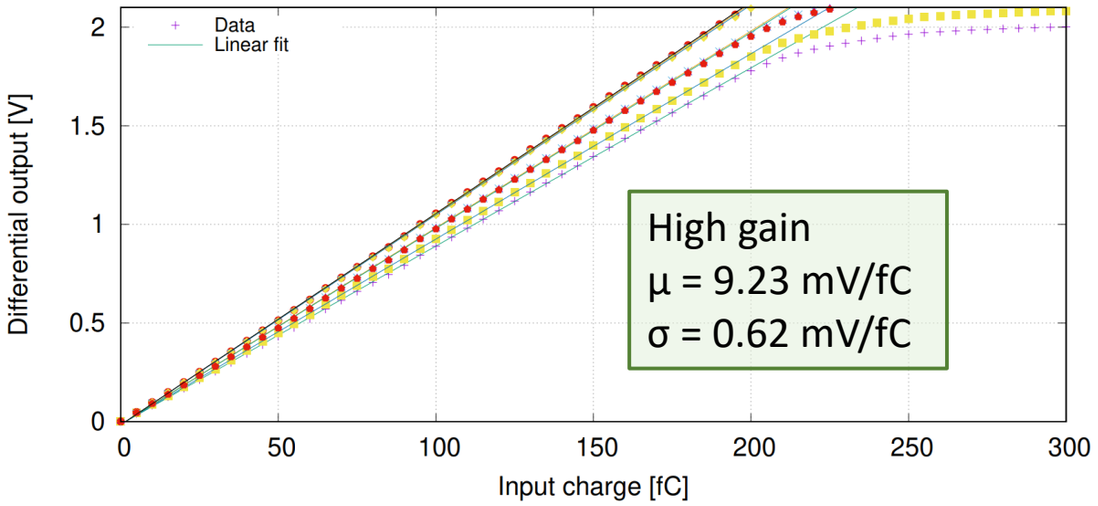
- Design adapted for ECALp testbeam due to the production failure of new ASIC, FLAXE

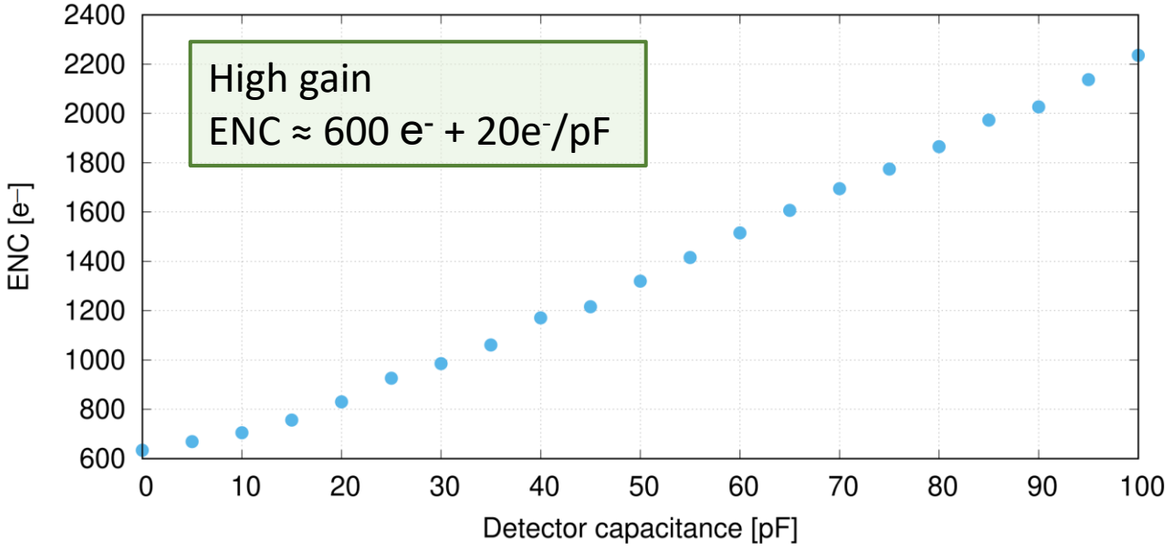
- Readout system successfully used with 11 layers, during 2025 testbeam of ECALp
  - FPGAs farm handling and processing almost 1 Tbps of incoming data
  - System fully stable at 2 kHz event rate, with >2 Gbps of outgoing data

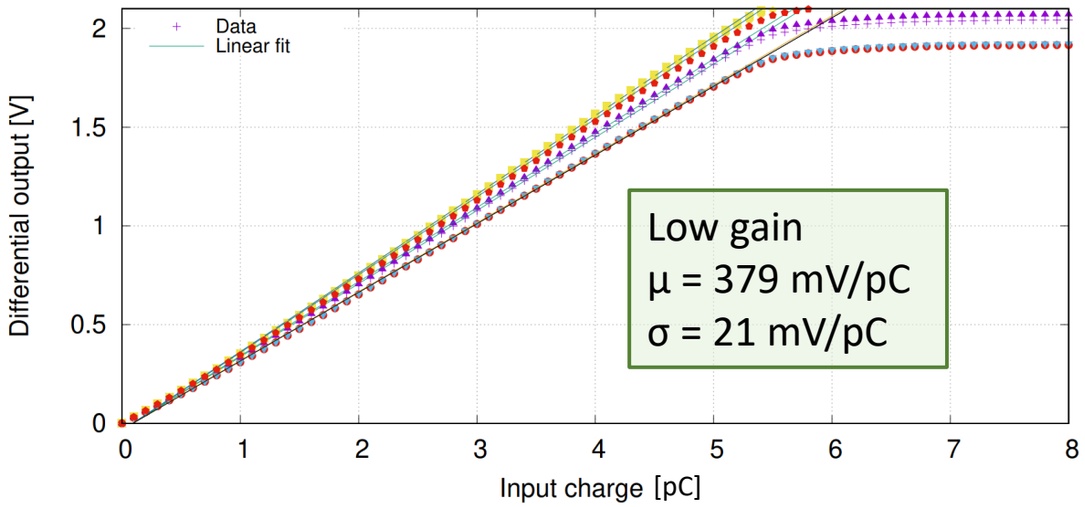
- EUDAQ producer with website-based frontend for remote access to system control and data quality monitoring developed and successfully used

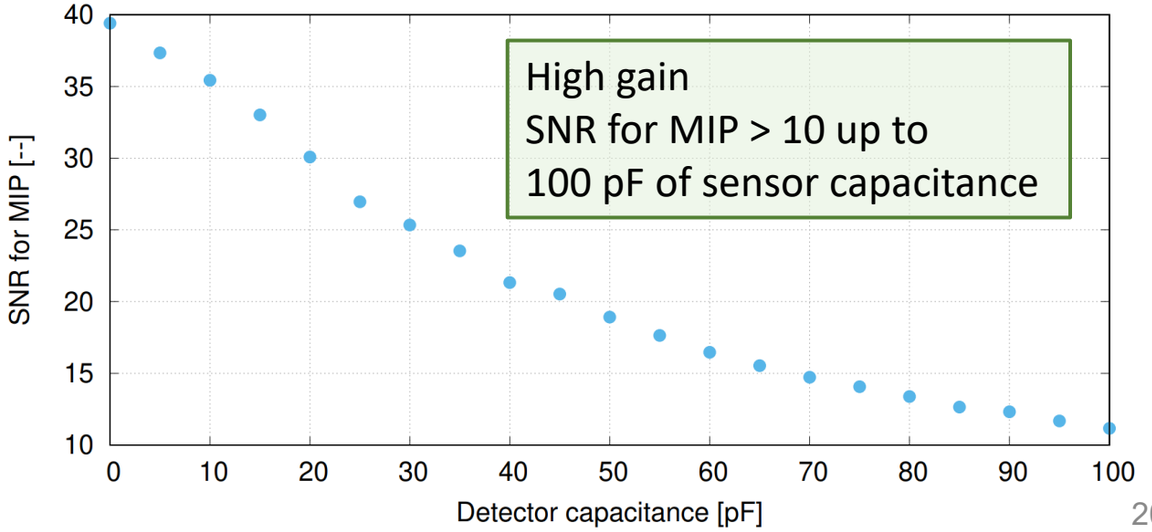
Backup materials

FLAME – front end performance









FLAME – power consumption

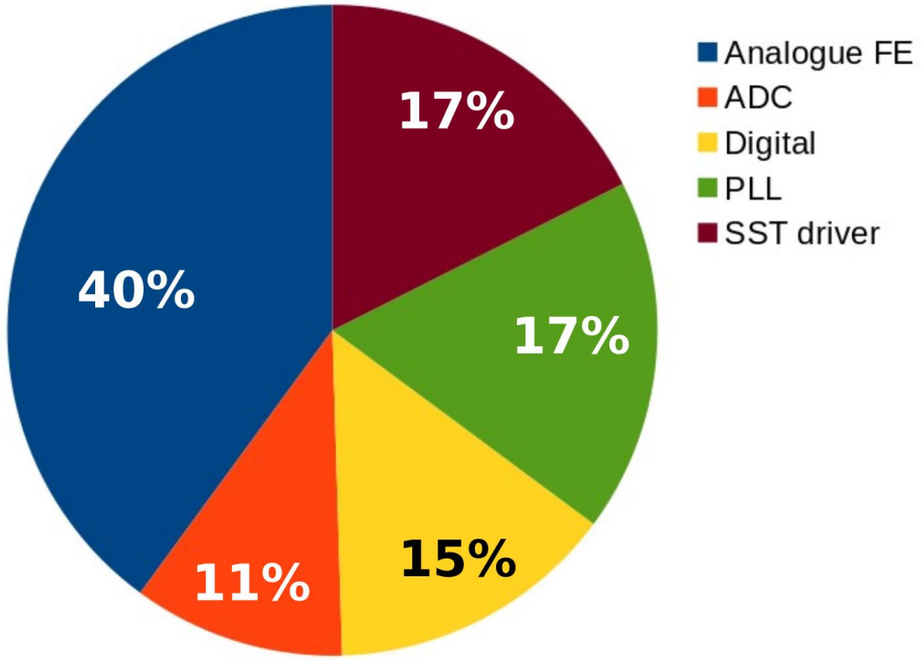
Average power consumption per channel

3.1 mW / channel

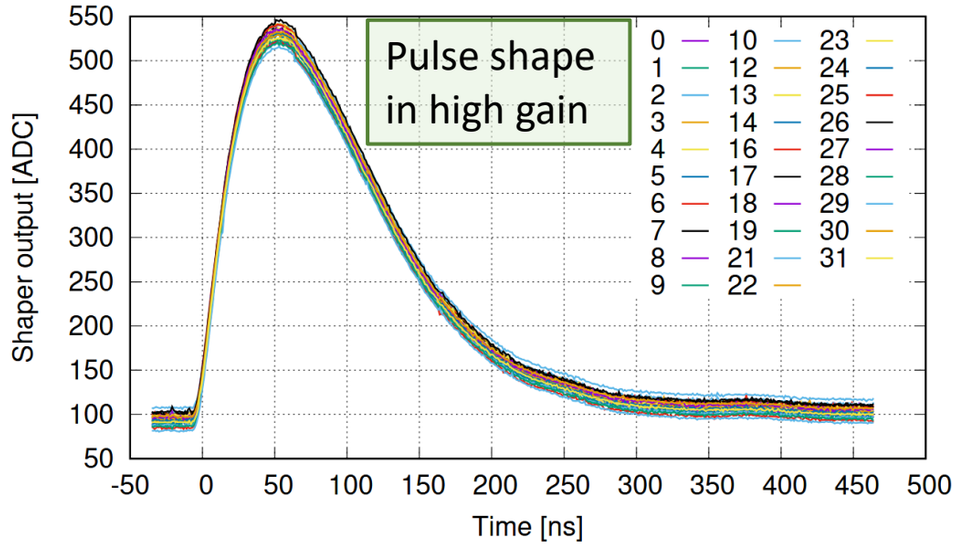
- Analogue front-end: 1.25 mW/channel
- ADC : 0.33 mW/channel
- Digital backend : 0.45 mW/channel
- PLL : 0.55 mW/channel
- SST driver : 0.55 mW/channel

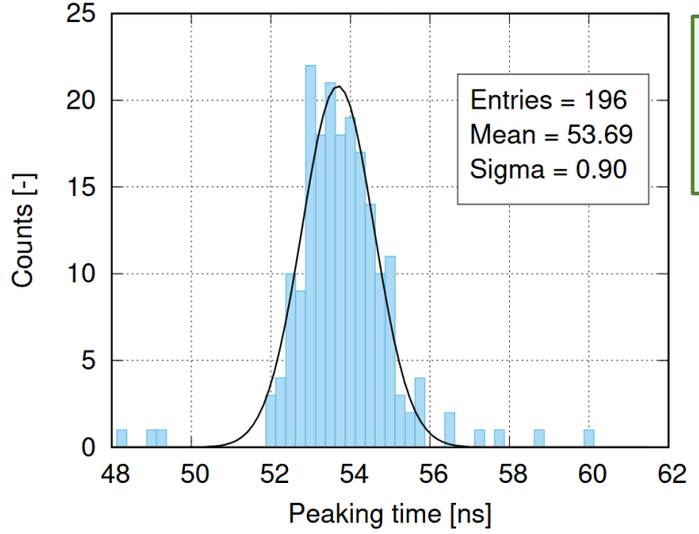
Total ASIC consumption: **100 mW**

- Analogue front-end: 40.0 mW
- ADC : 10.6 mW
- Digital backend : 14.4 mW
- PLLs : 17.6 mW
- SST drivers : 17.6 mW

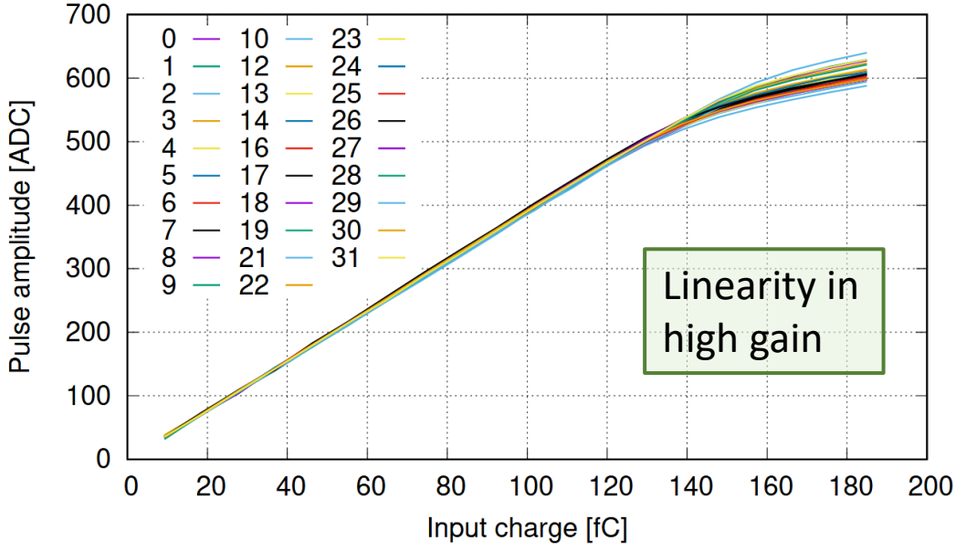


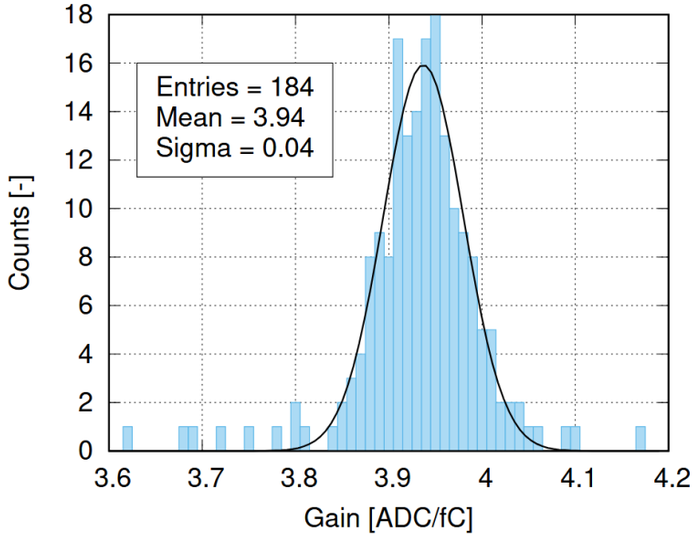
FLAXE – front end performance





Peaking time
μ = 53.7 ns
σ = 0.9 ns

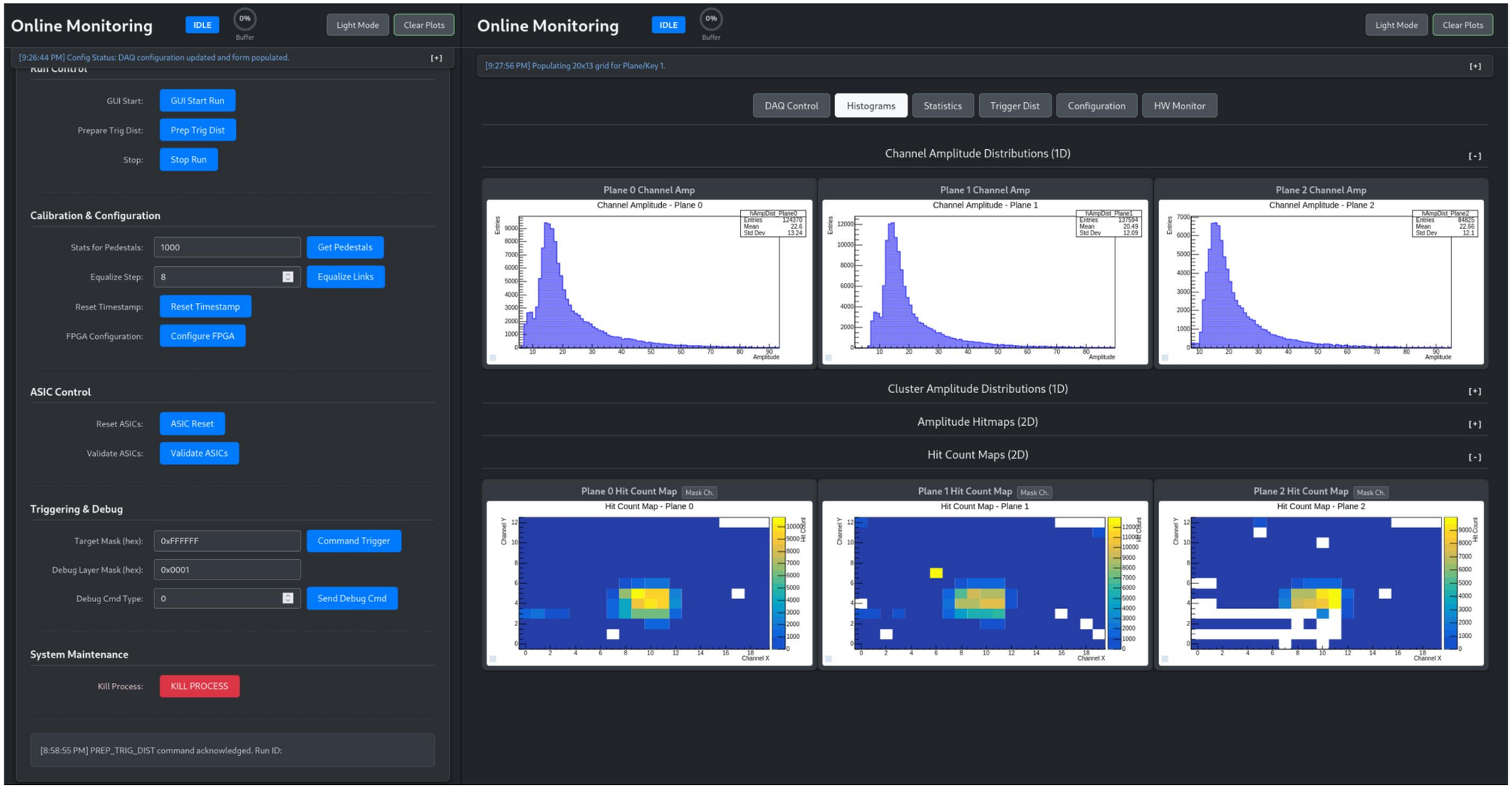




High gain
μ = 3.94 LSB/fC
σ = 0.04 LSB/fC

Website for online monitor and control

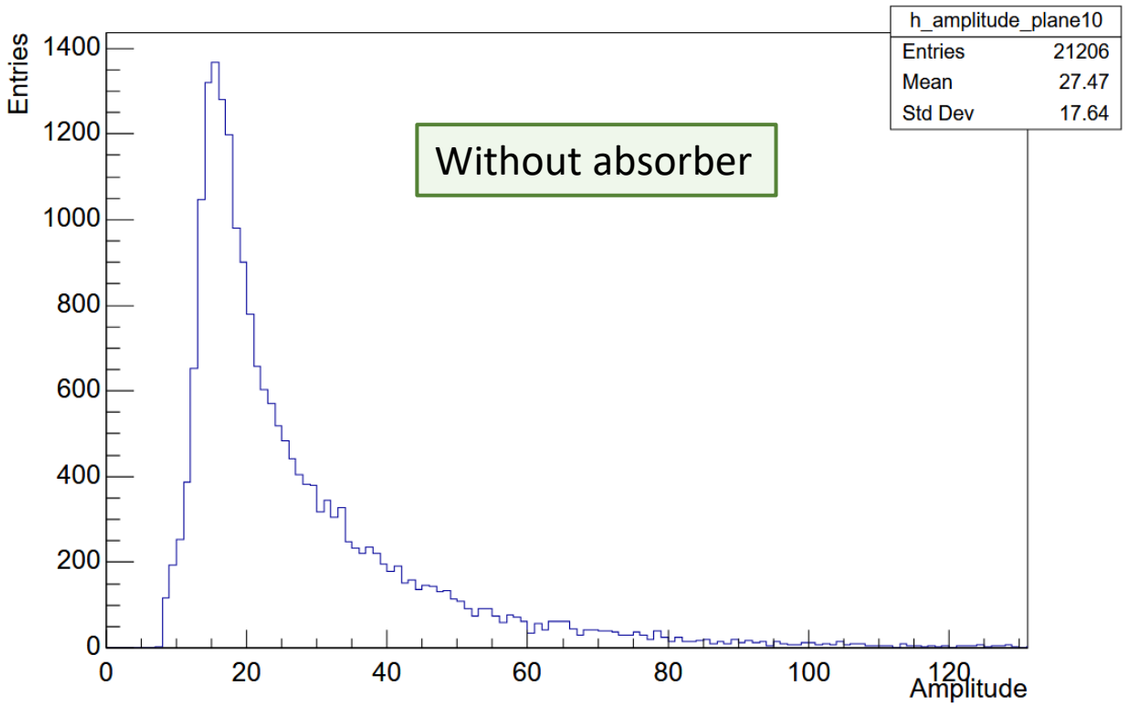
Website-based online monitoring and DAQ control – remote access

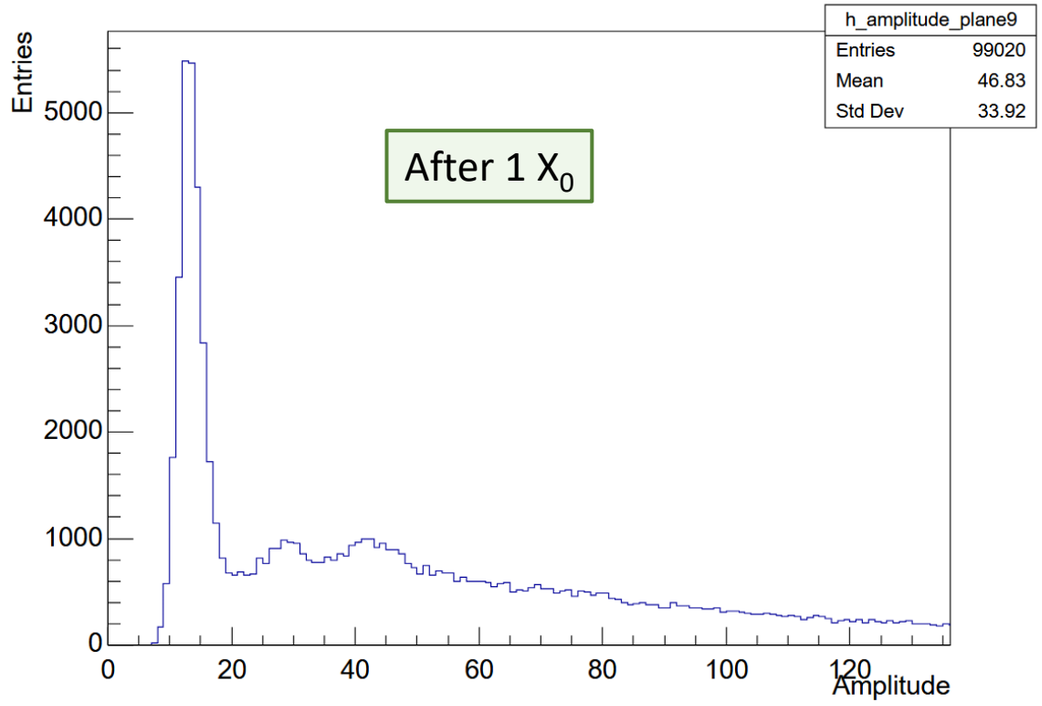


Example of testbeam data

Examples of online reconstructed data:

- Without absorber – pure Landau-Gauss distribution, MPV around 15 LSB
- After one absorber layer (1 X_0) – one, two and three MIP peaks visible



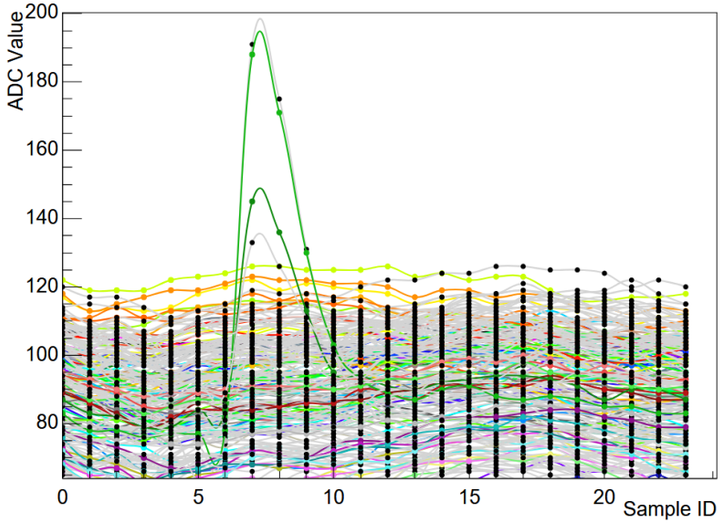


Data preprocessing

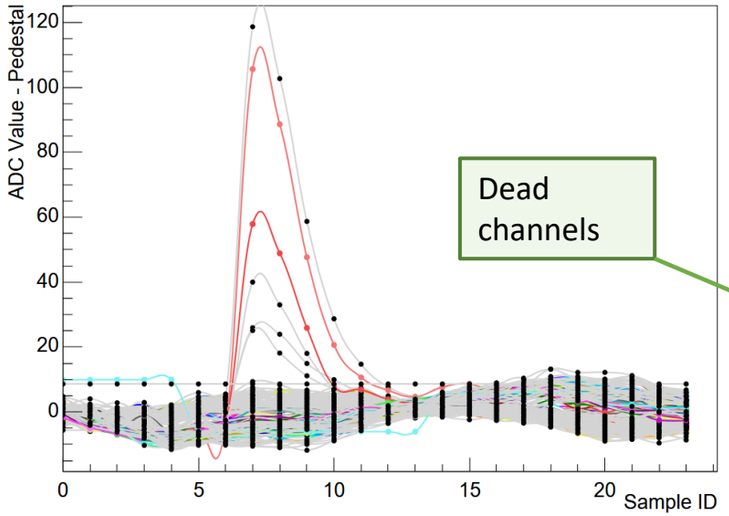
Example of data preprocessing:

- Raw ADC samples (left) from a single event and single FEB (256 channels)
- Pedestal subtracted data (center) – sine oscillation visible
- Common mode subtracted data (right) – oscillation removed almost completely
- Two dead (not responding/misbehaving) channels can be clearly seen after CMS

Raw ADC data



Pedestal subtracted



Pedestal and CM subtracted