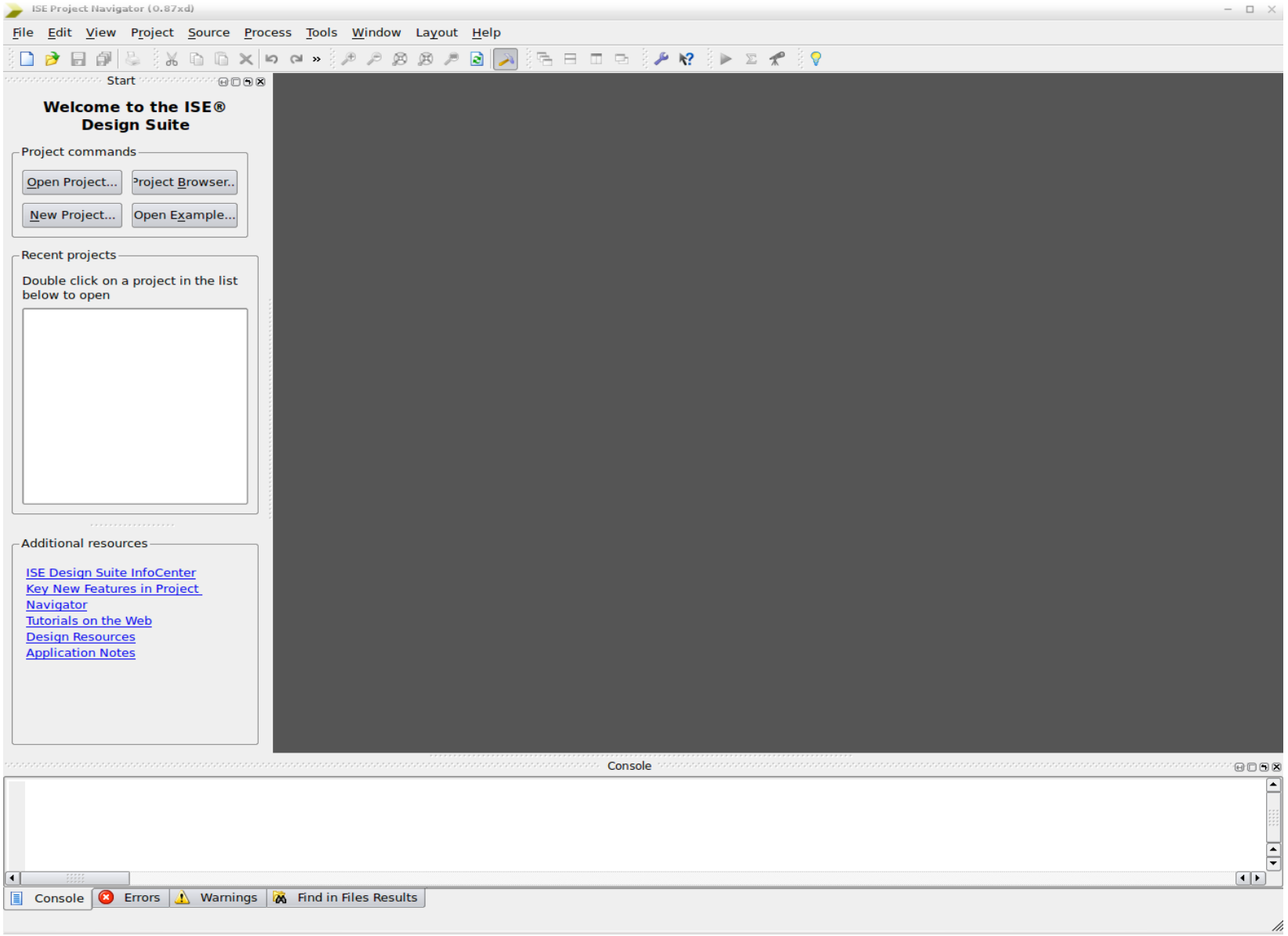
Xilinx ISE

Introduction

First Steps with ISE

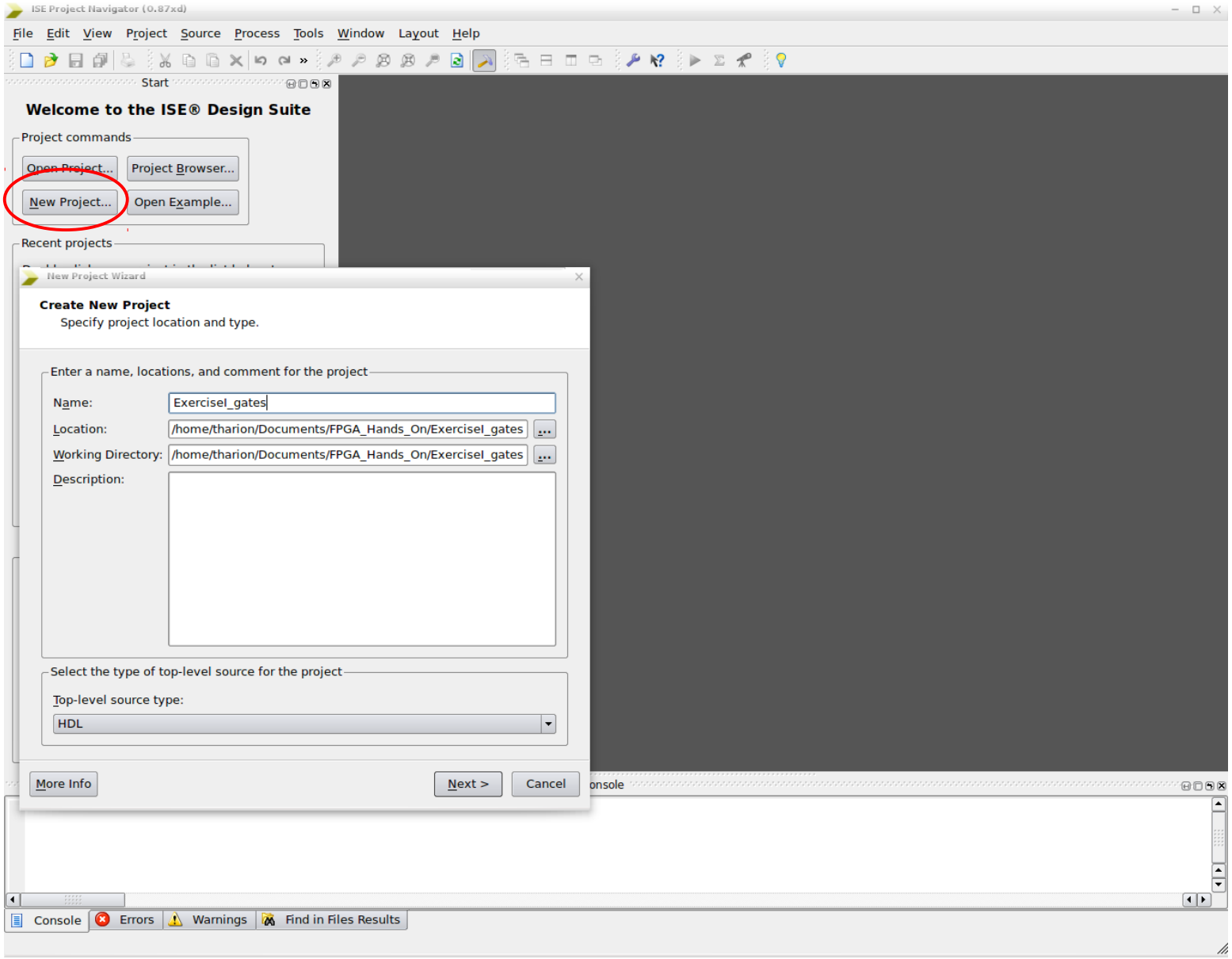
- ISE Project Navigator
  - Creating a new project
  - Adding new design sources
- Design Flow
  - Synthesising the design
    - RTL Viewer
    - Technology Viewer
  - Implementing the Desing
    - Tranlate, Map, Place and Route
    - Generate Programming File
- Programm the FPGA

Step1: Starting ISE



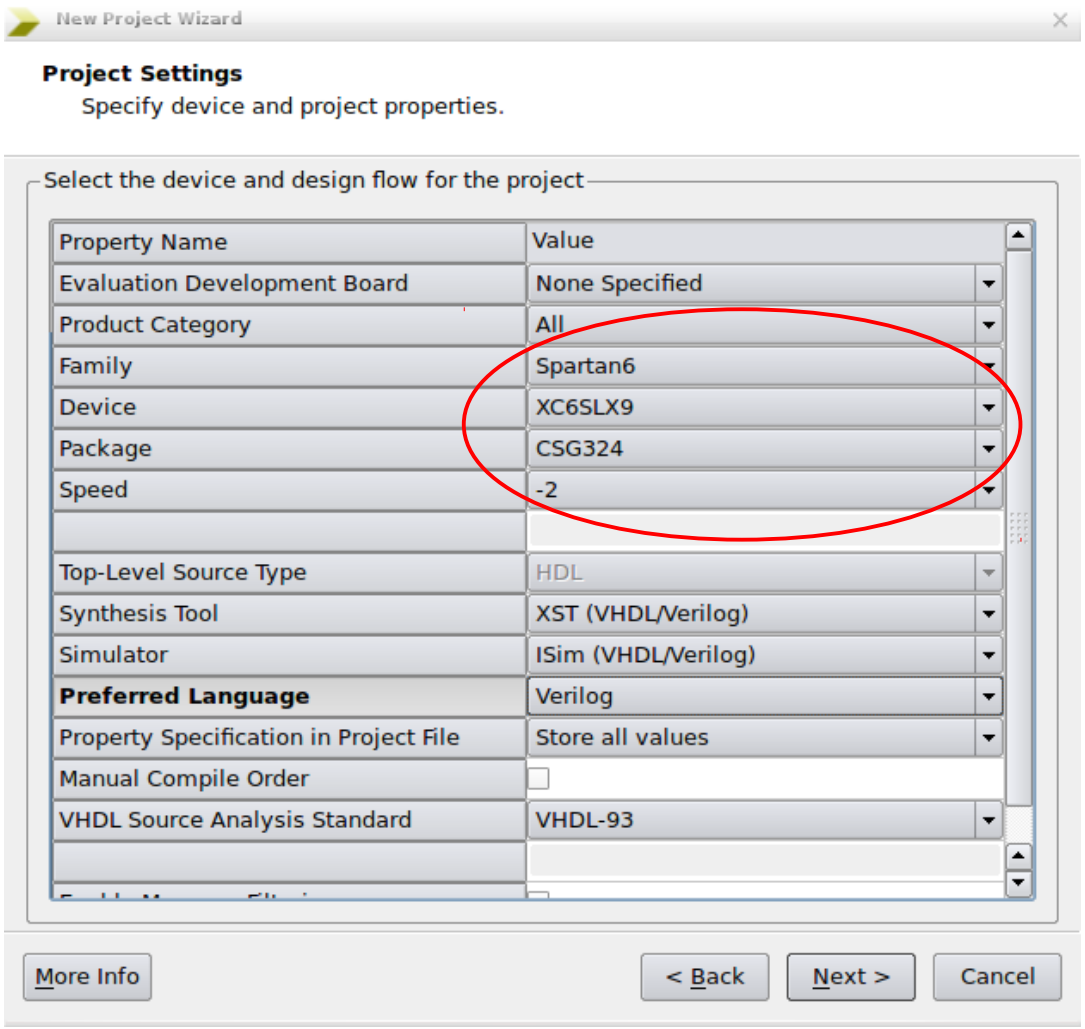
Start ISE by opening a terminal and running "xilinx" and "ise"

Step 2: Creating a new project



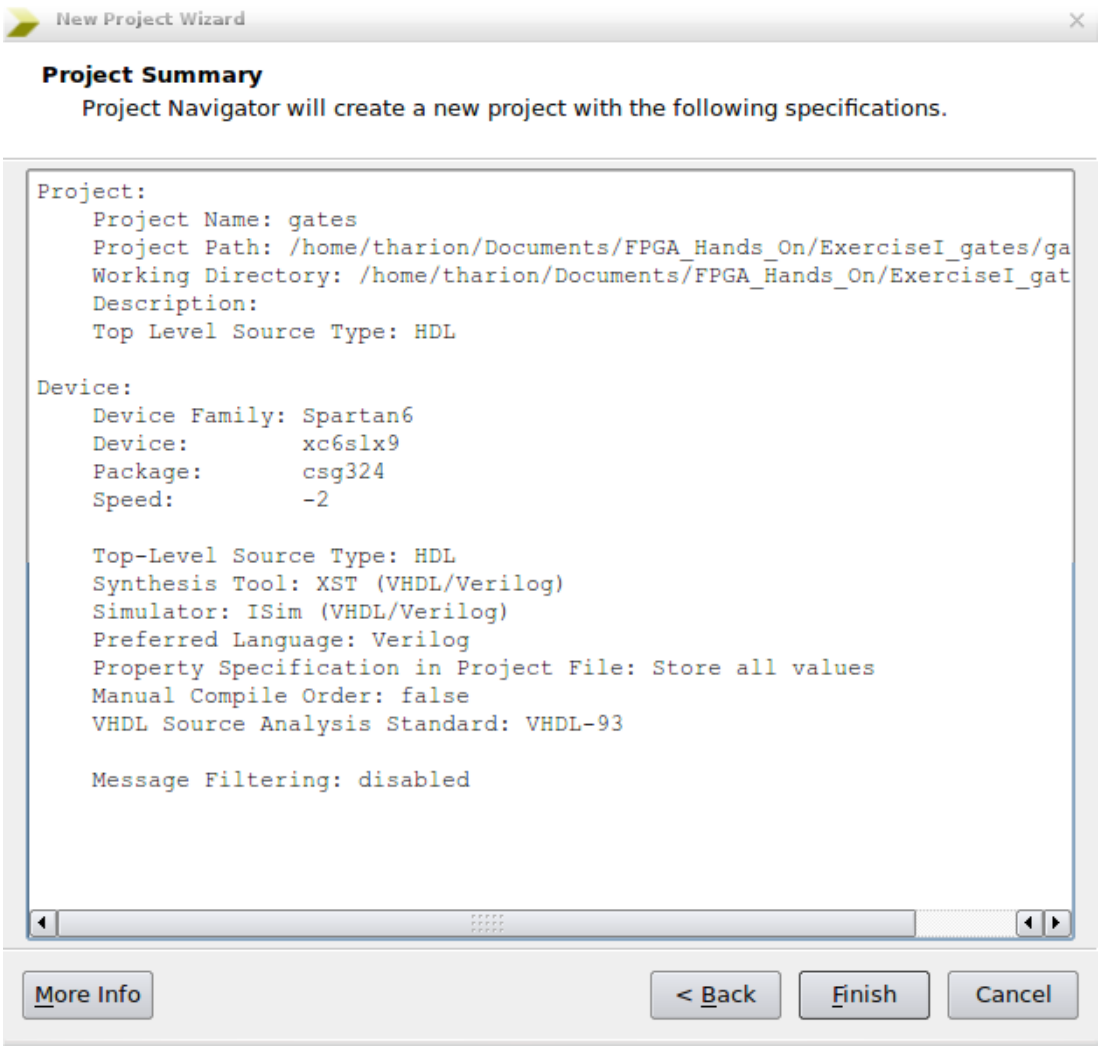
Create a new project using the "New Project" button

Step 2: Creating a new project



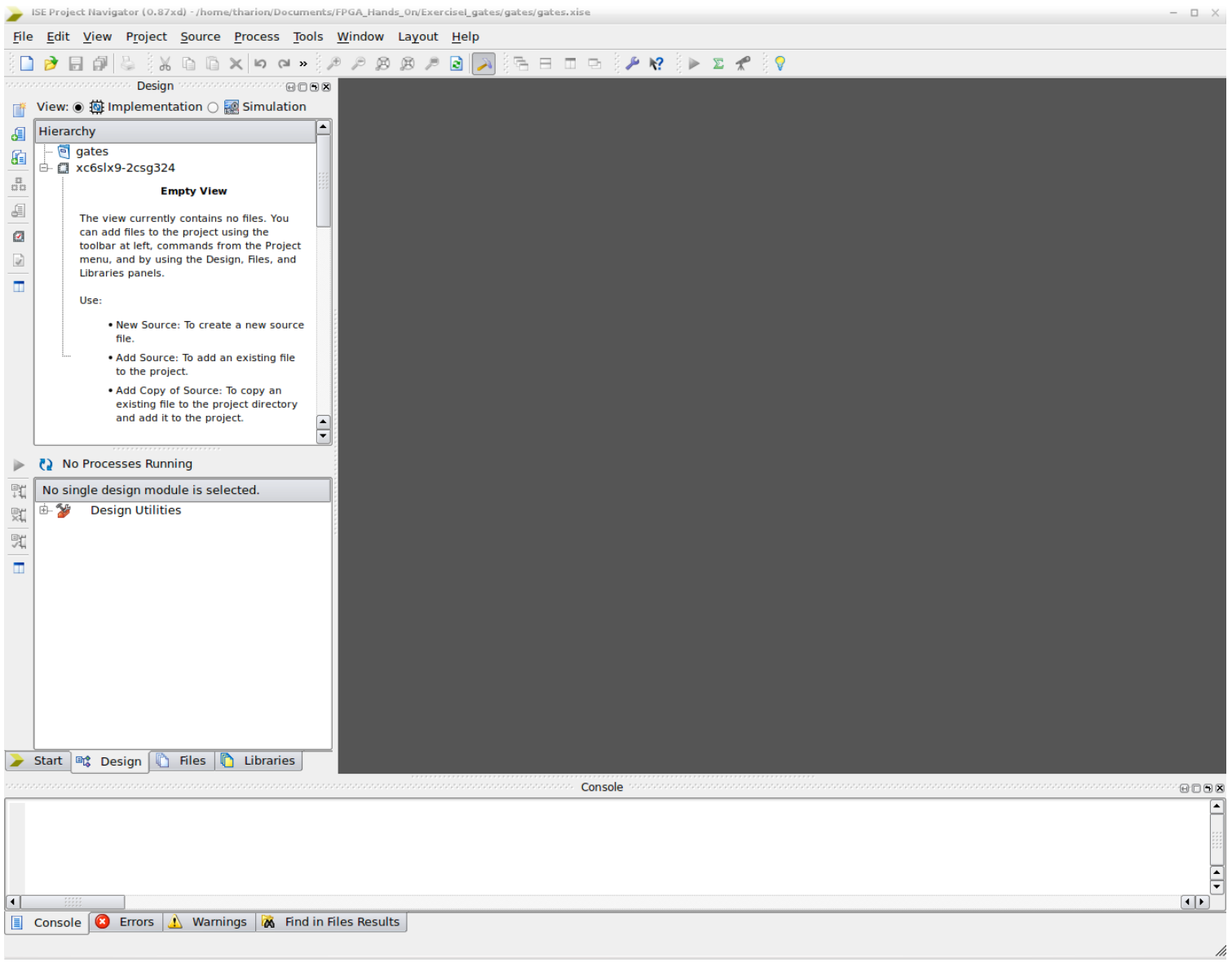
In the project settings choose the appropriate device family and package

Step 2: Creating a new project



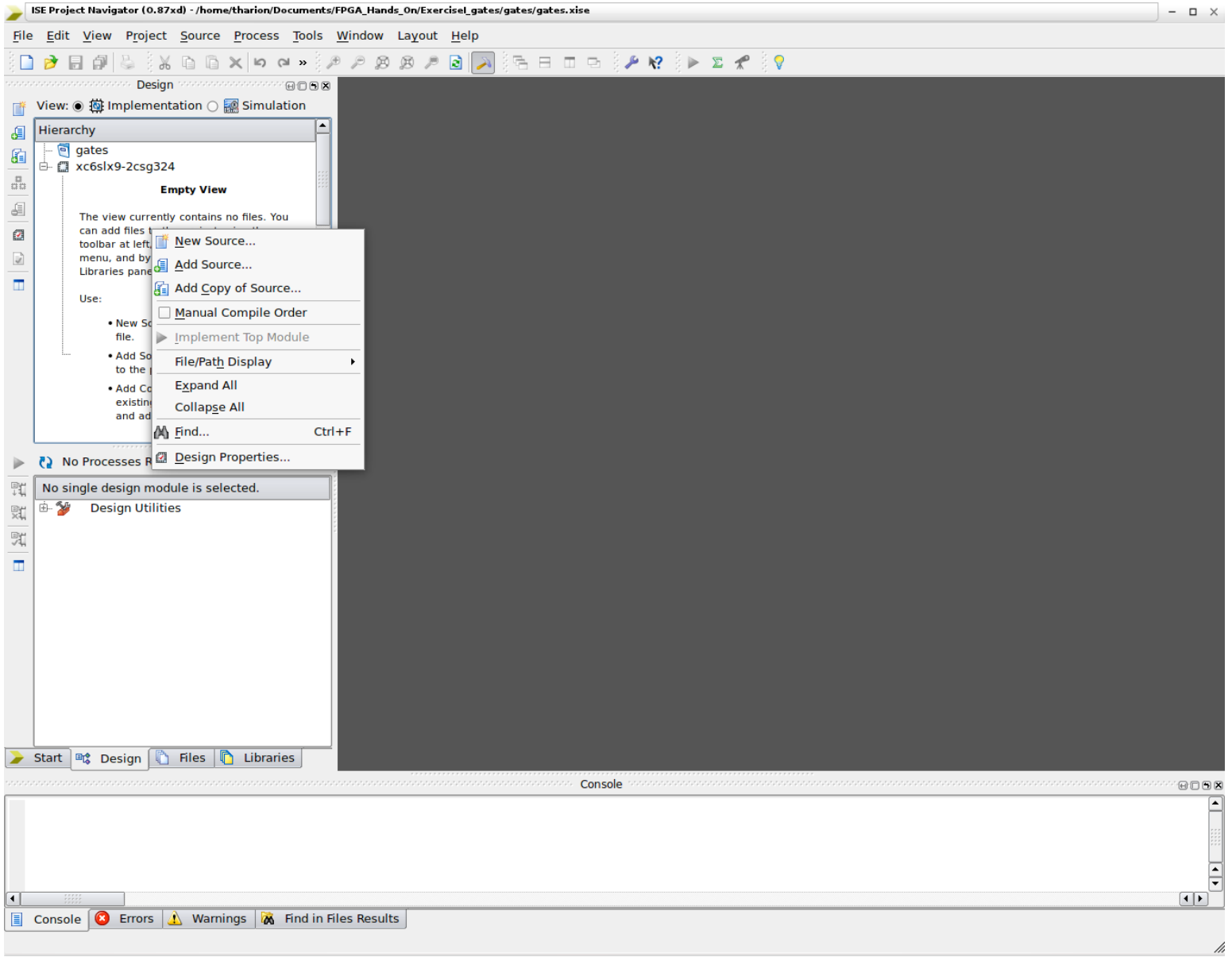
Click "Finish" to create the new project

Step 2: Creating a new project



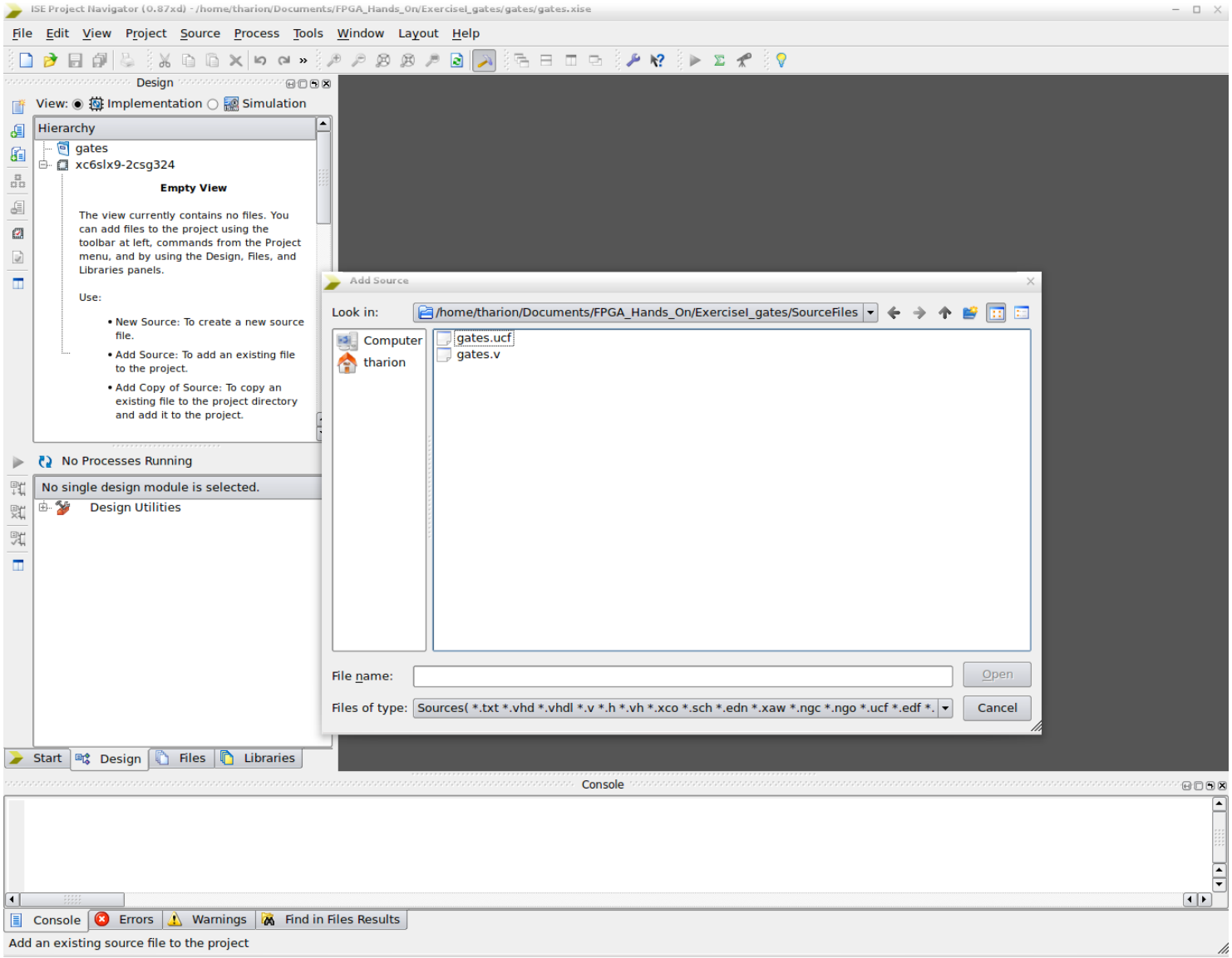
You have now created an empty project for the Spartan6-LX9 device

Step 3: Adding Design Sources



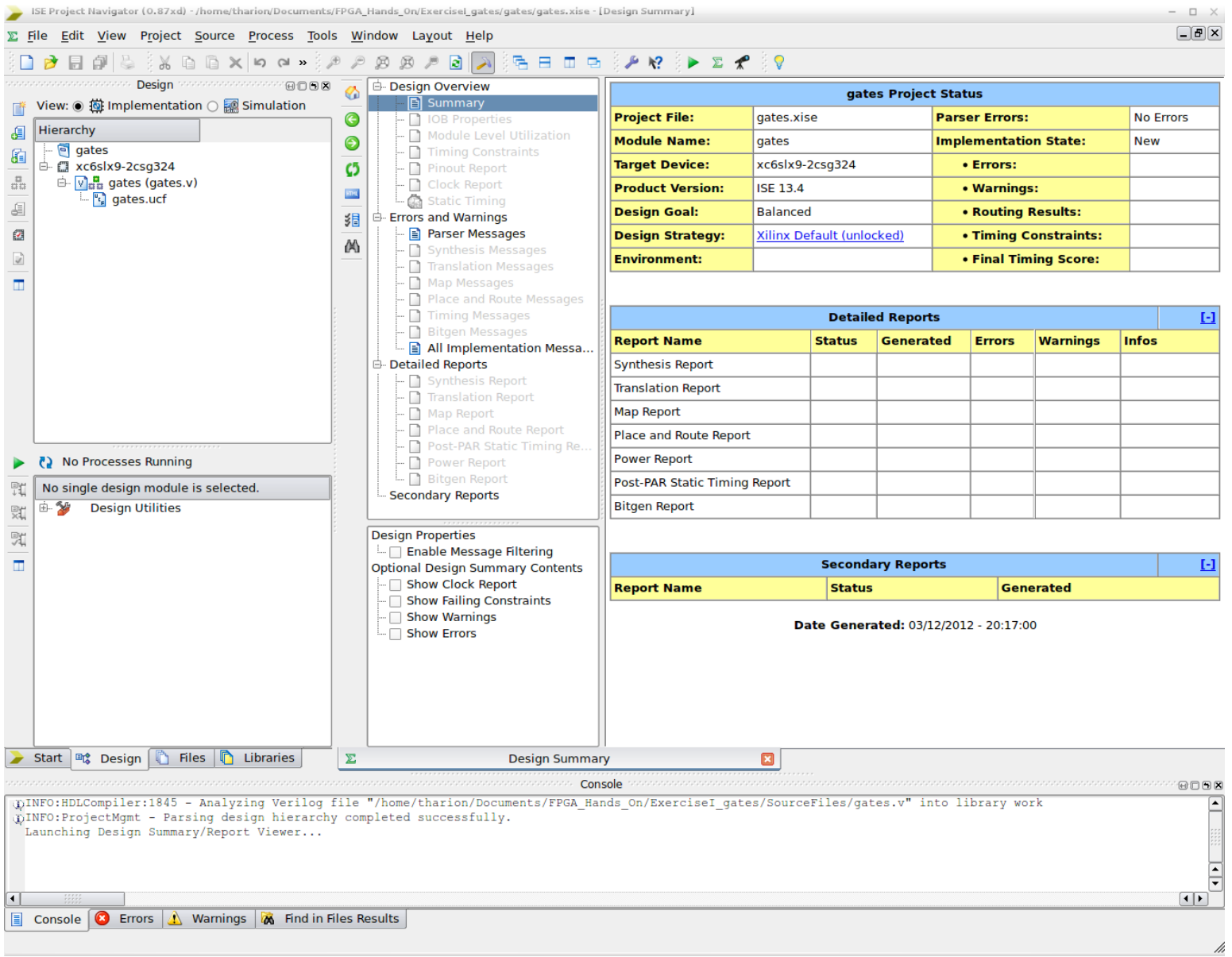
Right-click on the "Empty View" Area and choose "Add Source"

Step 3: Adding Design Sources



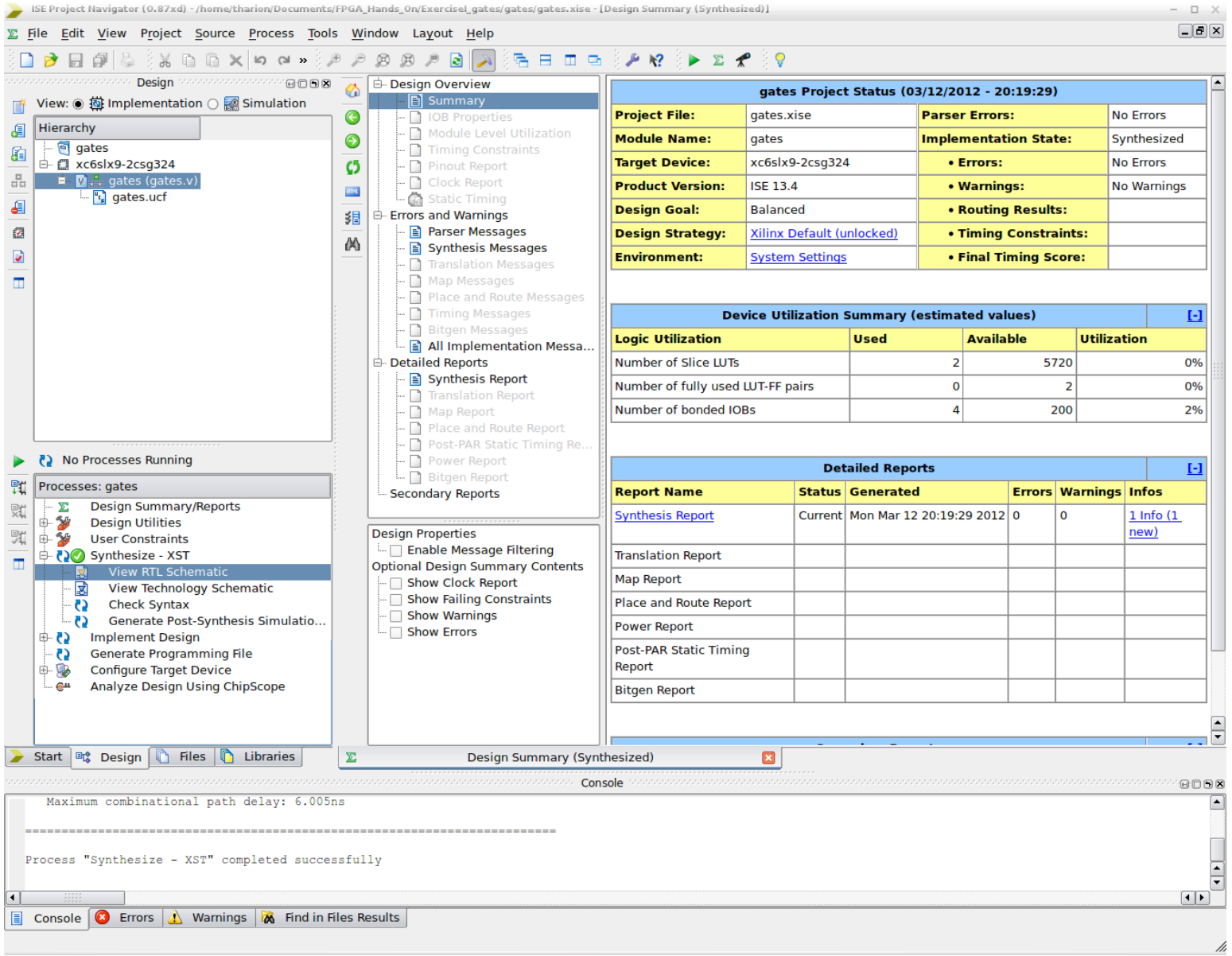
Browse to the source folder and select the files "gates.v" and "gates.ucf" containing the design and the constraints for the current project

Step 3: Adding Design Sources



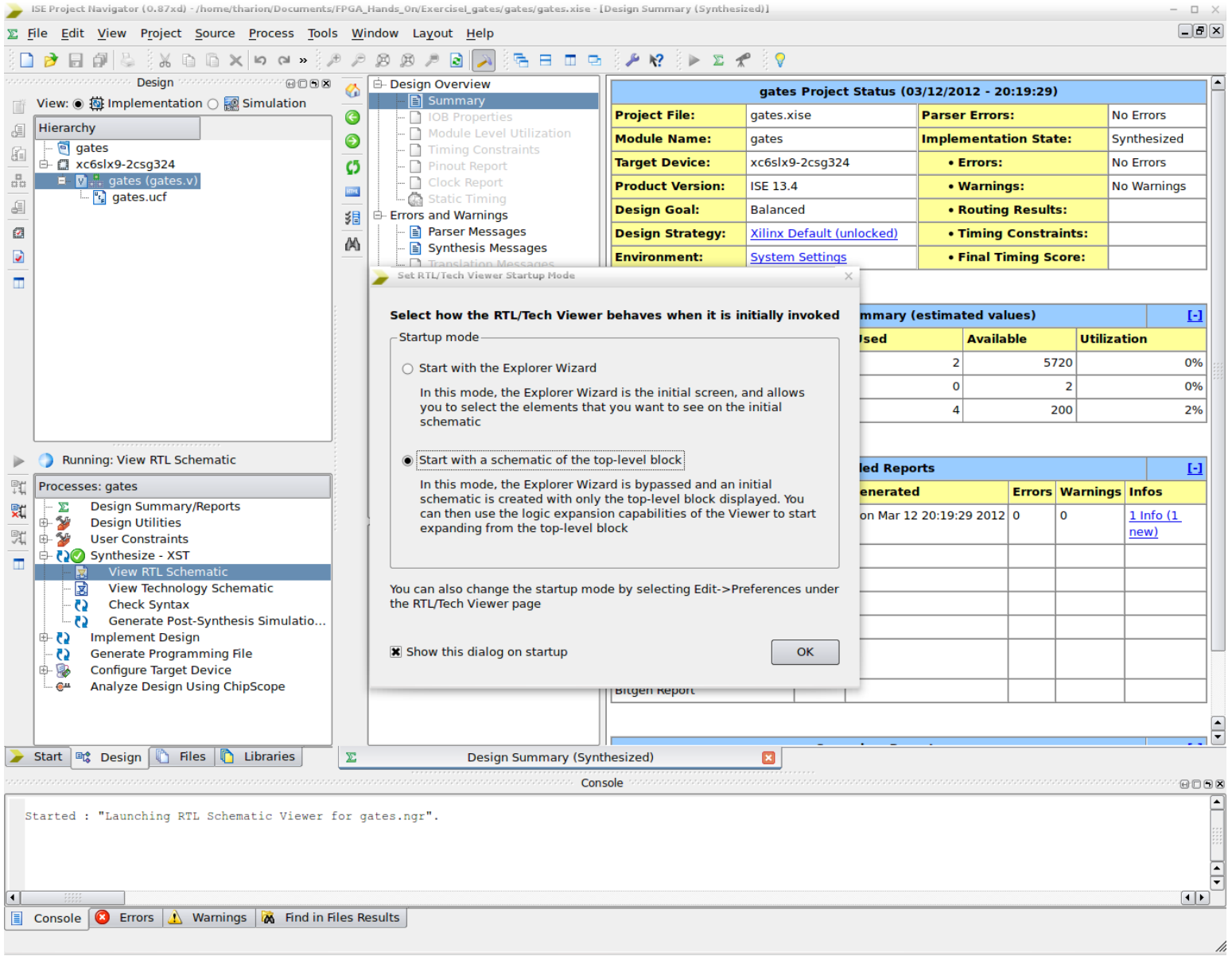
The design files are now present in the hierarchy viewer

Step 4: Synthesizing the Design



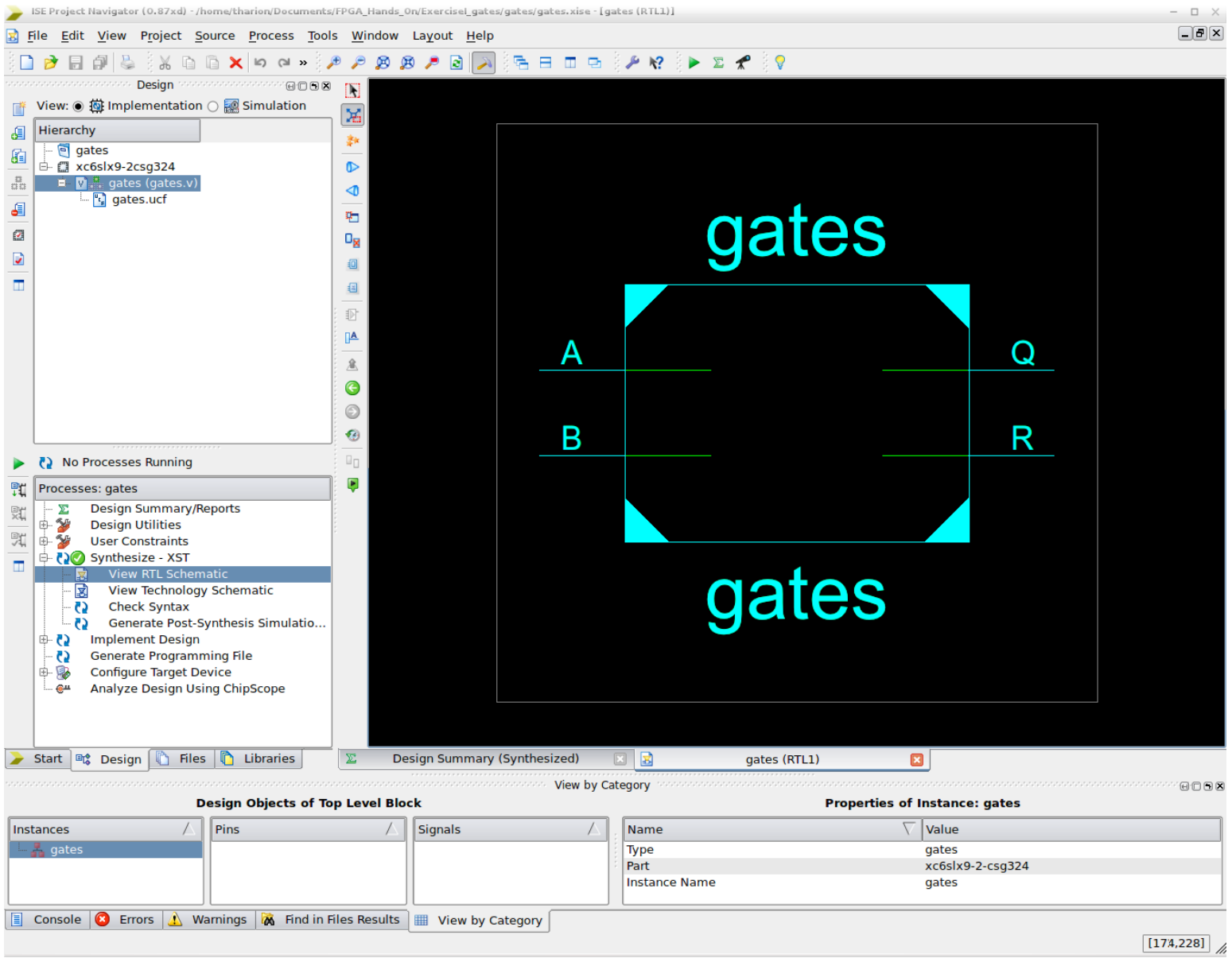
Select the module "gates" and double-click "Synthesize" in the "Processes" area

Step 5: Using the RTL Viewer



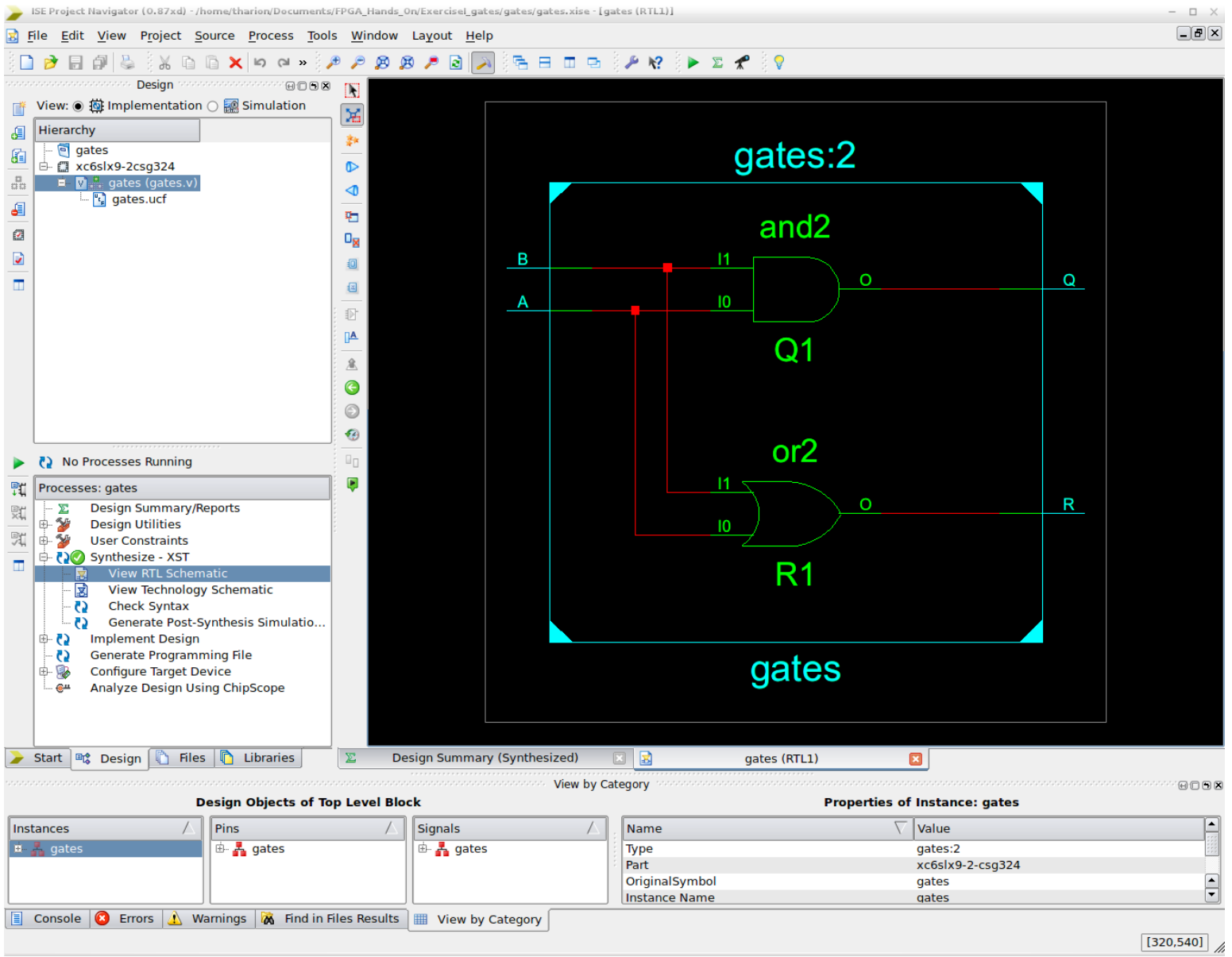
Select "View RTL Schematic" to launch the RTL Viewer, start with the top-level block

Step 5: Using the RTL Viewer



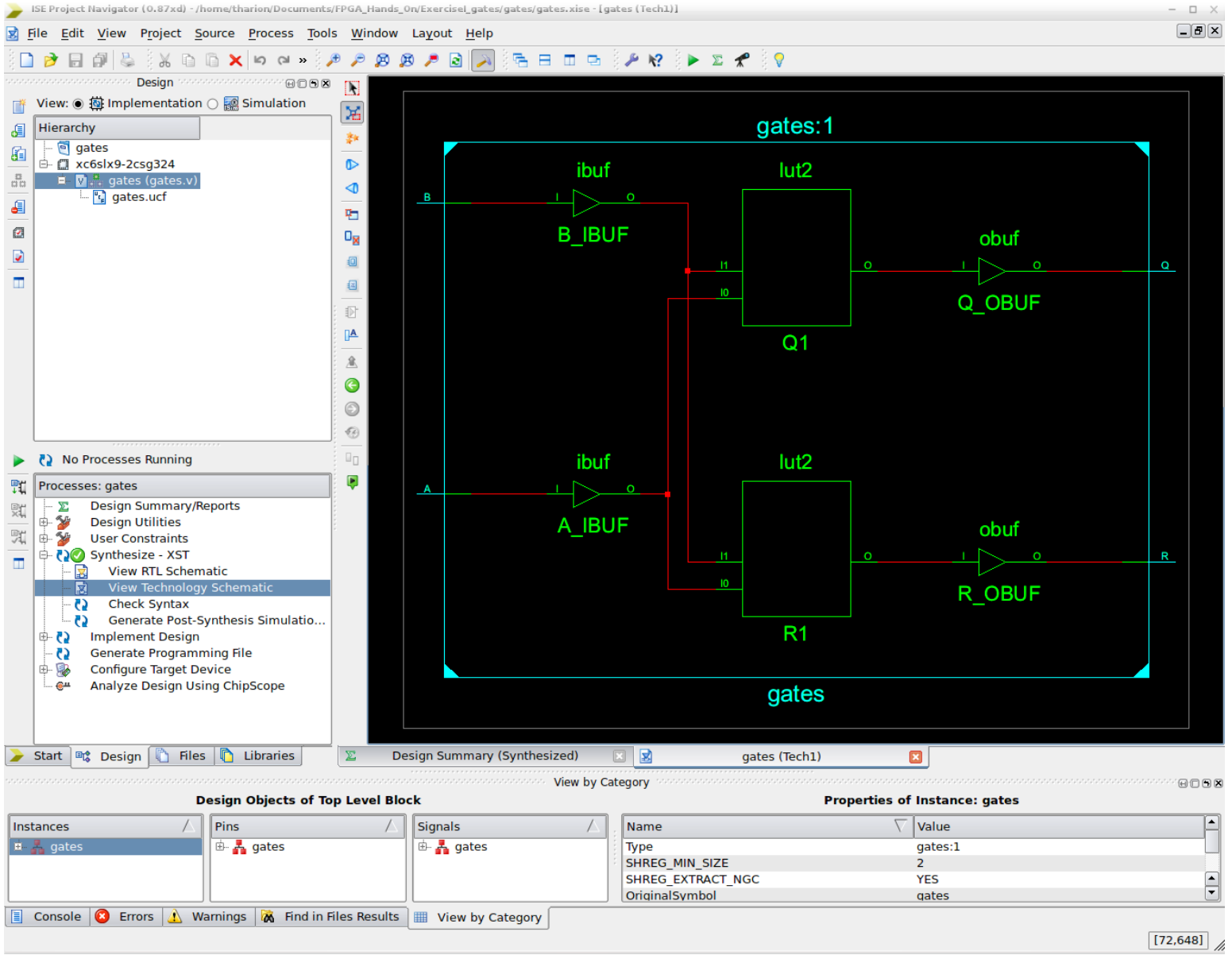
Double-click on the "gates" module to view the components of top-level block

Step 5: Using the RTL Viewer



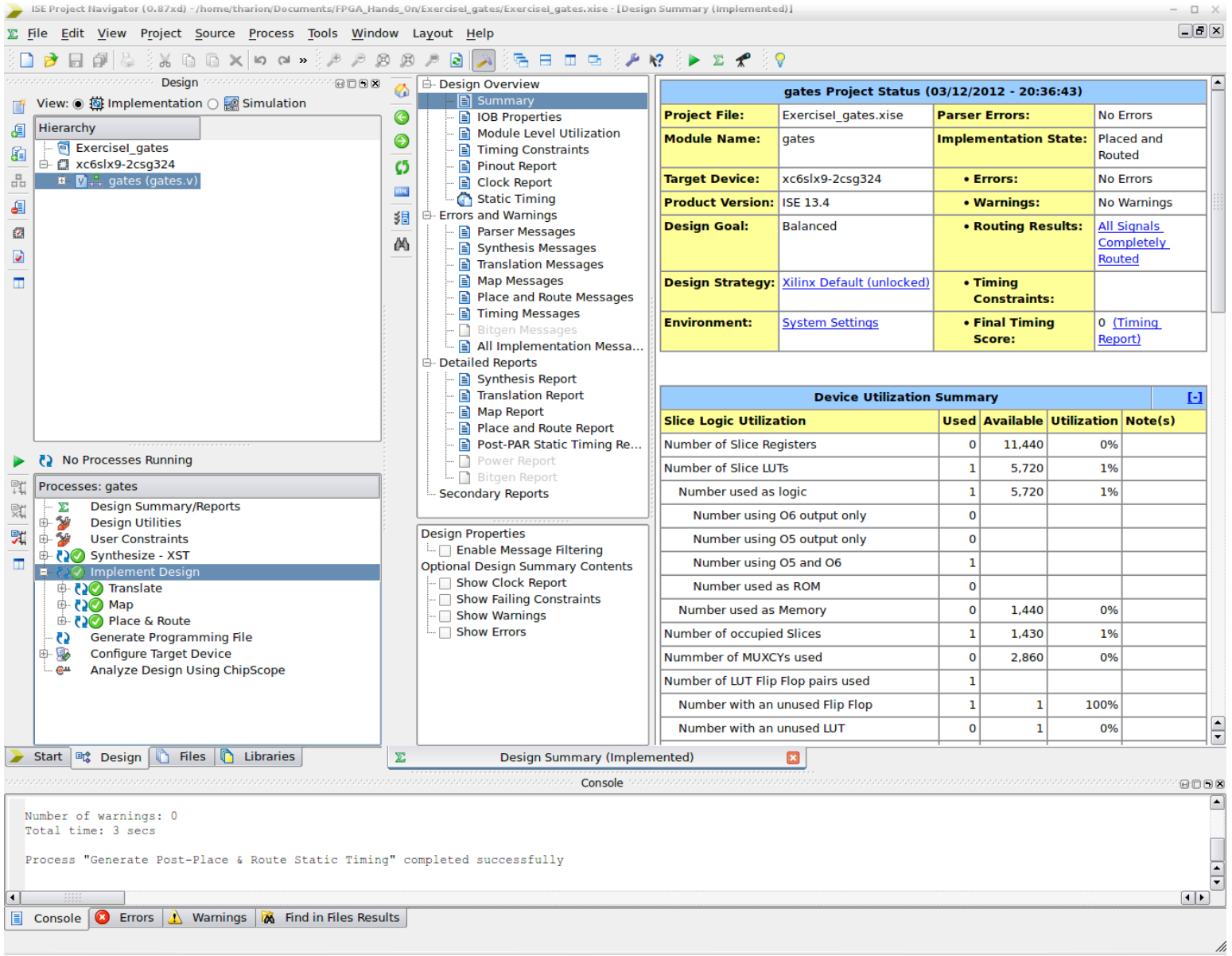
The viewer now shows a schematic view of the design

Step 6: Using the Technology Viewer



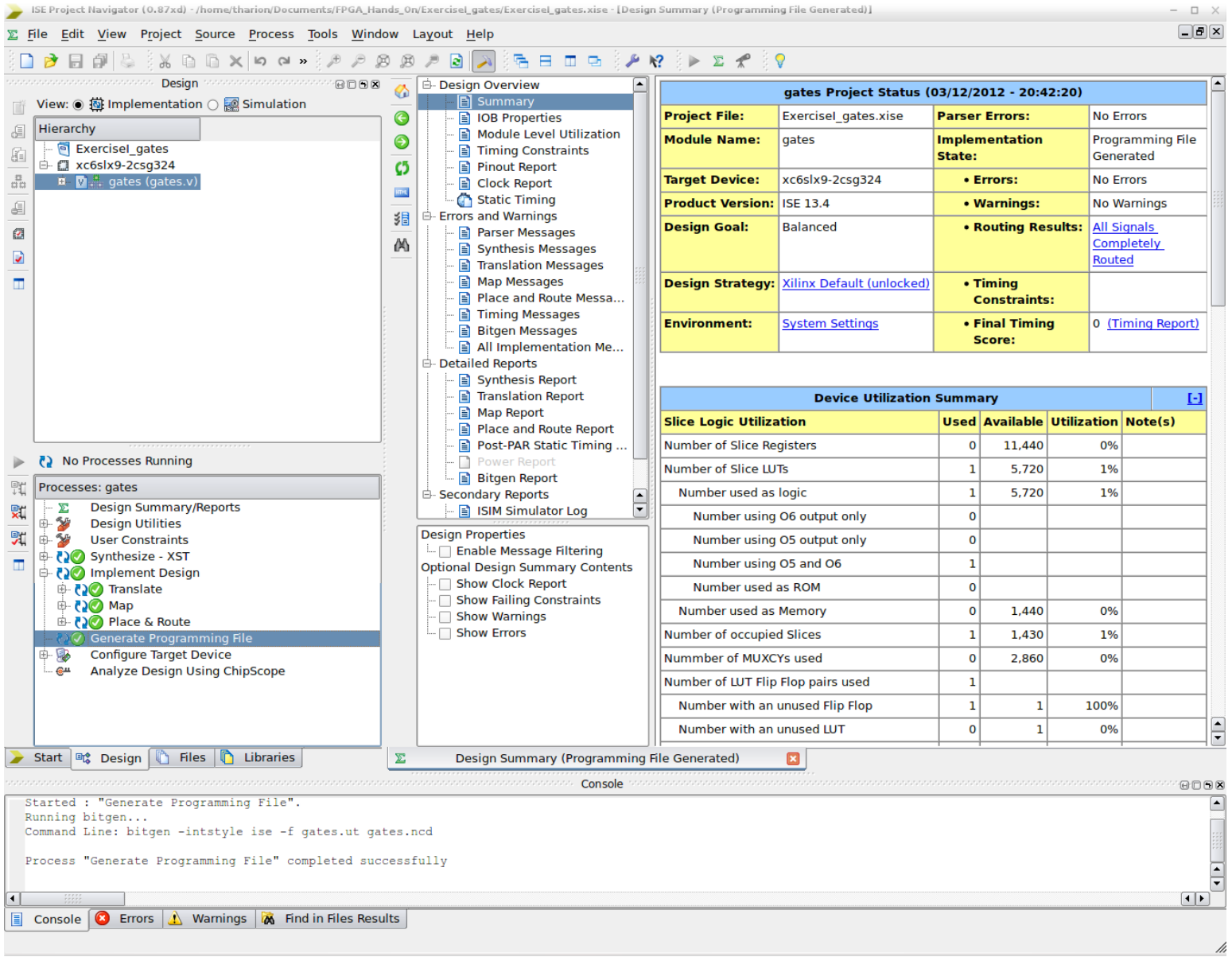
Similarly, the technology schematic can be inspected

Step 7: Implement the Design



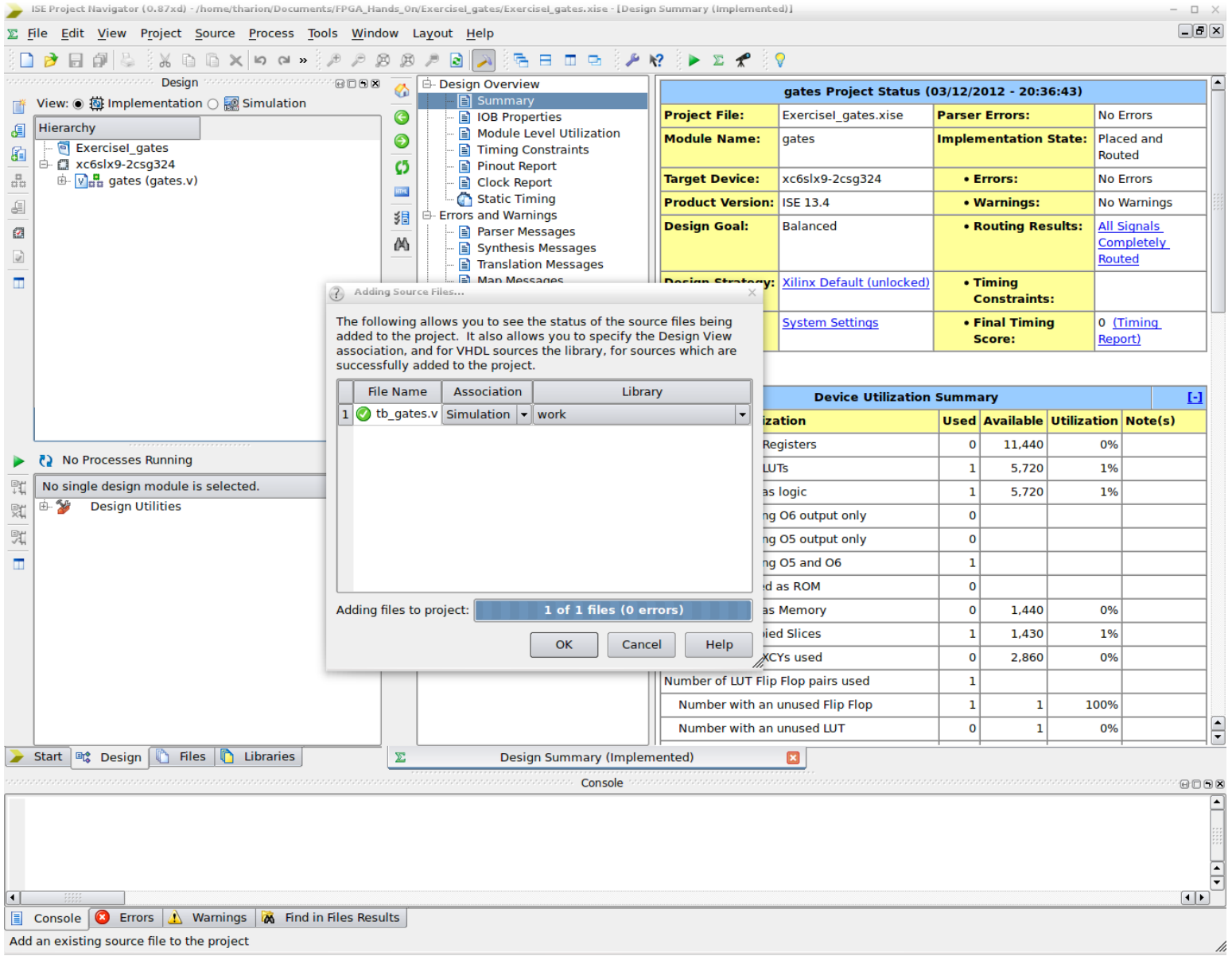
Translate, Map and Place and Route the design by selecting "Implement Design"

Step 8: Generate the Programming File



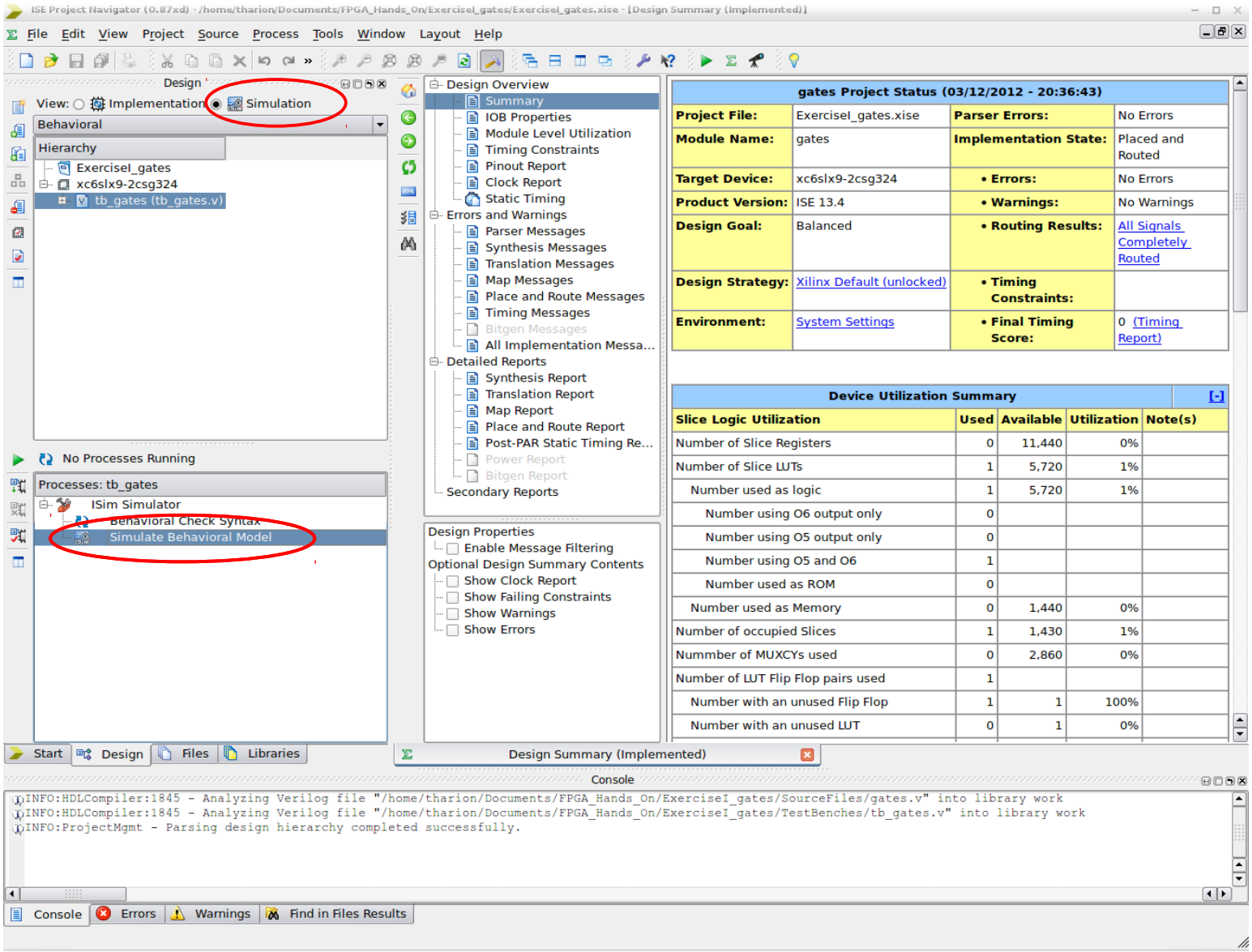
Generate the gates.bit file by selecting "Generate Programming File"

Step 9: Add a Testbench for Simulation



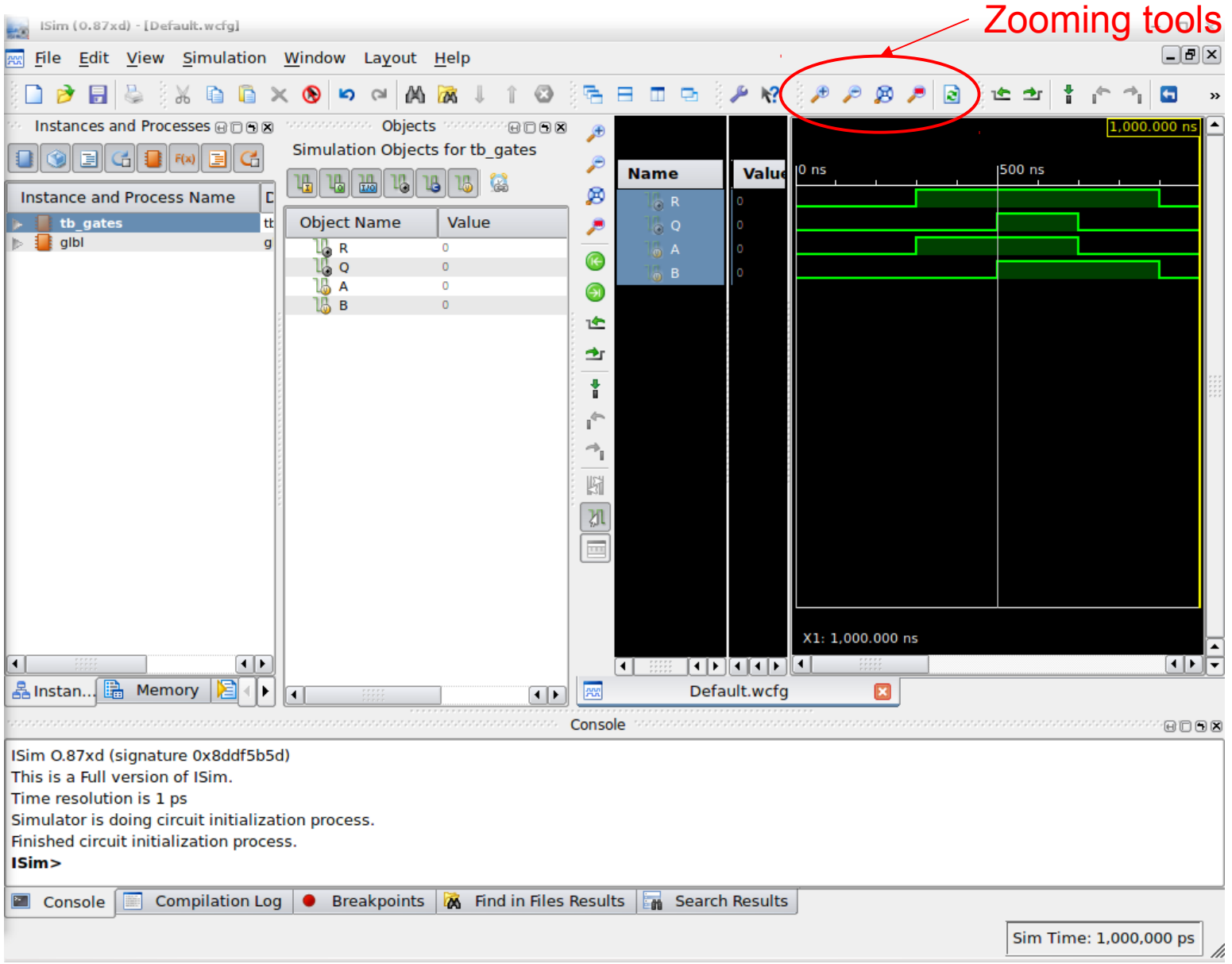
Add the tb_gates.v source as was done in Step 3. Choose Association: Simulation

Step 10: Perform a Behavorial Simulation



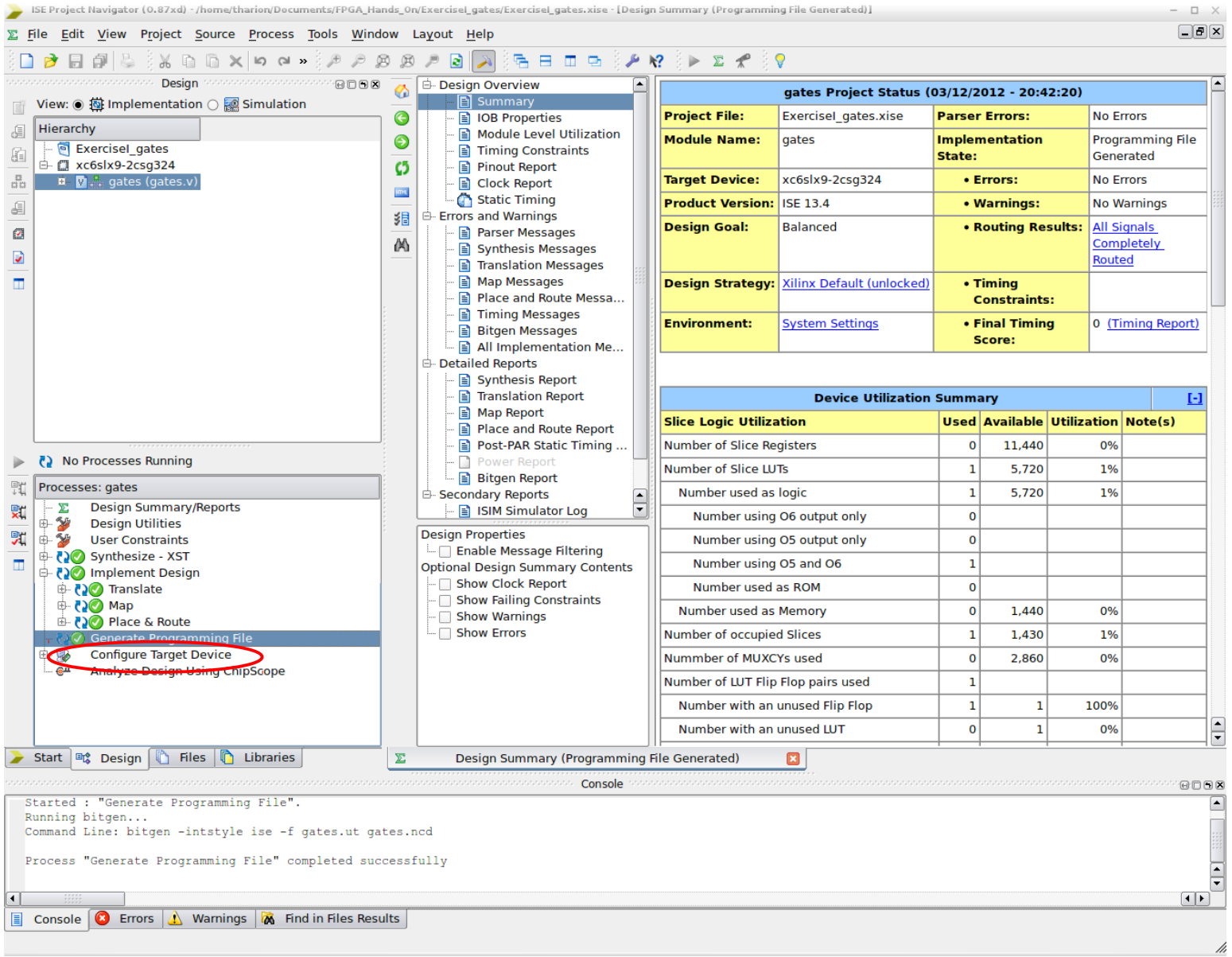
Change the Project View to Simulation. Select the tb_gates module and run "Simulate Behavorial Model"

Step 11: Check the Behavorial Simulation with ISim



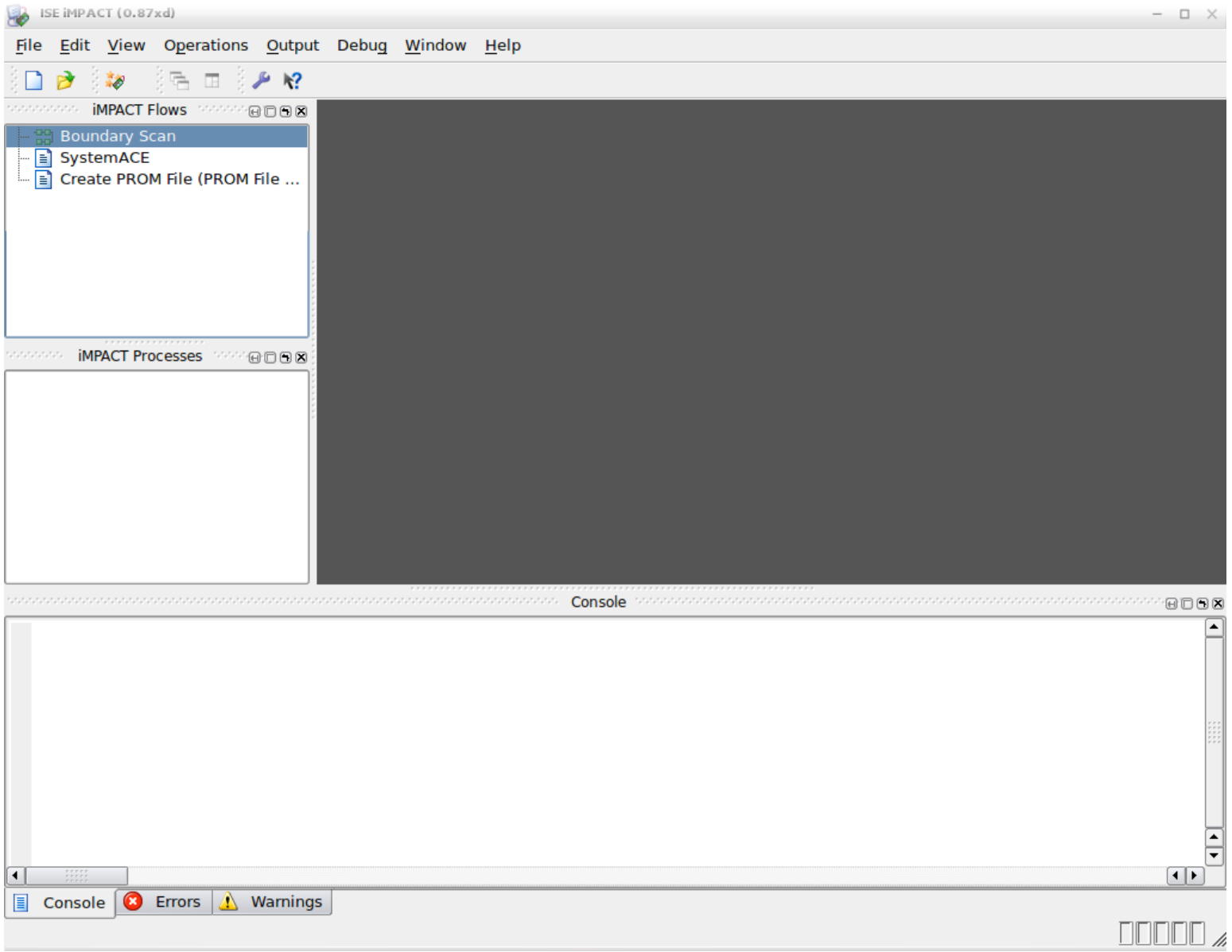
Use the ISim simulator to verify the expected behavior of the design

Step 12: Start iMPACT



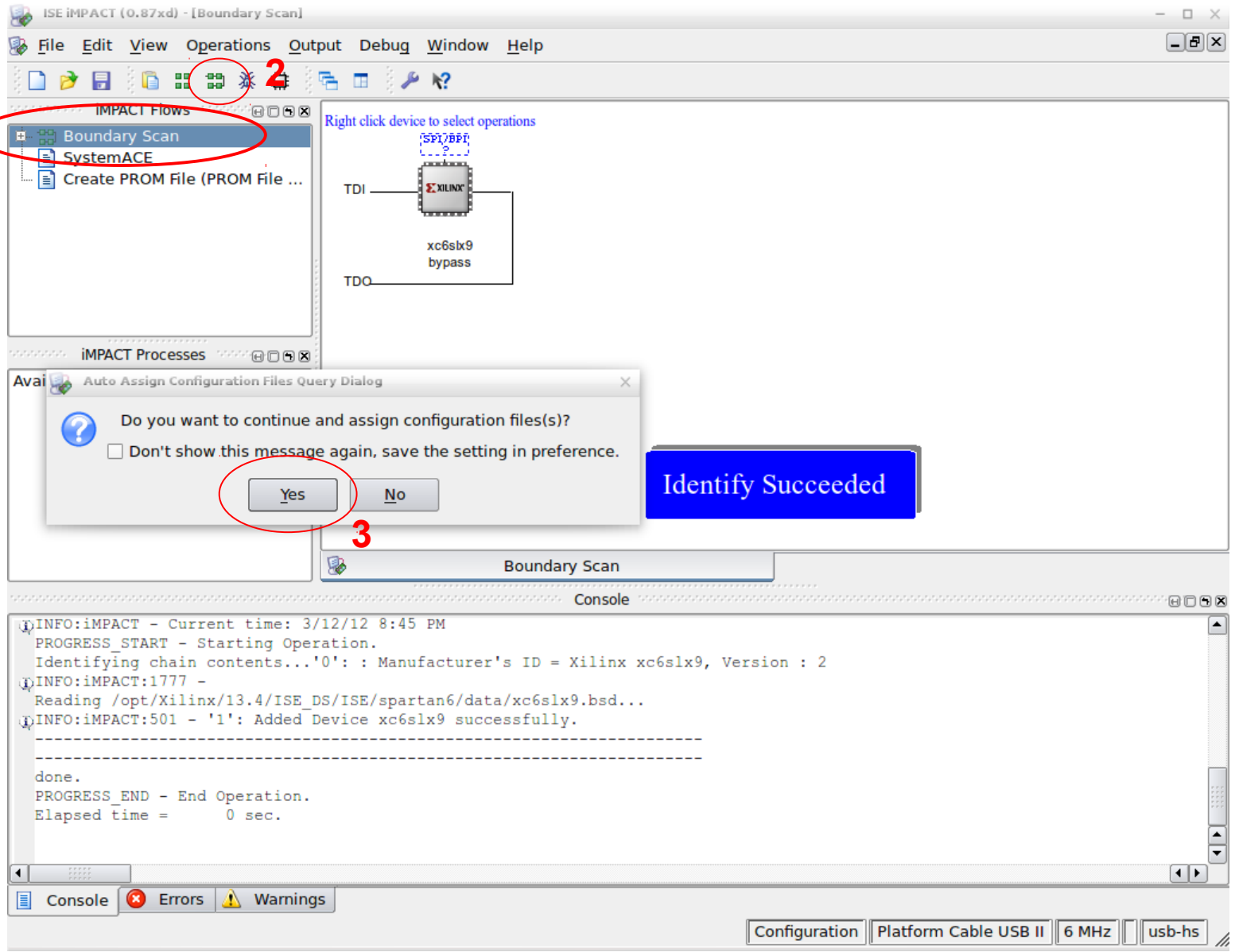
Start iMPACT by running "Configure Target Device"

Step 12: Start iMPACT



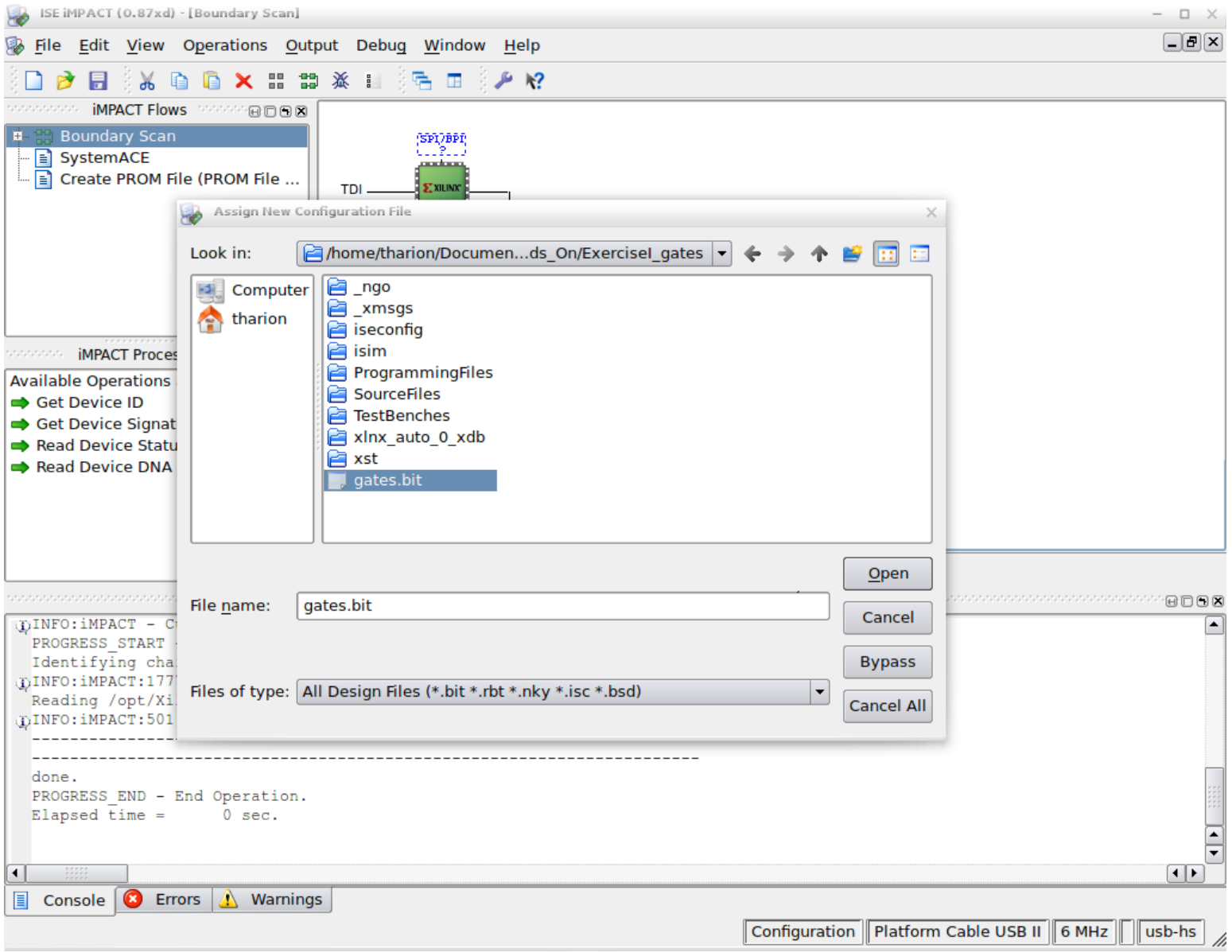
In the Implementation View chose "Configure Target Device" to start ISE iMPACT

Step 13: Initialize the JTAG Chain



Run "Boundary Scan". After completion click on the Initialize Chain button

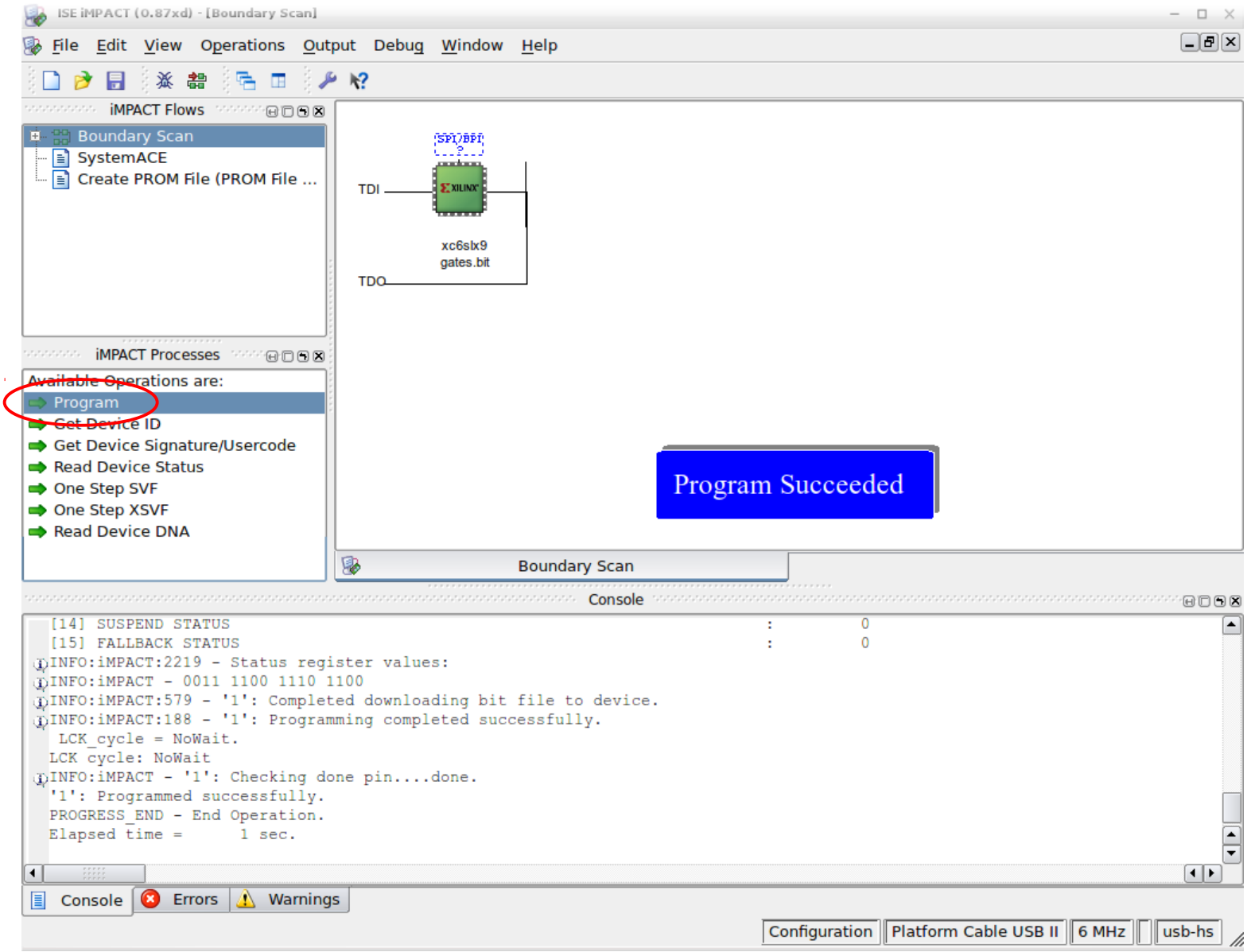
Step 14: Assign the Bitfile of the Design



ISE Introduction

the generated .bit file of the design which is located in the project di

Step 15: Program the FPGA



Under "iMPACT Processes" run "Program" to write the bit file to the FPGA