

Xilinx ISE

Introduction

First Steps with ISE

■ ISE Project Navigator

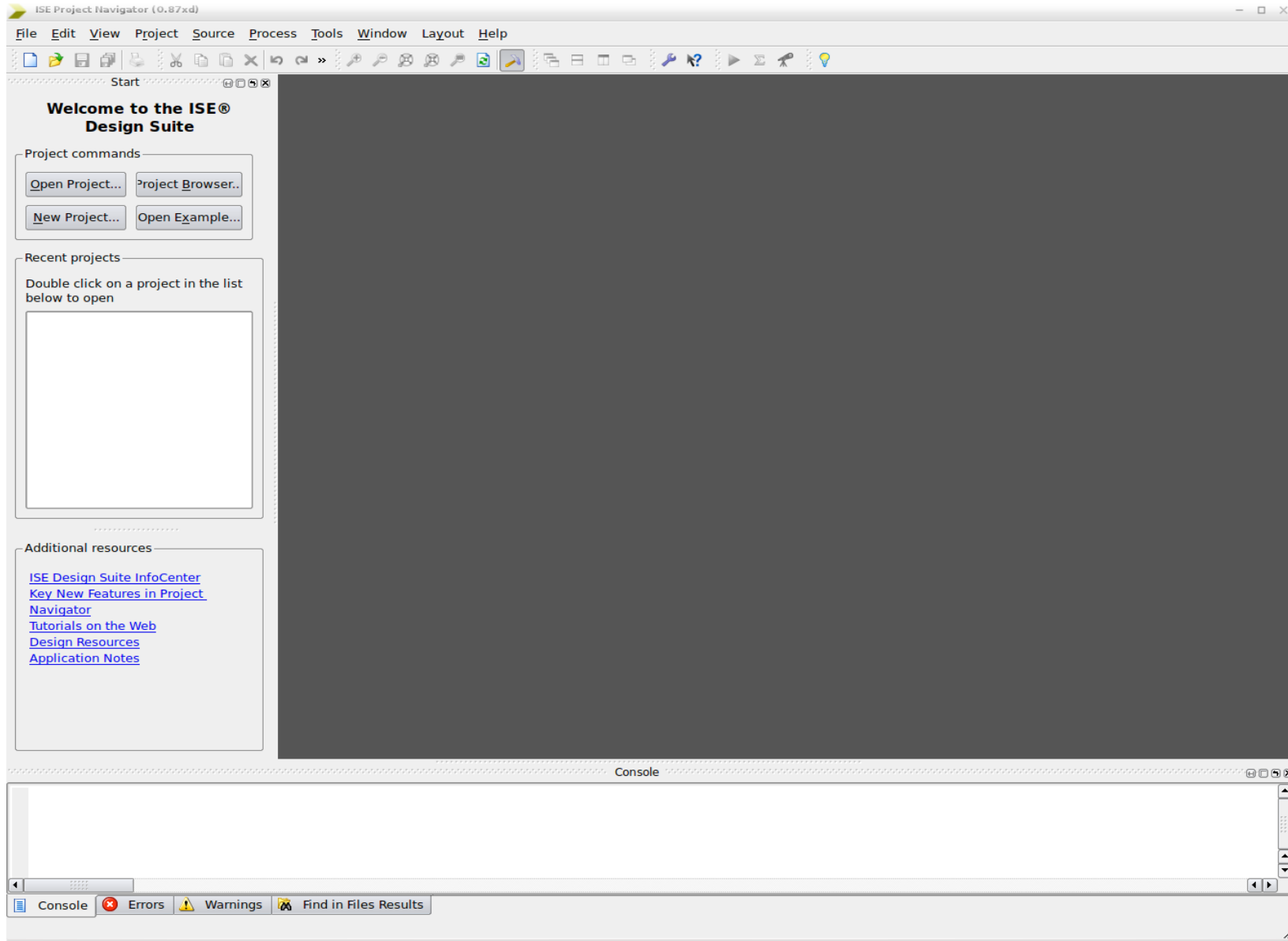
- Creating a new project
- Adding new design sources

■ Design Flow

- Synthesising the design
 - RTL Viewer
 - Technology Viewer
- Implementing the Design
 - Translate, Map, Place and Route
 - Generate Programming File

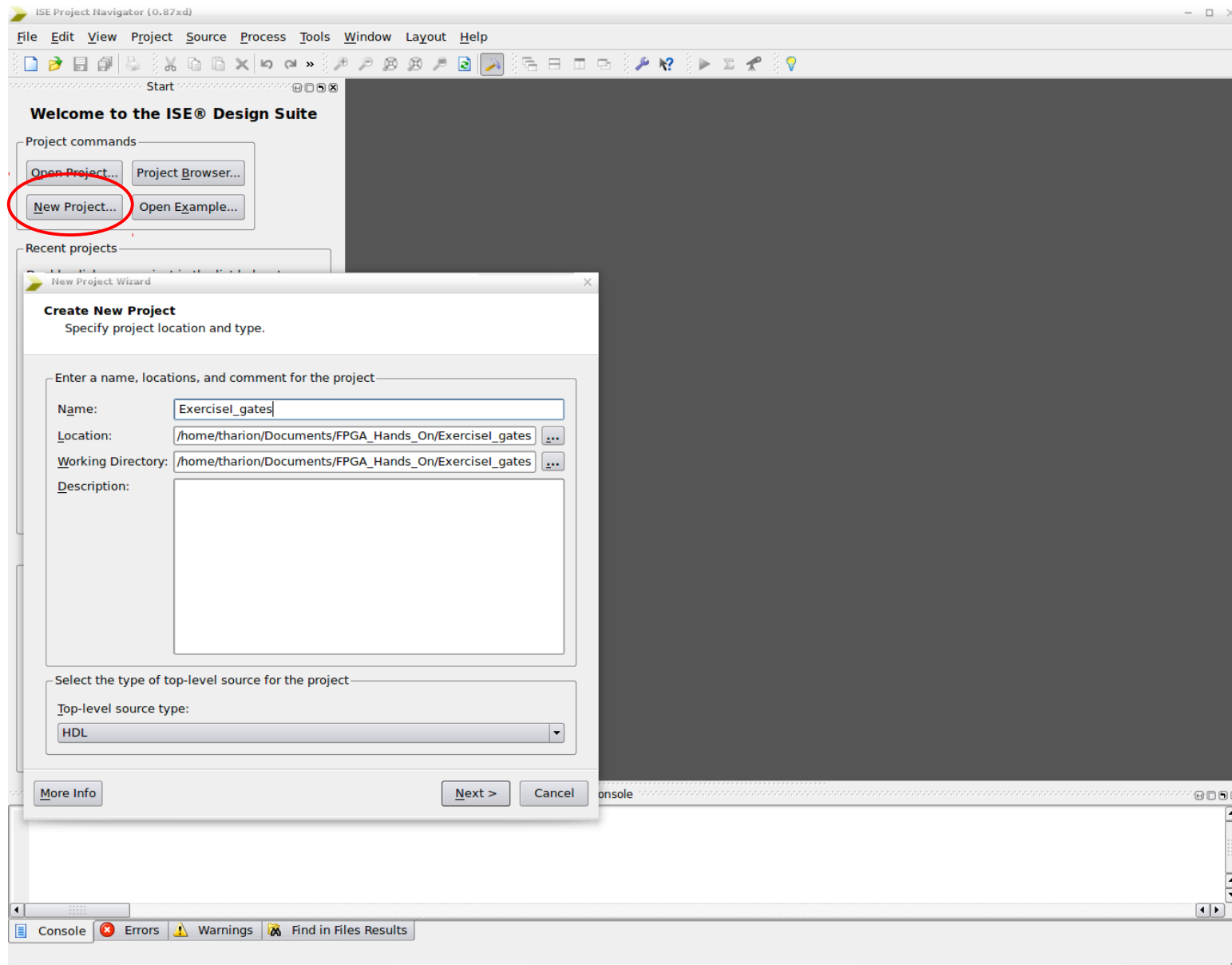
■ Programm the FPGA

Step1: Starting ISE



Start ISE by opening a terminal and running "xilinx" and "ise"

Step 2: Creating a new project



Create a new project using the "New Project" button

Step 2: Creating a new project

New Project Wizard

Project Settings
Specify device and project properties.

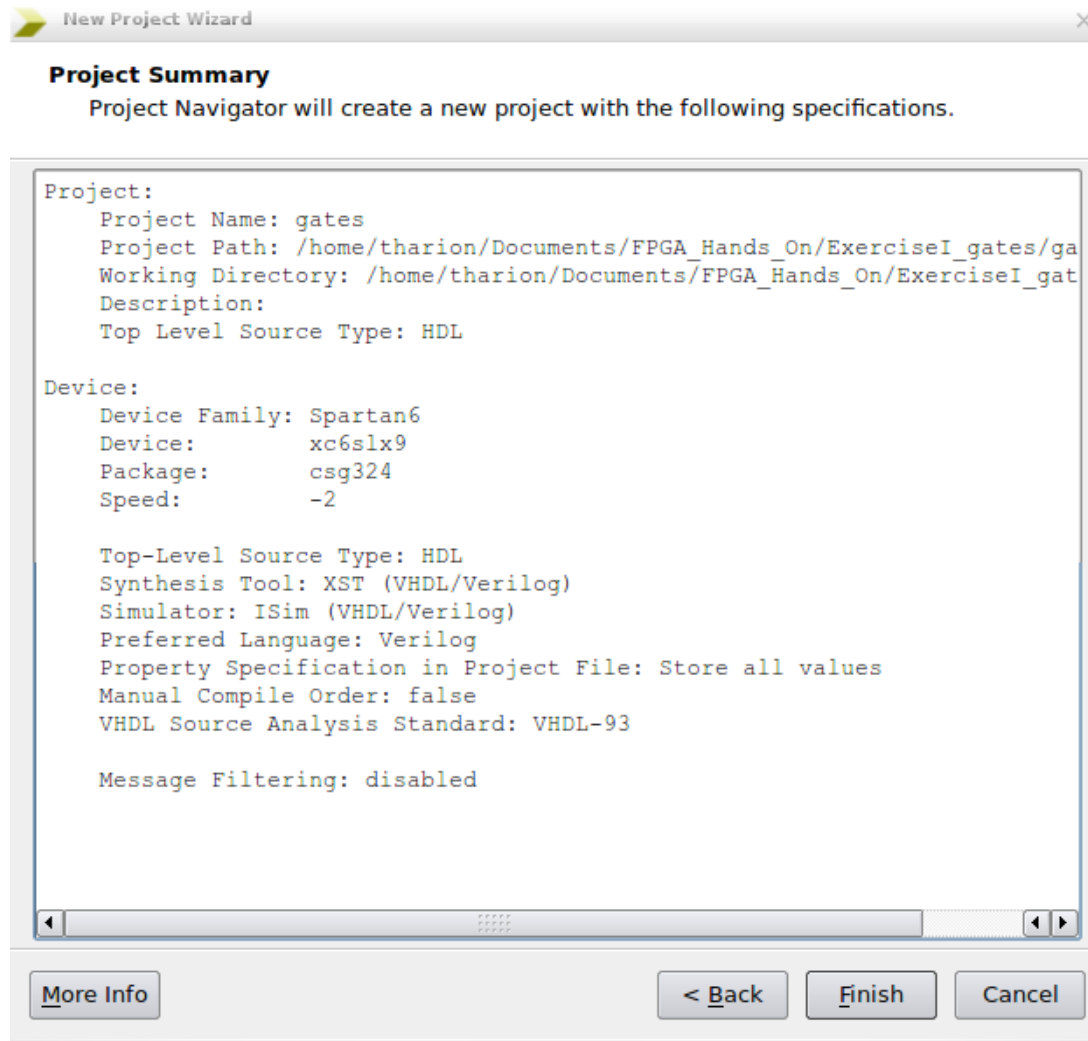
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan6
Device	XC6SLX9
Package	CSG324
Speed	-2
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93

[More Info](#) < Back Next > Cancel

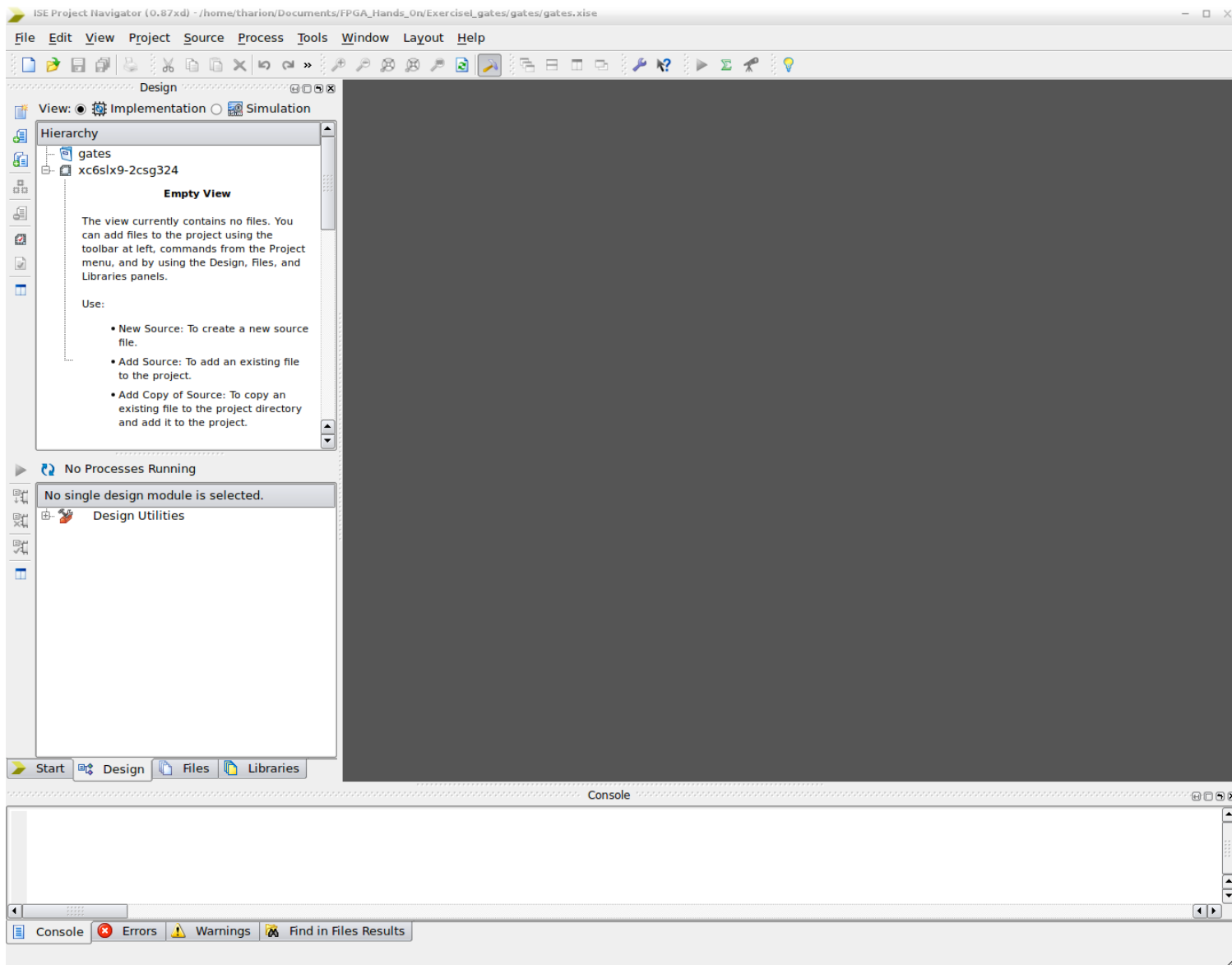
In the project settings choose the appropriate device family and package

Step 2: Creating a new project



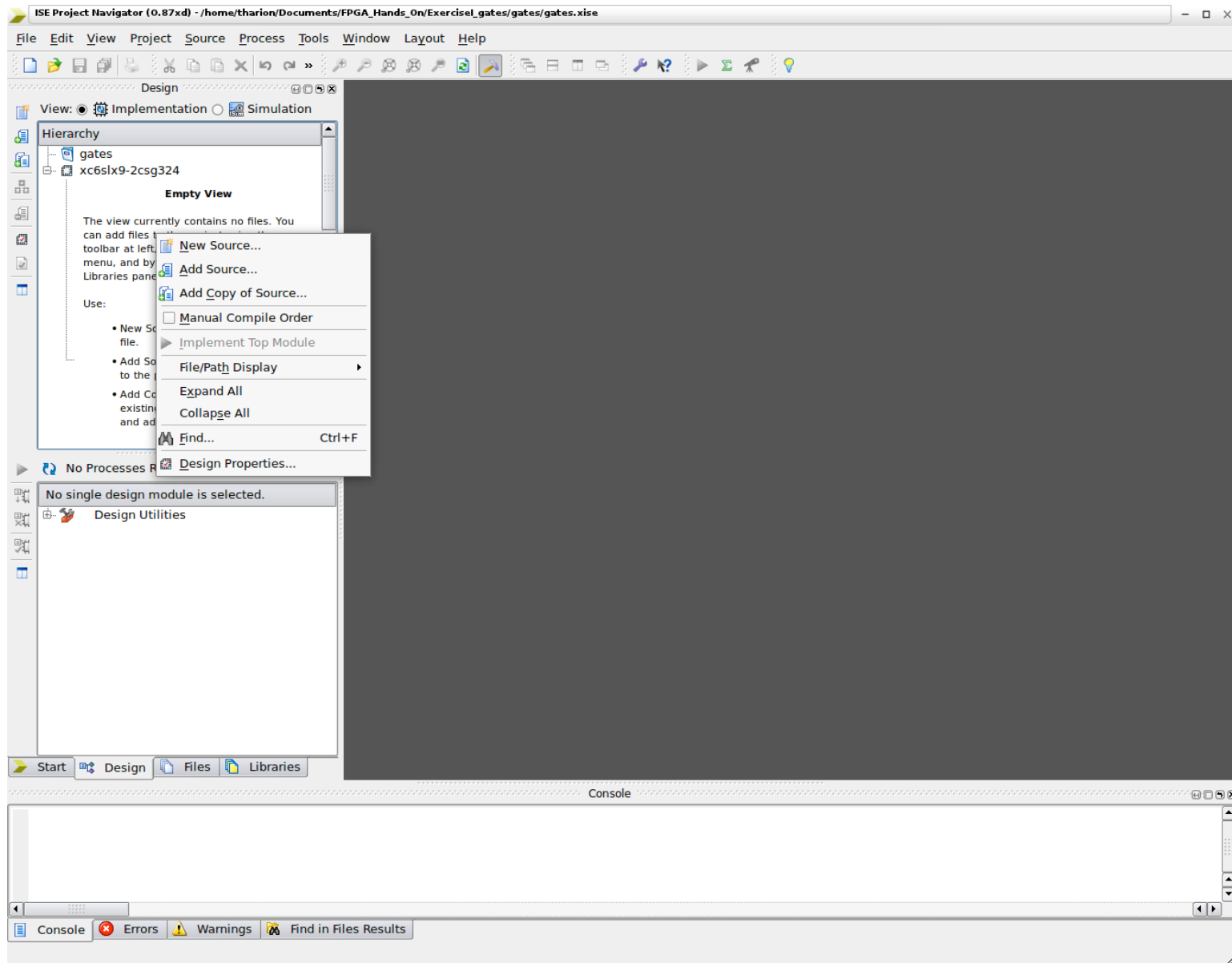
Click "Finish" to create the new project

Step 2: Creating a new project



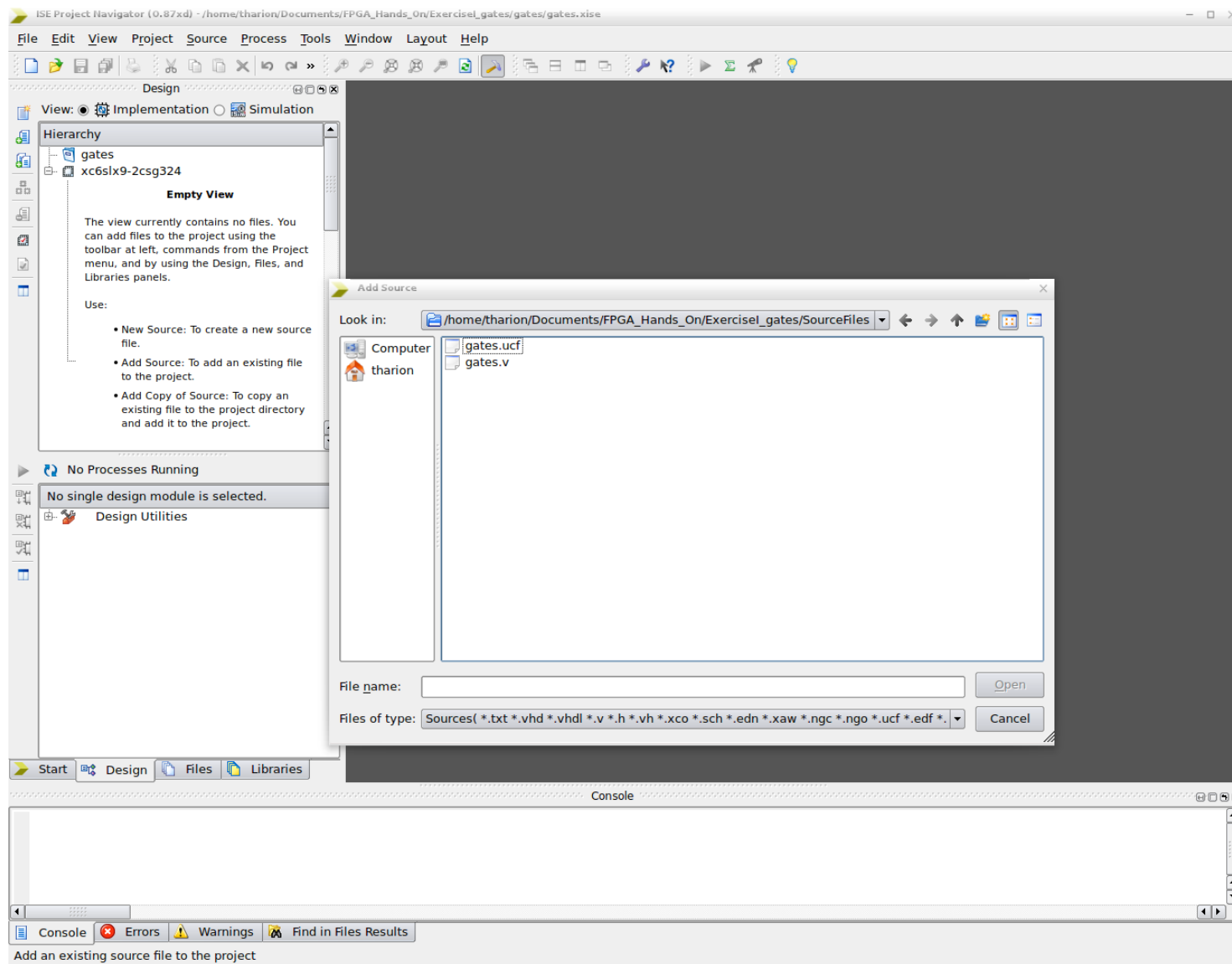
You have now created an empty project for the Spartan6-LX9 device

Step 3: Adding Design Sources



Right-click on the "Empty View" Area and choose "Add Source"

Step 3: Adding Design Sources



Browse to the source folder and select the files "gates.v" and "gates.ucf" containing the design and the constraints for the current project

Step 3: Adding Design Sources

The screenshot displays the Xilinx ISE Project Navigator interface. The 'Design Summary' window is open, showing the project status and a list of reports. The 'Hierarchy' viewer on the left shows the project structure: 'gates' containing 'xc6slx9-2csg324', which contains 'gates (gates.v)' and 'gates.ucf'. The 'Design Overview' pane shows a tree of reports including Summary, IOB Properties, Module Level Utilization, Timing Constraints, Pinout Report, Clock Report, Static Timing, Errors and Warnings, Parser Messages, Synthesis Messages, Translation Messages, Map Messages, Place and Route Messages, Timing Messages, Bitgen Messages, and All Implementation Messages. The 'Design Properties' pane shows options for message filtering and optional summary contents. The 'Design Summary' window displays a 'gates Project Status' table, a 'Detailed Reports' table, and a 'Secondary Reports' table. The Console window at the bottom shows log messages from the HDLCompiler and ProjectMgmt.

Property	Value	Property	Value
Project File:	gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	New
Target Device:	xc6slx9-2csg324	Errors:	
Product Version:	ISE 13.4	Warnings:	
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:		Final Timing Score:	

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Report Name	Status	Generated

Date Generated: 03/12/2012 - 20:17:00

```

INFO:HDLCompiler:1845 - Analyzing Verilog file "/home/tharion/Documents/FPGA_Hands_On/ExerciseI_gates/SourceFiles/gates.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
    
```

The design files are now present in the hierarchy viewer

Step 4: Synthesizing the Design

The screenshot shows the Xilinx ISE Project Navigator interface. The 'Design Overview' pane on the right displays the synthesis results for the 'gates' project. The 'gates Project Status' table indicates that the design was synthesized successfully with no errors or warnings. The 'Device Utilization Summary' table shows that 2 LUTs and 4 IOBs are used out of 5720 LUTs and 200 IOBs available. The 'Detailed Reports' table lists the 'Synthesis Report' as the current report, generated on March 12, 2012, at 20:19:29.

gates Project Status (03/12/2012 - 20:19:29)			
Project File:	gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Synthesized
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2	5720	0%
Number of fully used LUT-FF pairs	0	2	0%
Number of bonded IOBs	4	200	2%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Mon Mar 12 20:19:29 2012	0	0	1 Info (1 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

The 'Processes' pane on the left shows the 'Synthesize - XST' process as the current step. The console at the bottom displays the message: 'Process "Synthesize - XST" completed successfully'. The maximum combinational path delay is reported as 6.005ns.

Select the module "gates" and double-click "Synthesize" in the "Processes" area

Step 5: Using the RTL Viewer

The screenshot shows the ISE Project Navigator interface. The main window displays the Design Summary (Synthesized) for the 'gates' project. A dialog box titled 'Set RTL/Tech Viewer Startup Mode' is open, asking the user to select how the RTL/Tech Viewer behaves when initially invoked. The dialog has two options: 'Start with the Explorer Wizard' and 'Start with a schematic of the top-level block'. The second option is selected. There is also a checkbox for 'Show this dialog on startup' which is checked. The background window shows the Design Summary table and the Design Overview tree.

Property	Value	Property	Value
Project File:	gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Synthesized
Target Device:	xc6slx9-2csg324	• Errors:	No Errors
Product Version:	ISE 13.4	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Used	Available	Utilization
2	5720	0%
0	2	0%
4	200	2%

Generated	Errors	Warnings	Infos
on Mar 12 20:19:29 2012	0	0	1 Info (1 new)

ISE Introduction

Select "View RTL Schematic" to launch the RTL Viewer, start with the top-level block

Step 5: Using the RTL Viewer

The screenshot shows the ISE Project Navigator interface. The main window displays the RTL Viewer for a 'gates' module. The schematic shows two 'gates' blocks, each with inputs A and B, and outputs Q and R. The left pane shows the Hierarchy and Processes. The bottom pane shows Design Objects and Properties.

Design Objects of Top Level Block

Instances	Pins	Signals
gates		

Properties of Instance: gates

Name	Value
Type	gates
Part	xc6slx9-2-csg324
Instance Name	gates

Double-click on the "gates" module to view the components of top-level block

Step 5: Using the RTL Viewer

The screenshot displays the ISE Project Navigator interface. The main window shows the RTL Schematic view of a design. The schematic is titled 'gates:2' and contains two 2-input gates: an AND gate (Q1) and an OR gate (R1). The AND gate has inputs A and B, and output Q. The OR gate has inputs A and B, and output R. The design is titled 'gates:2' and 'gates'.

The left pane shows the Hierarchy view with the following structure:

- gates
- xc6slx9-2csg324
- gates (gates.v)
- gates.ucf

The bottom pane shows the Design Objects of Top Level Block and Properties of Instance: gates.

Design Objects of Top Level Block	
Instances	gates
Pins	gates
Signals	gates

Properties of Instance: gates	
Name	gates:2
Type	gates:2
Part	xc6slx9-2-csg324
OriginalSymbol	gates
Instance Name	gates

The viewer now shows a schematic view of the design

Step 6: Using the Technology Viewer

The screenshot displays the ISE Project Navigator interface. The main window shows the Technology Schematic for the 'gates' block. The schematic includes two LUT2 blocks (Q1 and R1), two input buffers (B_IBUF and A_IBUF), and two output buffers (Q_OBUF and R_OBUF). The inputs are labeled B and A, and the outputs are labeled Q and R. The schematic is enclosed in a cyan border with the label 'gates:1' at the top and 'gates' at the bottom.

The left sidebar shows the Hierarchy tree with 'gates (gates.v)' selected. Below it, the 'Processes: gates' list includes 'View Technology Schematic' which is highlighted. The bottom of the window shows the 'Design Objects of Top Level Block' and 'Properties of Instance: gates' panels.

Design Objects of Top Level Block		
Instances	Pins	Signals
gates	gates	gates

Properties of Instance: gates	
Name	Value
Type	gates:1
SHREG_MIN_SIZE	2
SHREG_EXTRACT_NGC	YES
OriginalSymbol	gates

Similarly, the technology schematic can be inspected

Step 7: Implement the Design

The screenshot shows the Xilinx ISE Project Navigator interface. The main window is titled "Design Summary (Implemented)" and displays the following information:

gates Project Status (03/12/2012 - 20:36:43)

Project File:	Exercisel_gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Placed and Routed
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	11,440	0%	
Number of Slice LUTs	1	5,720	1%	
Number used as logic	1	5,720	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number of occupied Slices	1	1,430	1%	
Number of MUXCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	

Console

```
Number of warnings: 0
Total time: 3 secs

Process "Generate Post-Place & Route Static Timing" completed successfully
```

Translate, Map and Place and Route the design by selecting "Implement Design"

Step 8: Generate the Programming File

The screenshot displays the ISE Project Navigator interface. The Design Overview pane shows the 'Design Summary' report selected. The Console pane shows the following output:

```
Started : "Generate Programming File".
Running bitgen...
Command Line: bitgen -intstyle ise -f gates.ut gates.ncd
Process "Generate Programming File" completed successfully
```

The Design Summary report is displayed in the right pane, showing the following information:

gates Project Status (03/12/2012 - 20:42:20)			
Project File:	Exercisel_gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Programming File Generated
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	11,440	0%	
Number of Slice LUTs	1	5,720	1%	
Number used as logic	1	5,720	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number of occupied Slices	1	1,430	1%	
Number of MUXCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	

Generate the gates.bit file by selecting "Generate Programming File"

Step 9: Add a Testbench for Simulation

The screenshot shows the ISE Project Navigator interface. A dialog box titled 'Adding Source Files...' is open in the center. It contains a table with the following data:

File Name	Association	Library
1 ✓ tb_gates.v	Simulation	work

Below the table, it says 'Adding files to project: 1 of 1 files (0 errors)'. The background shows the 'Design Summary' window with the following data:

gates Project Status (03/12/2012 - 20:36:43)			
Project File:	Exercisel_gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Placed and Routed
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
System Settings		Final Timing Score:	0 (Timing Report)

Below this is the 'Device Utilization Summary' table:

Utilization	Used	Available	Utilization	Note(s)
Registers	0	11,440	0%	
LUTs	1	5,720	1%	
as logic	1	5,720	1%	
ng O6 output only	0			
ng O5 output only	0			
ng O5 and O6	1			
ed as ROM	0			
as Memory	0	1,440	0%	
ried Slices	1	1,430	1%	
MCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	

Add the tb_gates.v source as was done in Step 3. Choose Association: Simulation

Step 10: Perform a Behavioral Simulation

The screenshot shows the ISE Project Navigator interface. The 'View' dropdown is set to 'Simulation'. The 'Design Overview' pane shows a tree of reports, with 'Simulation' selected. The 'Processes: tb_gates' pane shows the 'Simulate Behavioral Model' button highlighted with a red circle. The 'Design Summary (Implemented)' pane shows the project status, including the target device (xc6slx9-2csg324) and implementation state (Placed and Routed). The 'Device Utilization Summary' table is also visible.

gates Project Status (03/12/2012 - 20:36:43)			
Project File:	Exercisel_gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Placed and Routed
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	11,440	0%	
Number of Slice LUTs	1	5,720	1%	
Number used as logic	1	5,720	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number of occupied Slices	1	1,430	1%	
Number of MUXCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	

Change the Project View to Simulation. Select the tb_gates module and run "Simulate Behavioral Model"

Step 11: Check the Behavioral Simulation with ISim

The screenshot shows the ISim (0.87xd) interface. The main window displays a timing diagram for simulation objects R, Q, A, and B. The signals are shown as green traces on a black background. The time axis ranges from 0 ns to 1,000,000 ns. A red circle highlights the zooming tools in the toolbar, with an arrow pointing to them and the text "Zooming tools".

The console window shows the following text:

```
ISim 0.87xd (signature 0x8ddf5b5d)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

The status bar at the bottom right indicates "Sim Time: 1,000,000 ps".

Use the ISim simulator to verify the expected behavior of the design

Step 12: Start iMPACT

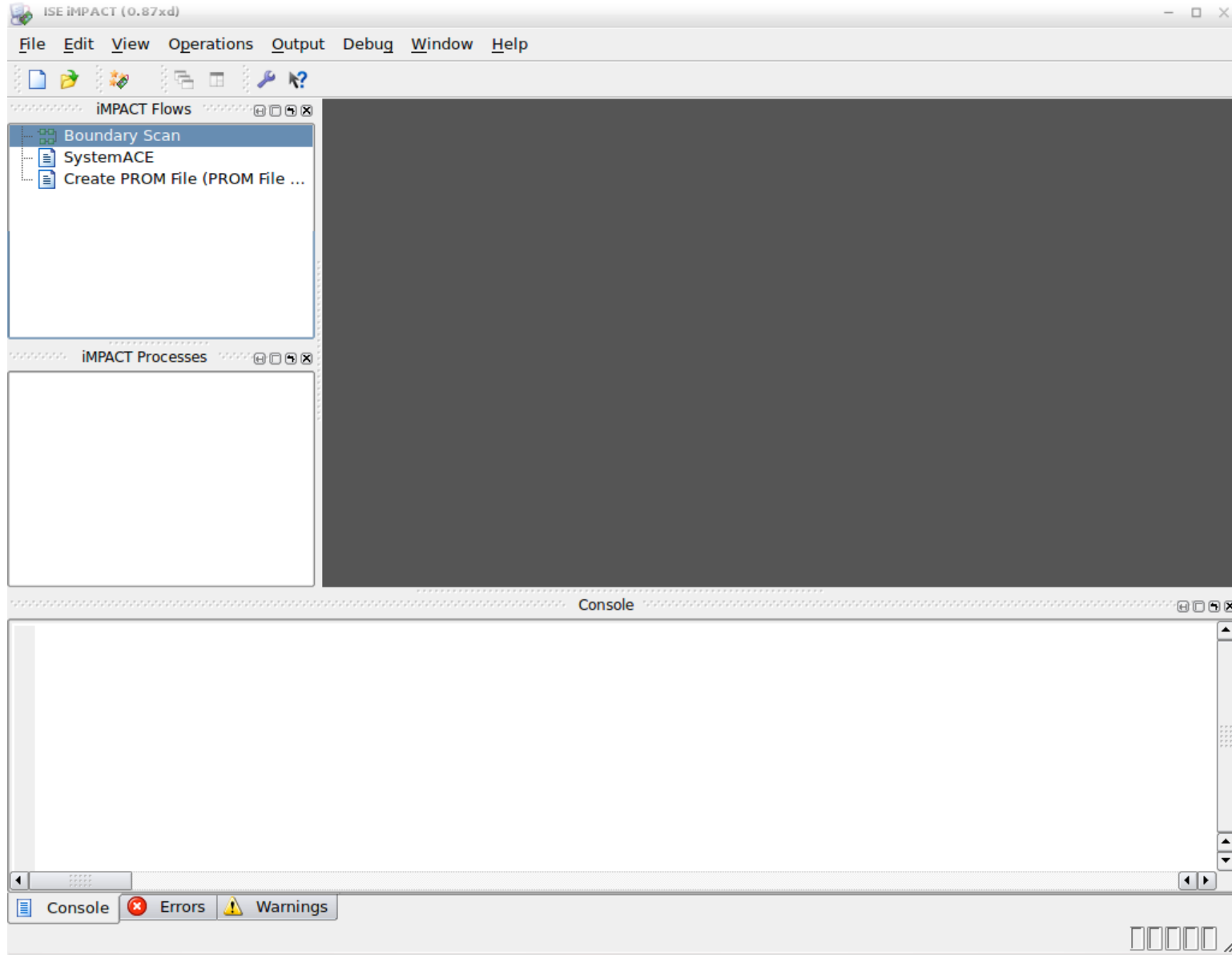
The screenshot shows the ISE Project Navigator interface. The 'Processes: gates' pane on the left has 'Configure Target Device' selected and circled in red. The 'Design Overview' pane on the right shows a tree view of reports, with 'Design Properties' expanded to show 'Optional Design Summary Contents' options like 'Show Clock Report' and 'Show Errors'. The 'Console' pane at the bottom shows the command line: `bitgen -intstyle ise -f gates.ut gates.ncd` and the message 'Process "Generate Programming File" completed successfully'. The 'gates Project Status' table on the right provides a summary of the project configuration.

gates Project Status (03/12/2012 - 20:42:20)			
Project File:	Exercisel_gates.xise	Parser Errors:	No Errors
Module Name:	gates	Implementation State:	Programming File Generated
Target Device:	xc6slx9-2csg324	Errors:	No Errors
Product Version:	ISE 13.4	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	11,440	0%	
Number of Slice LUTs	1	5,720	1%	
Number used as logic	1	5,720	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number of occupied Slices	1	1,430	1%	
Number of MUXCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	

Start iMPACT by running "Configure Target Device"

Step 12: Start iMPACT



In the Implementation View chose "Configure Target Device" to start ISE iMPACT

Step 13: Initialize the JTAG Chain

ISE iMPACT (0.87xd) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

IMPACT Flows

- Boundary Scan (1)
- SystemACE
- Create PROM File (PROM File ...)

Right click device to select operations

TDI

XILINX

xc6slx9 bypass

TDO

IMPACT Processes

Auto Assign Configuration Files Query Dialog

Do you want to continue and assign configuration file(s)?

Don't show this message again, save the setting in preference.

Yes (3) No

Identify Succeeded

Boundary Scan

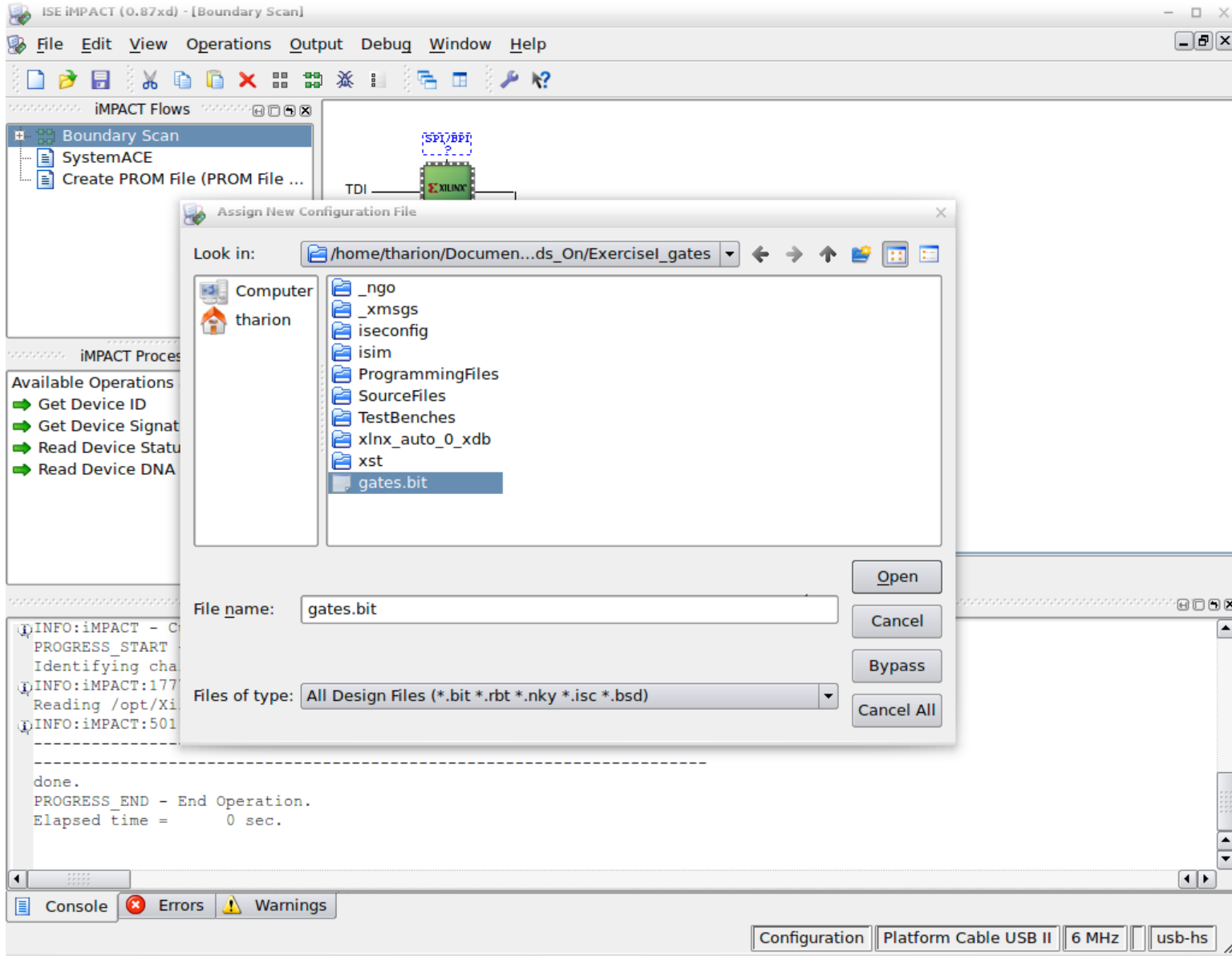
Console

```
INFO:iMPACT - Current time: 3/12/12 8:45 PM
PROGRESS_START - Starting Operation.
Identifying chain contents...'0': : Manufacturer's ID = Xilinx xc6slx9, Version : 2
INFO:iMPACT:1777 -
Reading /opt/Xilinx/13.4/ISE_DS/ISE/spartan6/data/xc6slx9.bsd...
INFO:iMPACT:501 - '1': Added Device xc6slx9 successfully.
-----
done.
PROGRESS_END - End Operation.
Elapsed time = 0 sec.
```

Configuration Platform Cable USB II 6 MHz usb-hs

Run "Boundary Scan". After completion click on the Initialize Chain button

Step 14: Assign the Bitfile of the Design



the generated .bit file of the design which is located in the project dir

Step 15: Program the FPGA

The screenshot shows the ISE iMPACT (0.87xd) - [Boundary Scan] interface. The 'iMPACT Processes' panel on the left lists available operations, with 'Program' highlighted and circled in red. The main workspace displays a diagram of an 'xc6s1x9 gates.bit' device connected to TDI and TDO. A blue box with the text 'Program Succeeded' is overlaid on the diagram. The console window at the bottom shows the output of the programming process, including status messages and a successful completion message.

```
[14] SUSPEND STATUS : 0
[15] FALLBACK STATUS : 0
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1100 1110 1100
INFO:iMPACT:579 - '1': Completed downloading bit file to device.
INFO:iMPACT:188 - '1': Programming completed successfully.
LCK_cycle = NoWait.
LCK_cycle: NoWait
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time = 1 sec.
```

Under "iMPACT Processes" run "Program" to write the bit file to the FPGA