Contribution ID: **26** Type: **not specified**

Lab Exercise (ISE design flow)

Wednesday 14 March 2012 11:10 (1h 20m)

Introduction to Xilinx Design Tools, Design of
digital modules with Verilog, e.g. simple logical unit, shift registers
edge detection, up/down counter, clock dividers, multiplexers etc.

Presenter: ANDREI, Victor (University of Heidelberg)

Session Classification: FPGA School