3D Integration
& New Pixel Developments
(focus: High Luminosity LHC)

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March 15th 2012

5th Detector Workshop Helmholtz Alliance, Bonn, March 14th -16th 2012

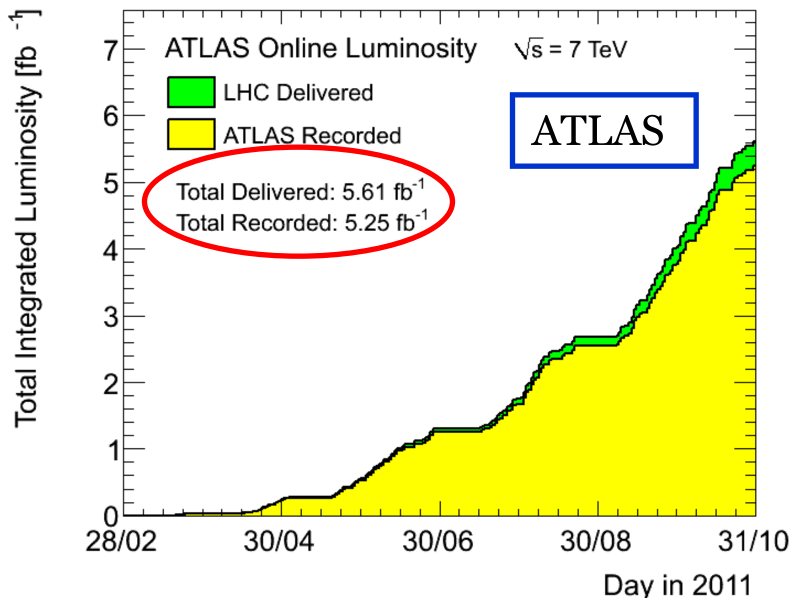
SI LAB
Silizium Labor Bonn

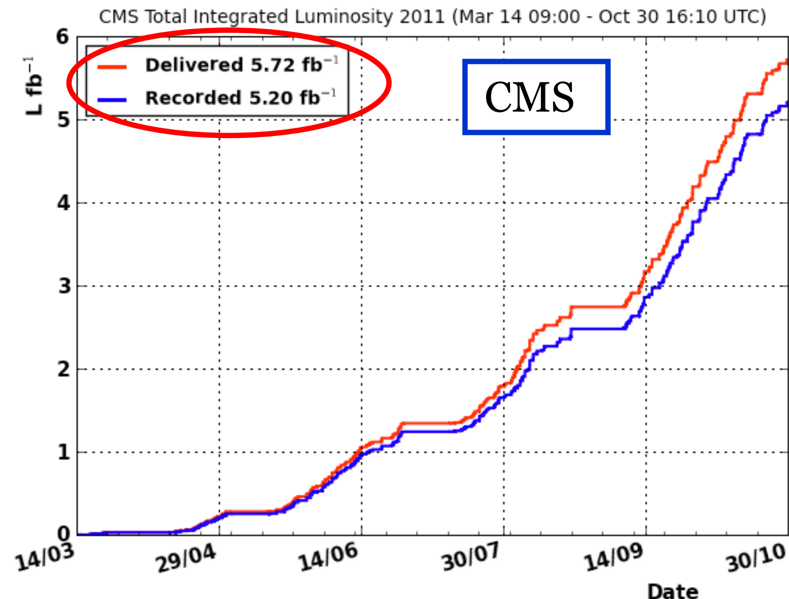
ATLAS Pixel Detector Collaboration

Introduction

- LHC, performing superbly.
- 2011: higher than expected luminosity
- 2011 a great LHC year…

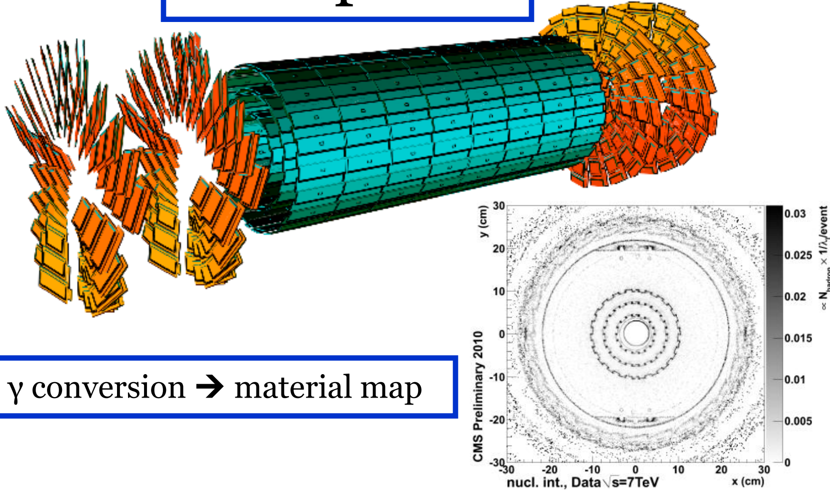
  and more to come for 2012!





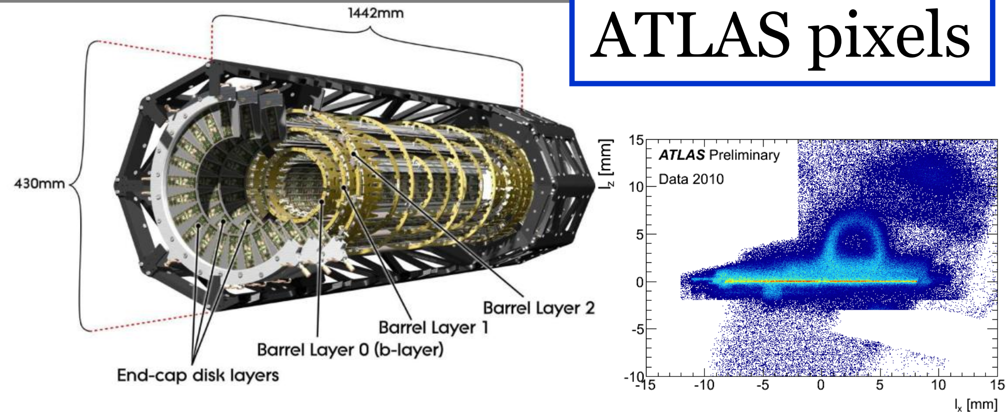
Current inner detectors at LHC

CMS pixels



γ conversion ➔ material map

ATLAS pixels



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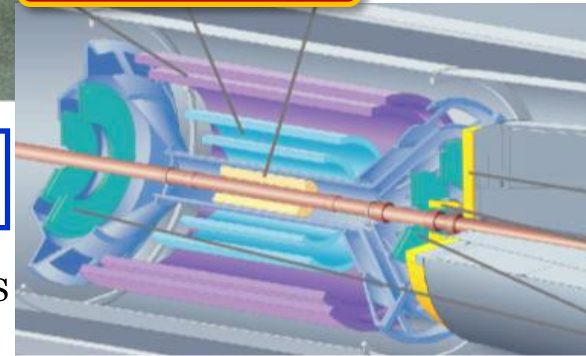
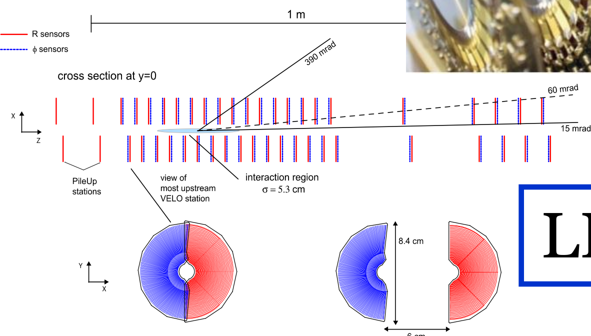




LHCb VELO

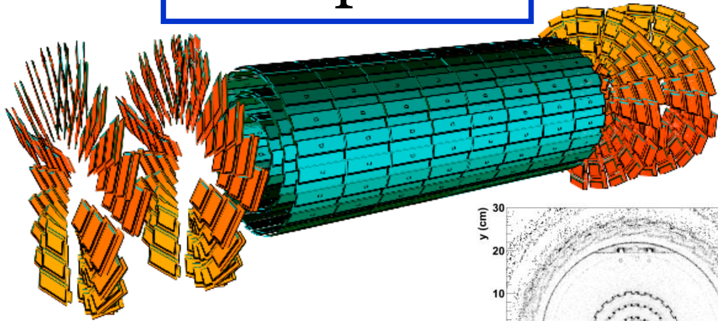
Alice Pixel

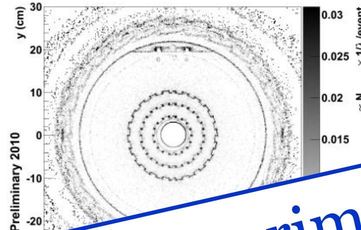
Closed for physics

Open during injection

Current inner detectors at LHC

CMS pixels





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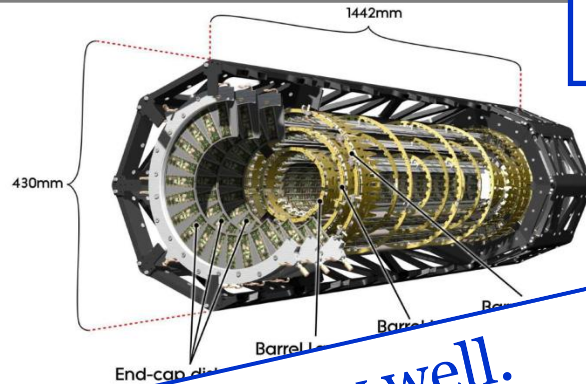
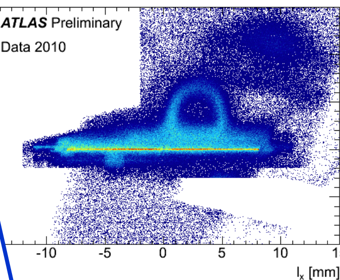
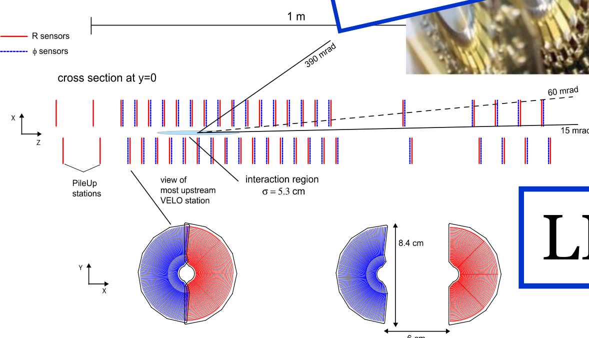




...sion ➔ material map

The 4 main experiments work very well.
Operational channel in all sub-detectors:
➔ typ ~> 97% or better for all!



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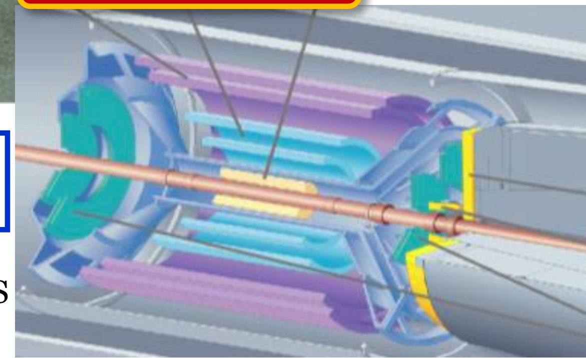

Needs for pixel upgrade for HL?

- High Luminosity LHC challenges for inner layers:

  - Higher hit rate.
  - Higher radiation levels.

  … while needing

  - High resolution.
  - Low material.

L. Gonella's talk

→leads to high performance for physics!

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ATLAS Pixel Detector Collaboration

ATLAS FE-I4 in 130nm CMOS

- Focus of ATLAS pixel FE designers' activity since ~2008.
- **Features**:
  - Smaller pixel 50×250μm² (resolution up + reduced X-section), big array -20×17mm² active- (simpler module, less material).
  - Low power (analog / digital array), low noise (digital / analog separation, T3 deep nwell), high radiation tolerance (130nm).
  - New pixel digital organization: buffers in 4-pixel region (only triggered hits are transferred to EoDC) ➔ efficient at high rate.
  - Data reformatting + 160Mb/s data transmission ➔high rate data transmission.
- **Full size 1st proto back fall 2010**, performs very well.
- **Production version** for IBL back Dec. 2011.
  - Works good (but not all parts thoroughly tested yet).

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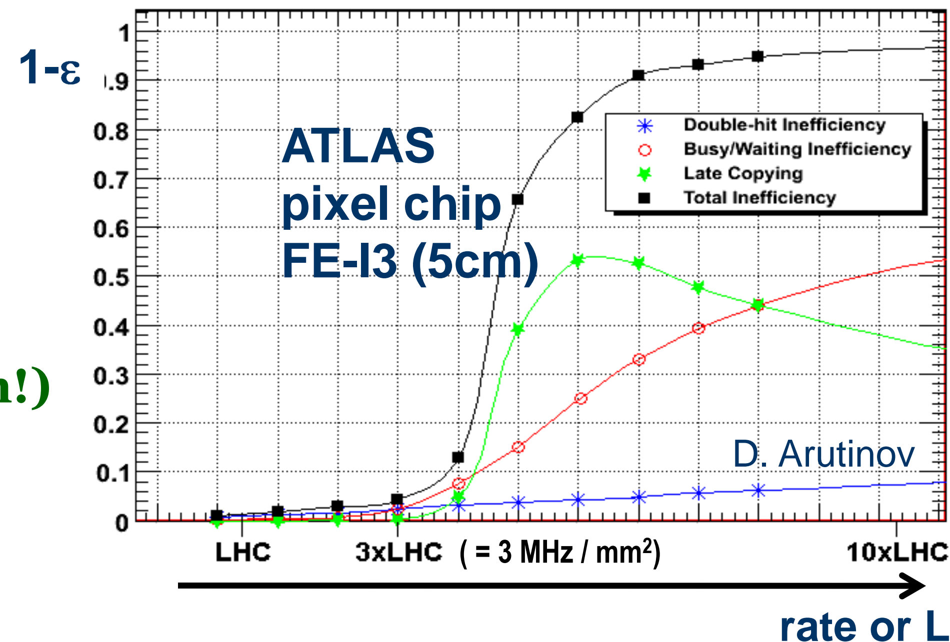
ATLAS Pixel Detector Collaboration

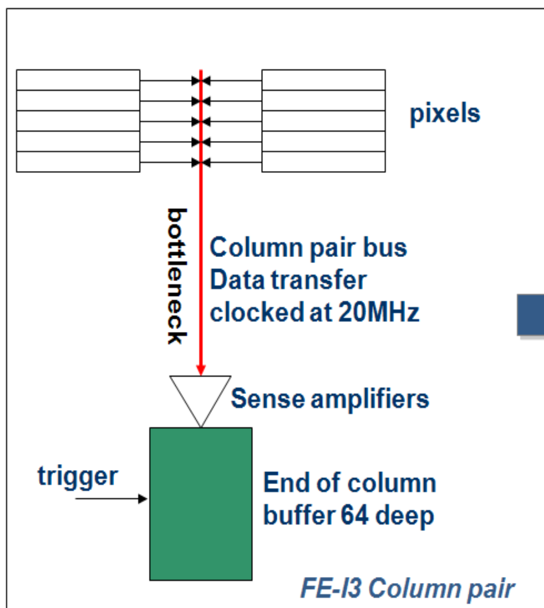
HL-LHC data rates & next ATLAS FE

Hit inefficiency rises steeply with the hit rate

Bottleneck: congestion in double column readout

⇒more local in-pixel storage (130nm!)
>99% of hits are not triggered
⇒don't move them -> not blocking





HL-LHC data rates & next ATLAS FE

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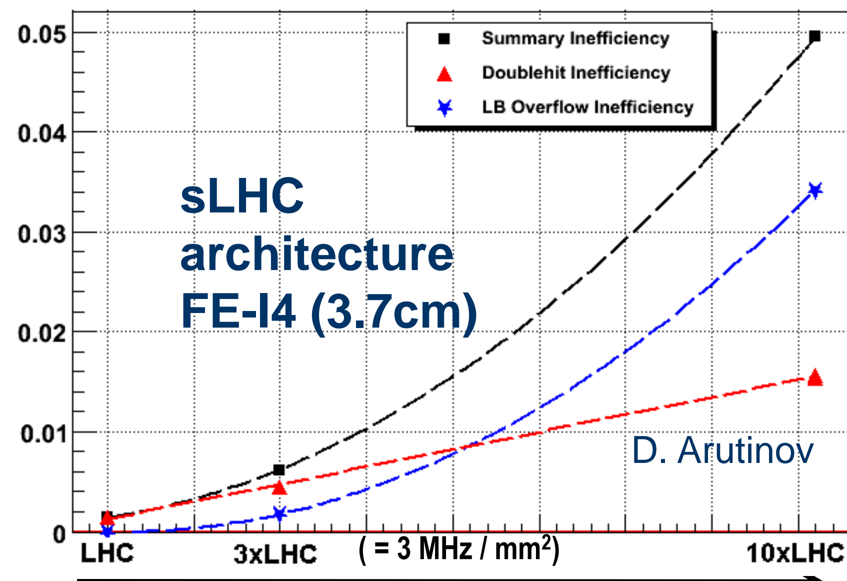
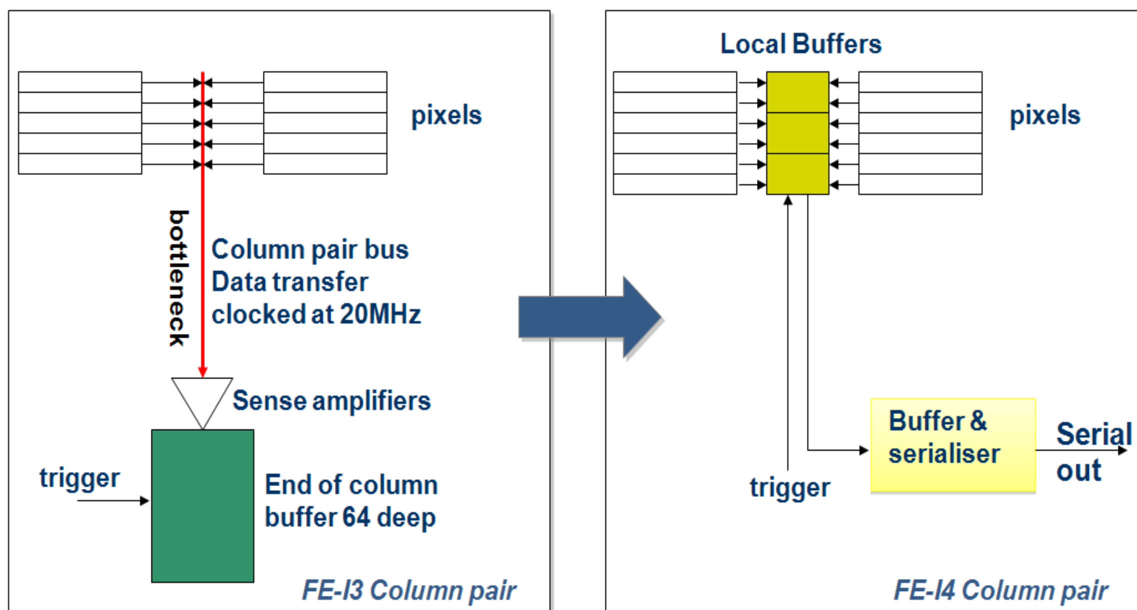
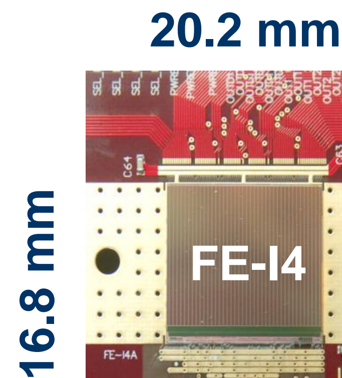




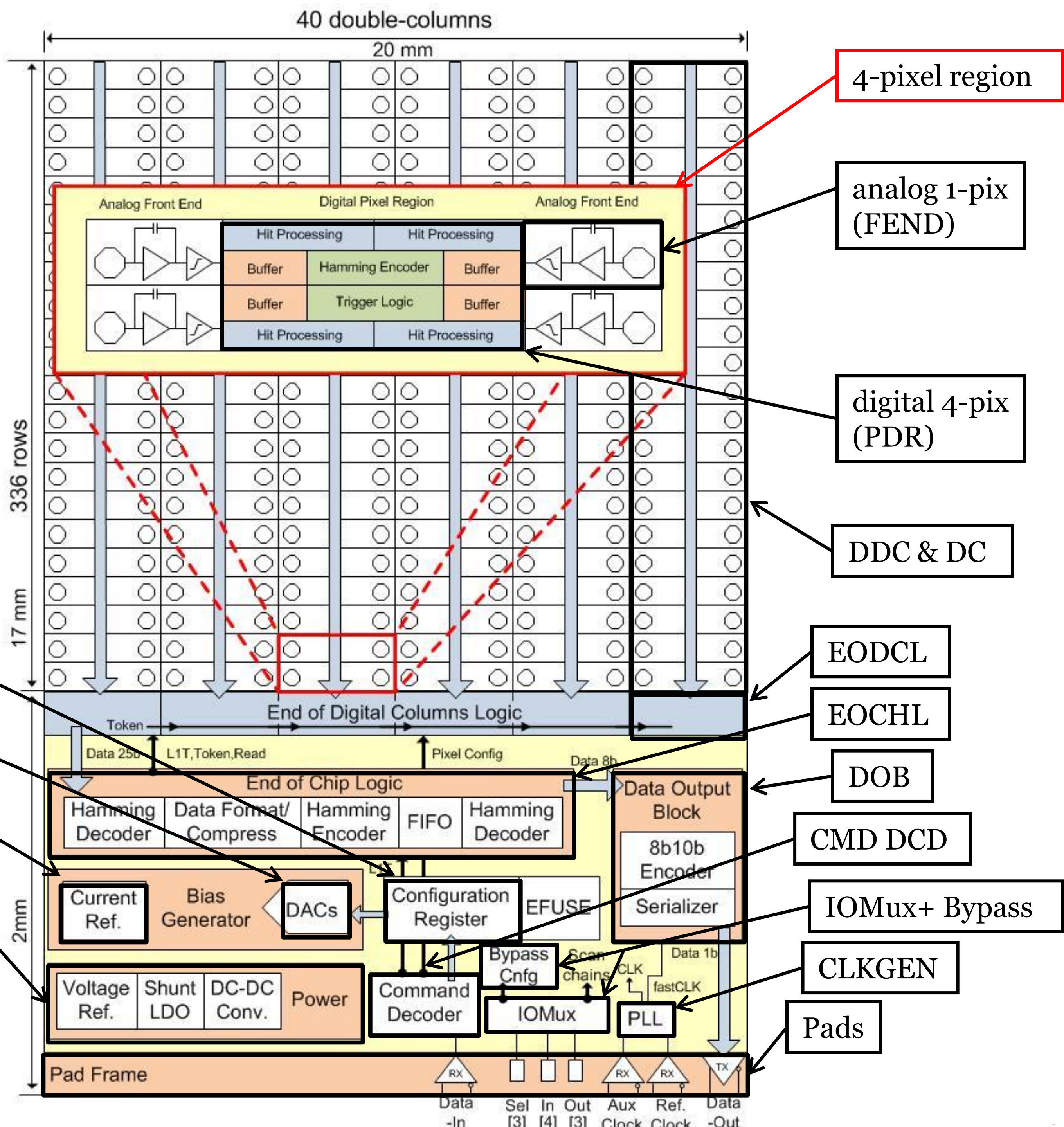


Bonn
CPPM
Genova
LBNL
NIKHEF

- **Overview**

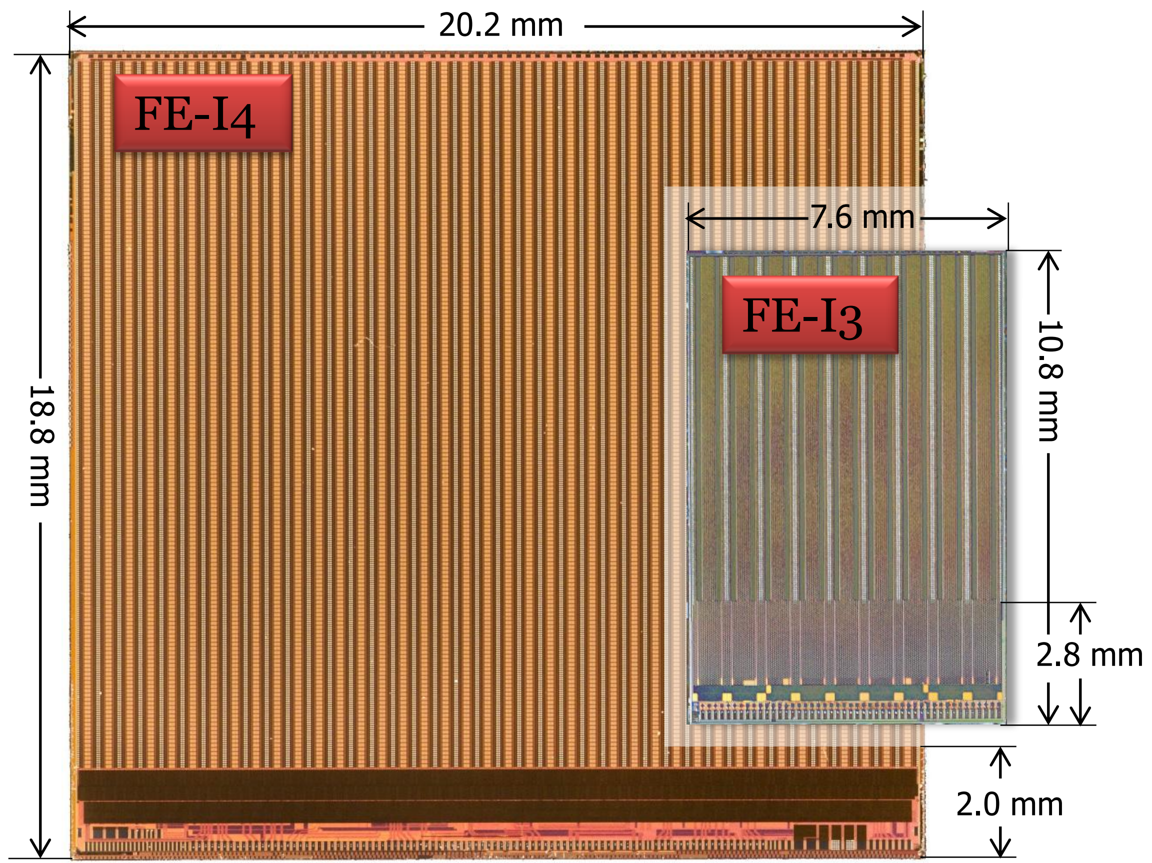
pixel array:
336×80 pixels

periphery



40 double-columns

20 mm



Data -In

Sel [3]

In [4]

Out [3]

Aux Clock

Ref. Clock

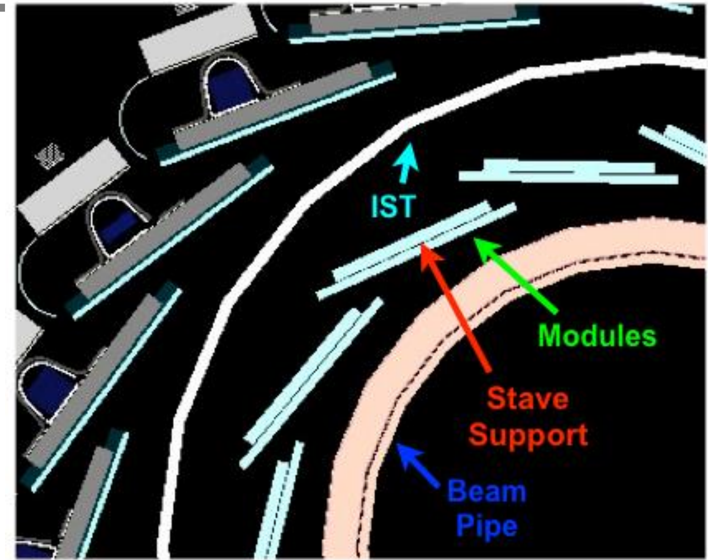
Data -Out

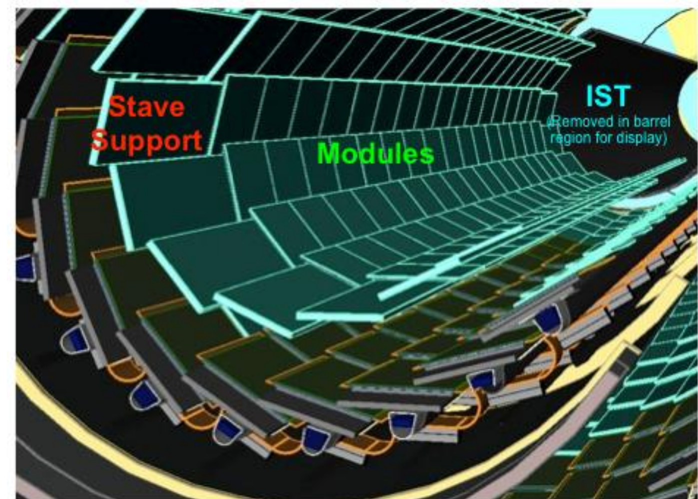
The Insertable B-Layer

- Layout based on performance studies in G4 and available space:

➡ smaller beam pipe (R_{min} = 26.5 mm)
➡ reconstruction: 4th Pixel layer
➡ IBL material adjusted to 1.5% X_o
➡ smaller z pitch (250 μm)

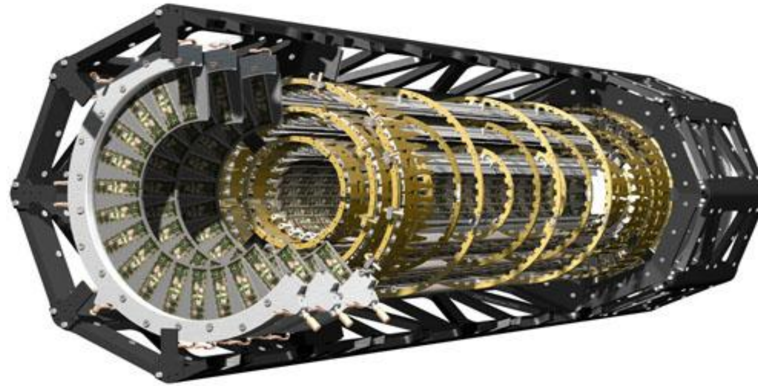
→Provide ATLAS with a 4 Layer Pixel Tracker from 2014 onwards.
→Maintain and improve physics performance (b-tagging vs. light jet rejection, vertexing) until HL-LHC.
→Provide redundancy in case of efficiency losses in other layers.
→Insertion of new pixel inside current pixel detector: Insertable B Layer IBL.
→IBL sensors at ~34mm radius: 250 Mrad TID and $5x10^{15}$ n_{eq}/cm^2 NIEL.
→ Installation 2013!





Targets FE-I4: IBL & HL-LHC

Present beam pipe & B-Layer

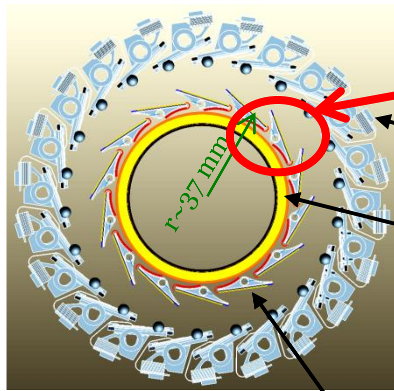


ATLAS Pixel Detector

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm

- Fast IBL ('13): inserted layer in current detector.

FE-I4B



Existing B-layer

New beam pipe

IBL mounted on beam pipe

FE-I4C

NewPix

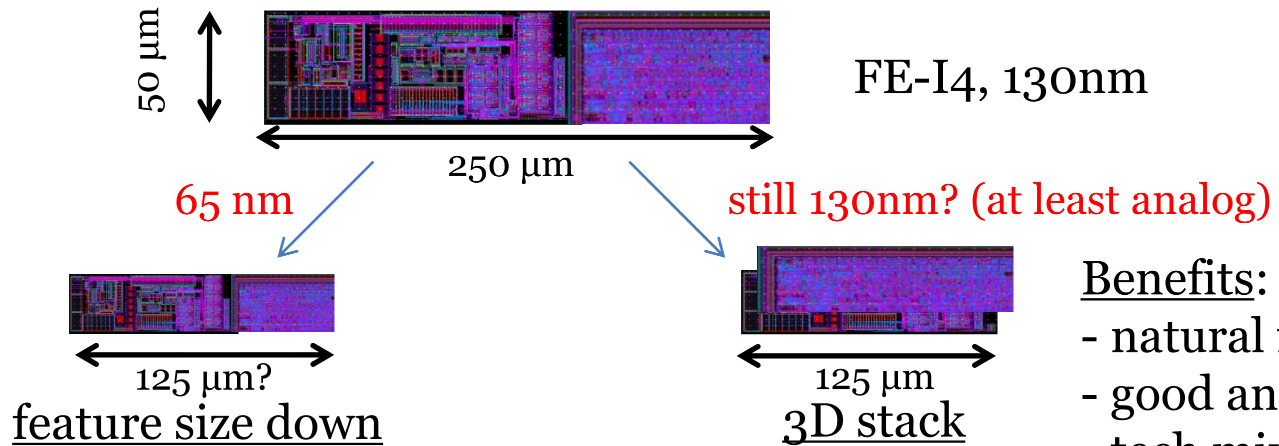
- Phase1 LHC / HL-LHC (>'17): 4-5 pixel layers, small radii / large(r) radii (note: Discussion on boundary pixel / short strips, ...).

  - All Silicon.
  - Long Strips/ Short Strips / Pixels.
  - Pixels:
    - 2 or 3 fixed layers at 'large' radii (large area at 16 / 20 / 25 cms?)
    - 2 removable layers at 'small' radii

Inner pixel layer at HL-LHC

- **Inefficient if FE-I4 like.**
- Need higher rate capability.
- Need smaller, faster pixel.
- Need more memory per pixel to handle high rate.
- Need new FE with smaller pixel size and more space for digital pixel → **smaller feature size** (e.g. 65nm) or **3D**.

IBL & outer pixel layers HL-LHC



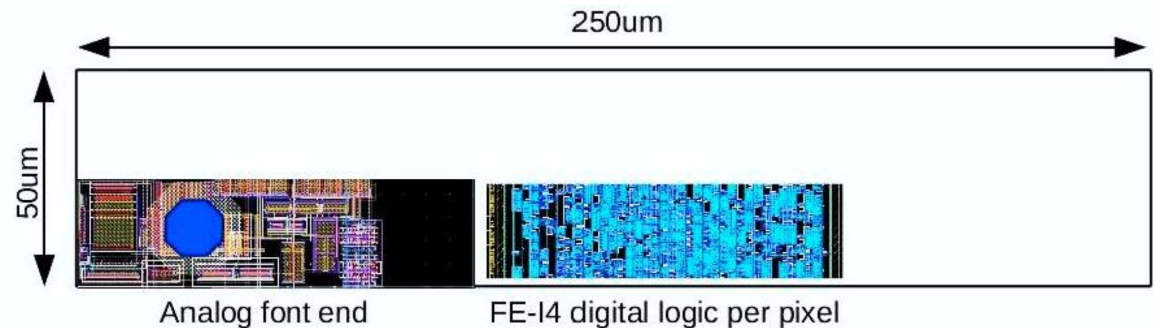
Benefits:
- maturity.
- mainstream.

Benefits:
- natural fn split.
- good analog.
- tech mix.

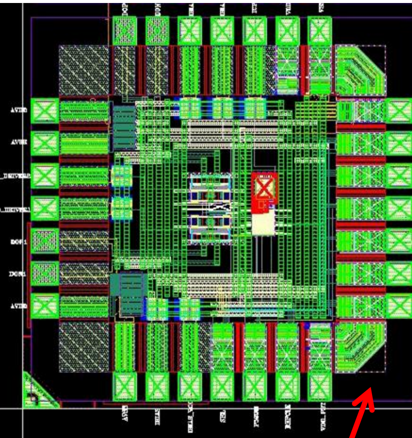
And make more cleaver pixels!

65nm CMOS effort

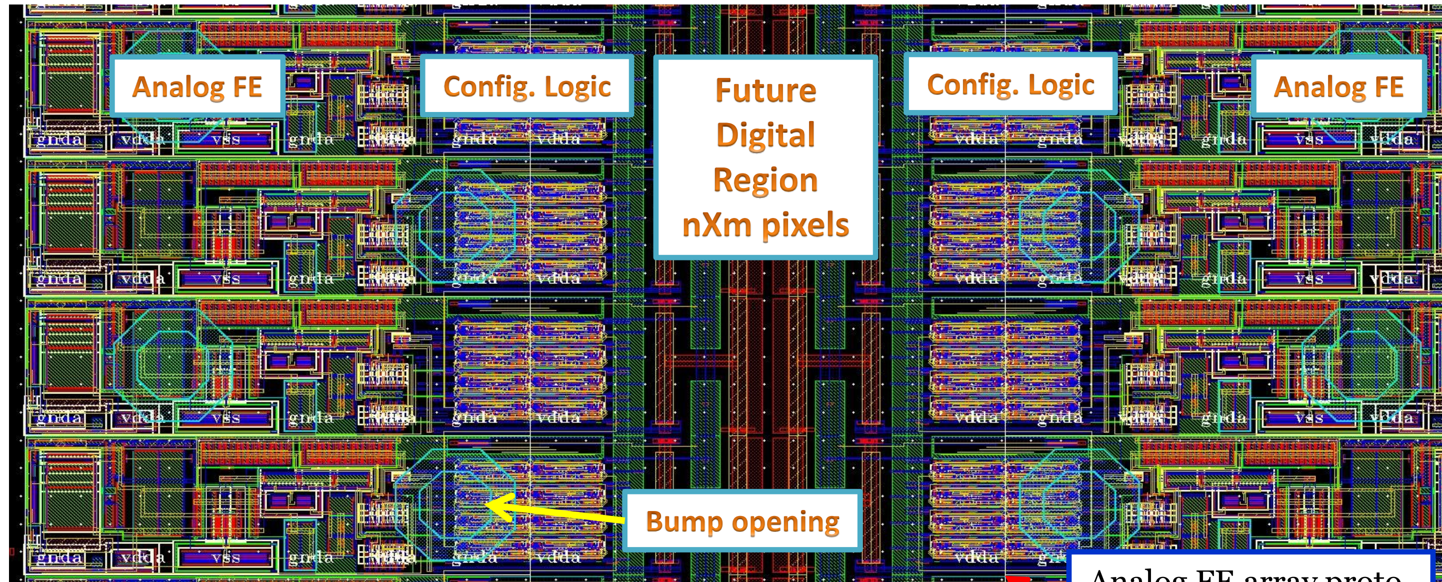
- Approx. factor 4 area reduction for digital circuits wrt 130nm.
- Conventional wisdom says not much gain for analog circuit (as needs employ more complex archi., move away from minimal).
  - Still transistor performance is not all the picture (capacitors, switches, interconnects do scale!)
  - Strategy then to reduce analog complexity, and do more on digital signal processing.
- Prototyping for HL-LHC has started: Array, prototype blocks – low power comparator, RAM, PLL (synergy with Depfet DHP digital IC design)-.



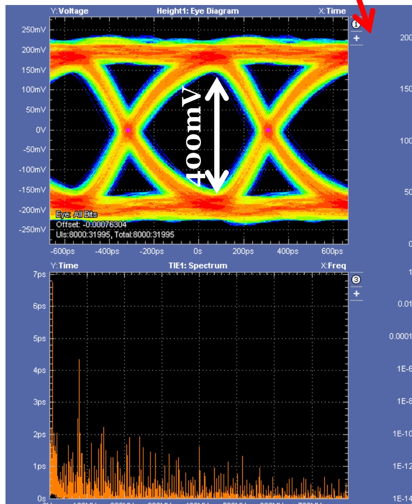
1st prototypes in 65nm

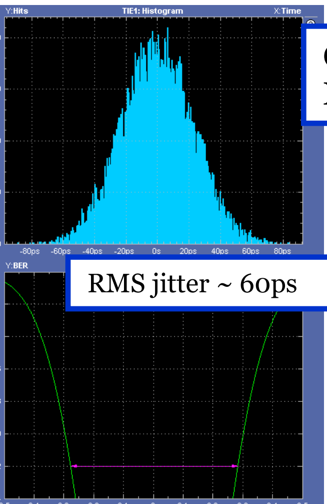


1.6 GHz PLL-PRBS-CML
T. Kishishita, Bonn



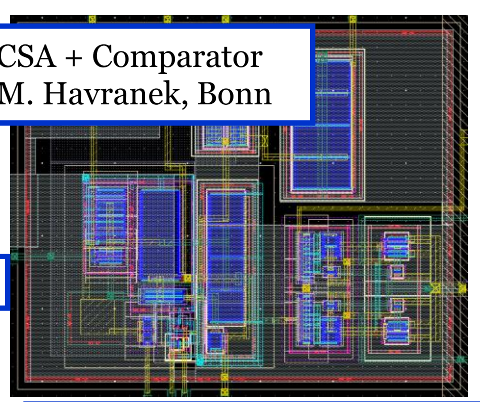
Analog FE array proto
A. Mekkaoui, LBNL





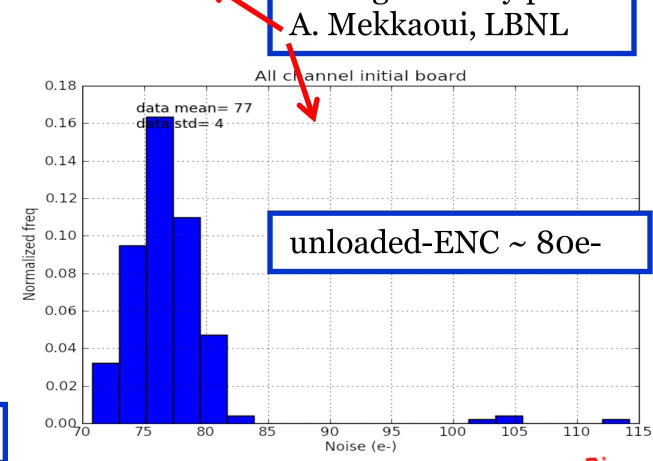
RMS jitter ~ 60ps

1.6 Gbps, PRBS, preamp on



CSA + Comparator
M. Havranek, Bonn

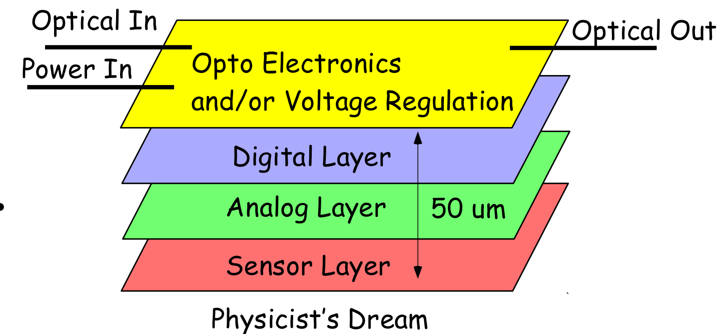
dyn. comp.: 2.4μW @40MHz



unloaded-ENC ~ 80e-

3D electronics: FE-TC4

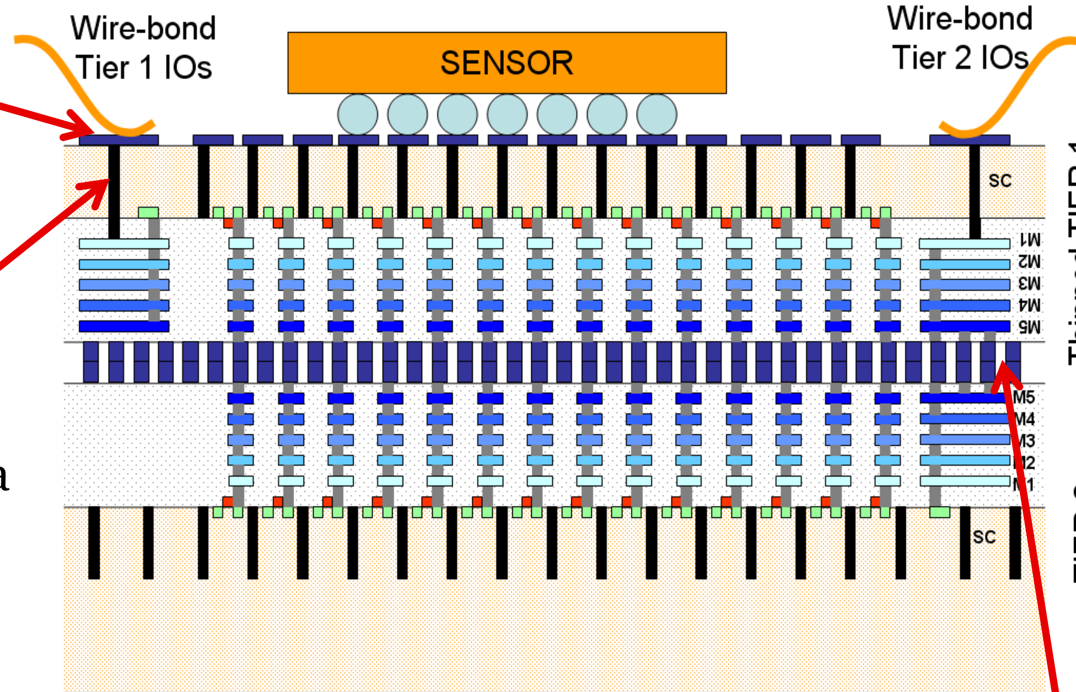
- Collaboration Bonn (Germany), CPPM (France), LBNL (USA).
- Goal: a 50×125 μm² 3D chip, with split analog and digital functionalities.
- Technology:
  - 130nm (restricted to 5 metals for now).
  - 3D process.



- Prototypes submitted in 2D, as technology test bench.
  - Good performance, good radiation tolerance.
- 3D analog + digital stack submitted. 1st prototypes back last year.

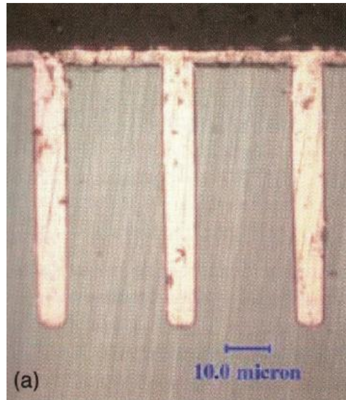
3D technology enablers

Metallization after thinning

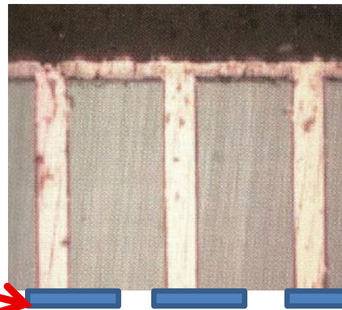


Face to face

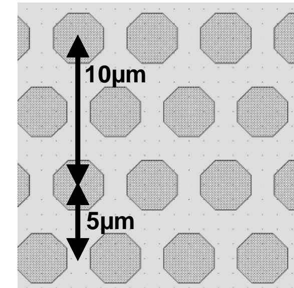
Through silicon via



Via access after thinning



Intertier bonding interface

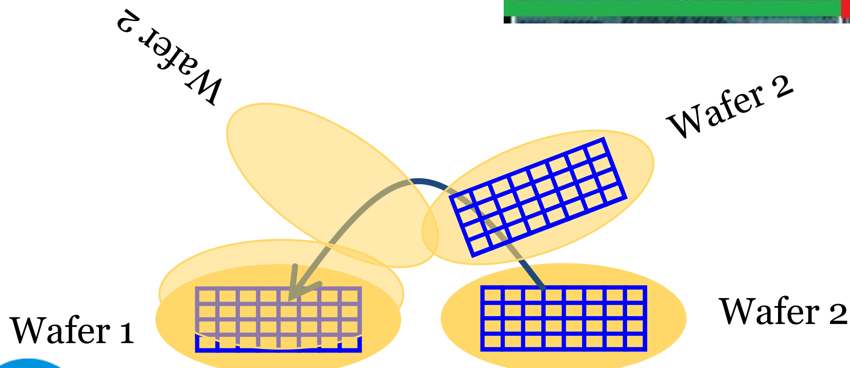


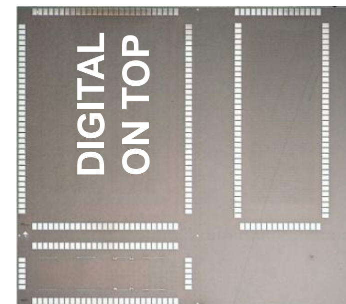
Metallization

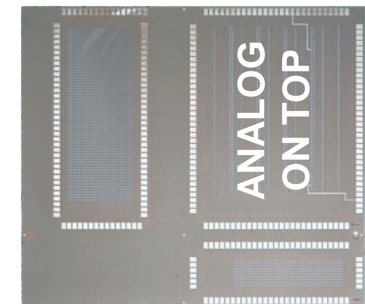
1st HEP 3D MPW

- FNAL led (participants from Canada, France, Germany, Italy, Poland, USA).

ANALOG
DIGITAL
DIGITAL
ANALOG







Analog Tier

Based on FE-I4 analog pixel

FE CELL BLOC DIAGRAM

Config word (13bits)

dacif5

docvth5

VFB

Local feedback tune

Local threshold tune

VFB2

VTHEFF

NotKill

super contact from the sensor

to the digital tier InterTier bonding

inj0

inj1

injectIn

Cinj1

Cinj2

CF

CF2

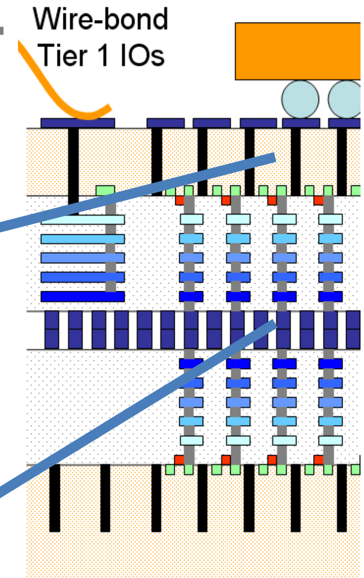
CC

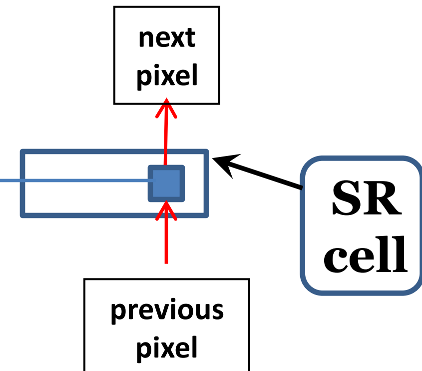
feedbox

preamp

amp2

HitOut





2 read-out mechanisms:

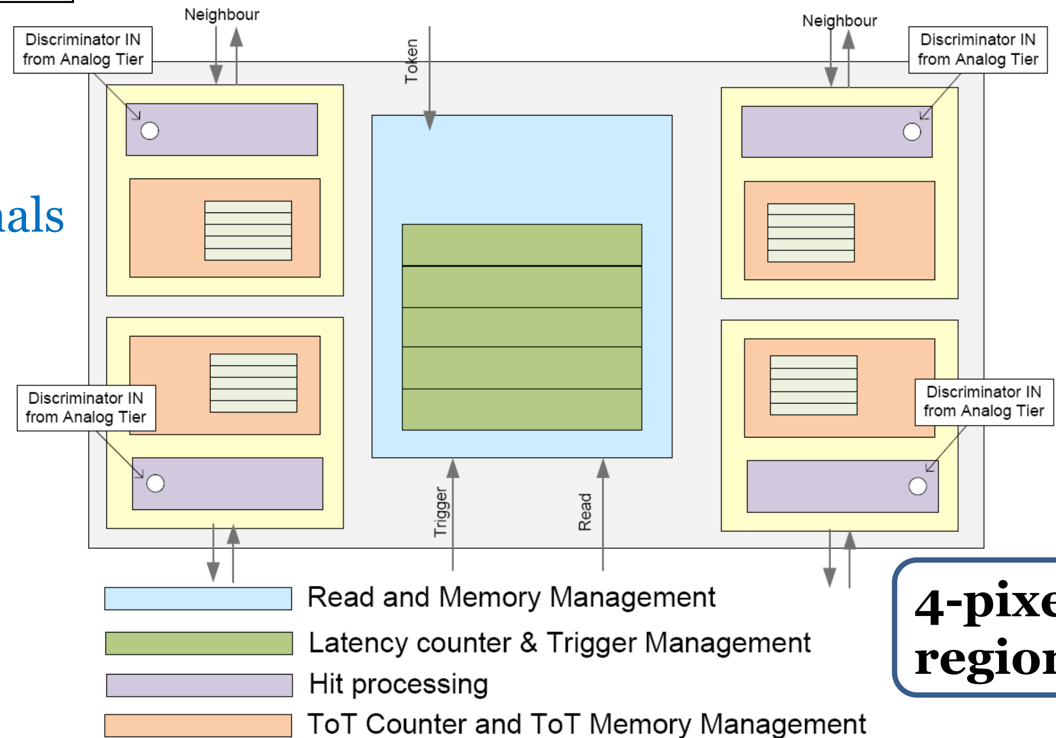
- Based on the analog tier shift register.
- Using the digital tier.

Digital Tier

Based on FE-I4 4-pixel region

- Simplified periphery: Control signals provided from outside

- Simple configuration through a shift register.

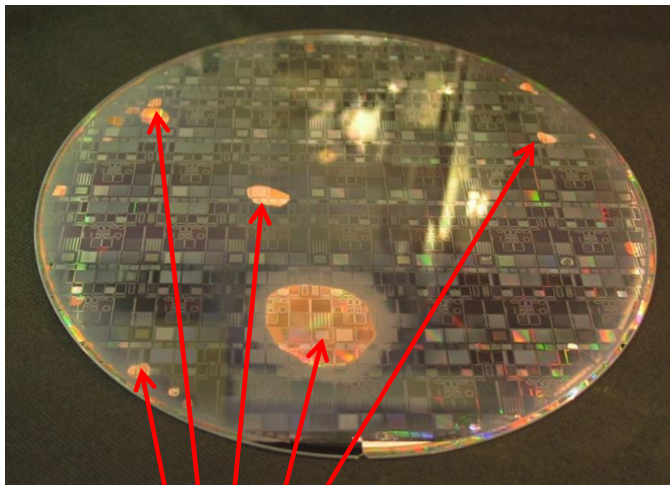


4-pixel region

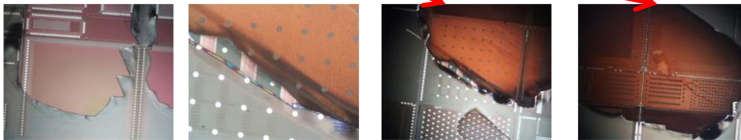
- 2 readout modes:
  - simple readout using DC shift register for test purposes only.
    → *no ToT, read-out whole pixel array.*
  - regular readout similar to the full FE-I4.
    → *read-out only triggered pixels, ToT information.*

3D IC processing issues

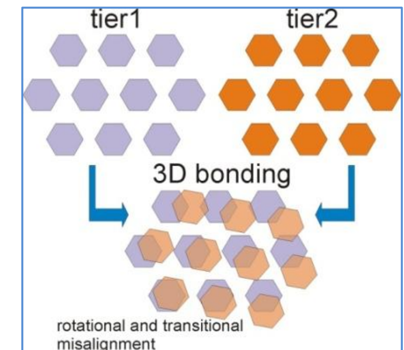
- > 30 single wafers produced , only 3 bonded wafer pair of poor quality accepted so far.



Damages on the wafer &
Close up photographs

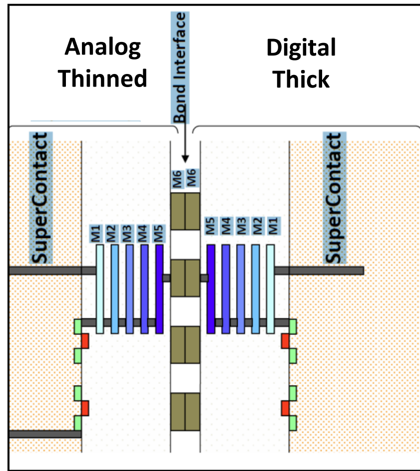


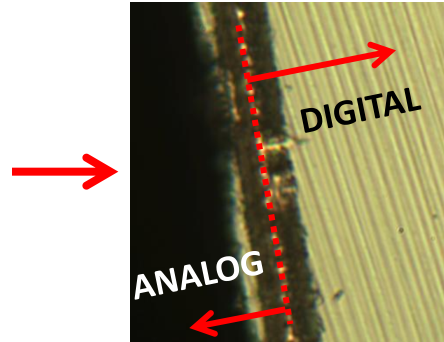
Bad electrical & mechanical connection due to misalignment of the tiers.

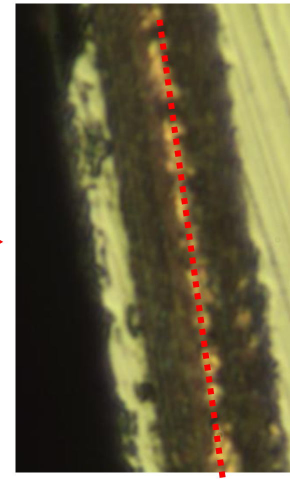


Bad mechanical connection between tiers lead to top tier removal during thinning process

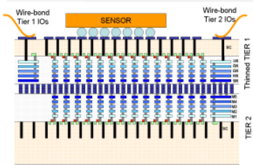
12µm thinned down analog tier

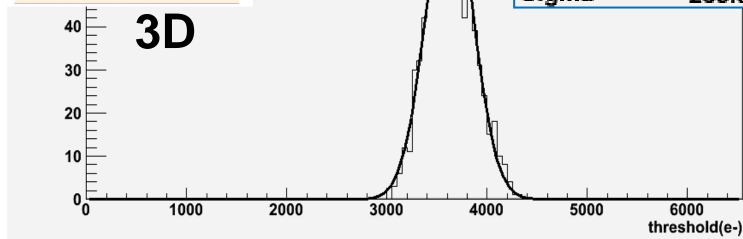






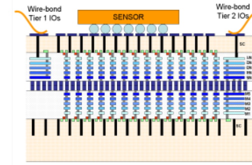
Threshold

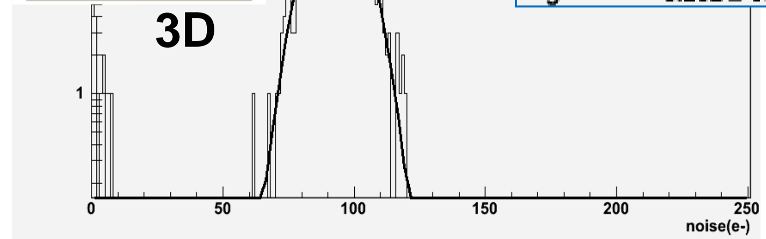




Entries	854
Mean	3630
χ^2 / ndf	20.54 / 23
Prob	0.6093
Constant	71.66 ± 3.14
Mean	3624 ± 8.5
Sigma	233.8 ± 6.7

Noise





Entries	854
Mean	91.31
χ^2 / ndf	56.67 / 52
Prob	0.3049
Constant	38.76 ± 1.79
Mean	93.19 ± 0.30
Sigma	8.252 ± 0.254

TSV drilled thinned down analog tier (12 µm !!!) works with marginal noise increase.

A perfect detector for HEP

Rad-hard

High hit rate

Large area

Monolithic

Intelligent pix

Low cost

High resolution

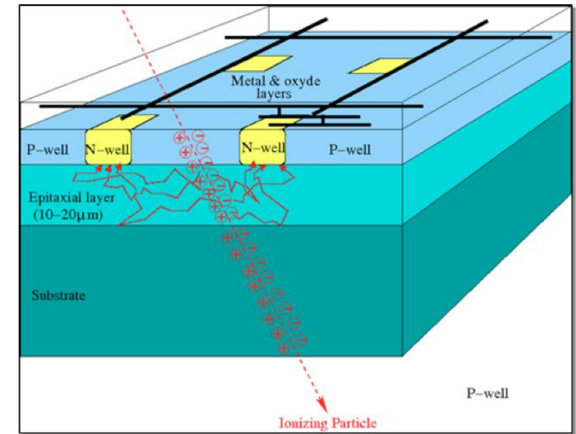
Low noise

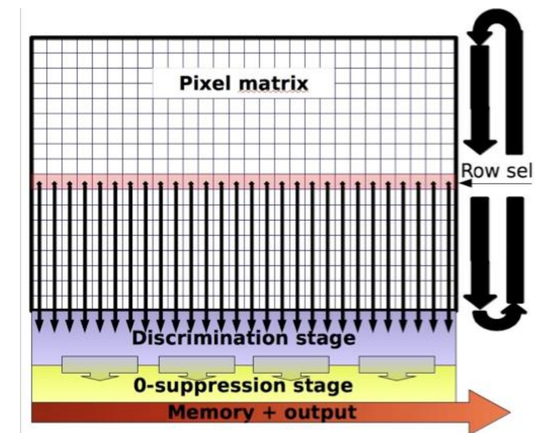
Low power

CMOS MAPS

- standard CMOS process.
- no PMOS in-pixel.
- signal collection diffusion (speed).
- small signal (typ. 1000e-).
- small noise (typ. 20e-)
- small pixel size.
- not rad-hard.

- STAR pixel upgrade, EUDET telescopes

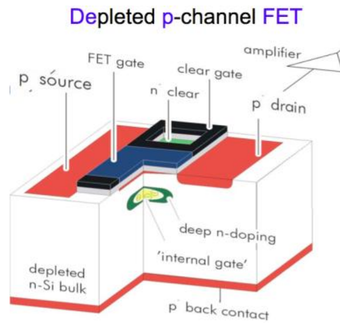


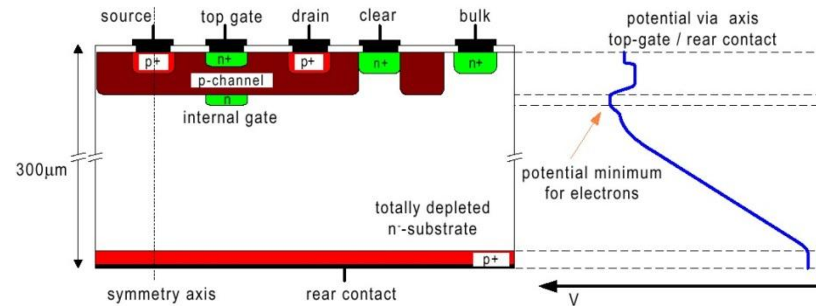


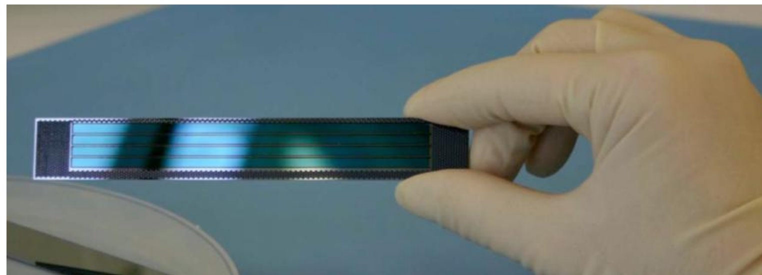
➔ Suited for high precision, low rate, low rad.

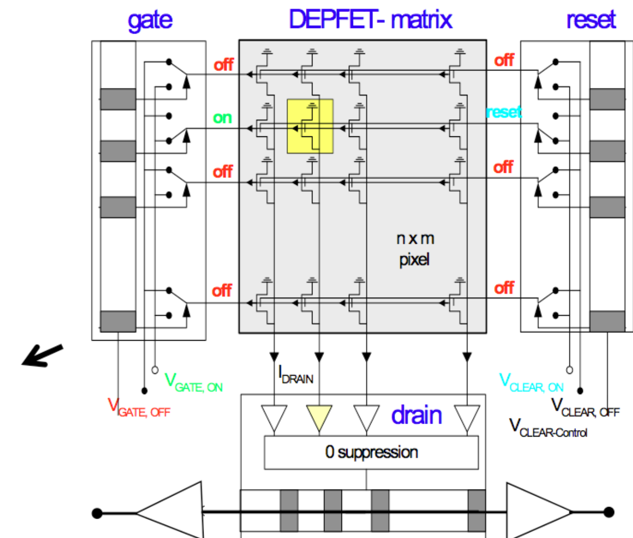
Depfet

- Baseline for Belle II.
- pixel size 50×50µm².
- SNR ~20/1
- rolling shutter, 100ns pro row.
- Thickness ~75µm.









→ Suited for high precision, low rate, low rad.

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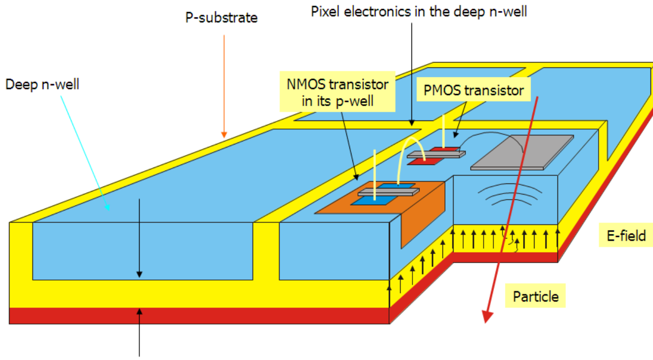


HV-MAPS

Ivan Peric, Mannheim / Heidelberg

AMS 350nm → 180nm

Pixel i

Pixel i+1

P-Well

HV deep N-well

14 μm @ 100V

~1000 e

Depleted

P-substrate

~1000e

Not depleted

Benefits and drawbacks

- Monolithic, sensor + P/NMOS .
- Fast signal collection time by drift.
- Charge collection @ surface → thinning.
- Low price ("standard CMOS").
- Tolerance to non-ionizing radiation damage (high drift speed, short drift path)
- Tolerance to ionizing radiation
  - (DSM, rad tolerant designs can be used)

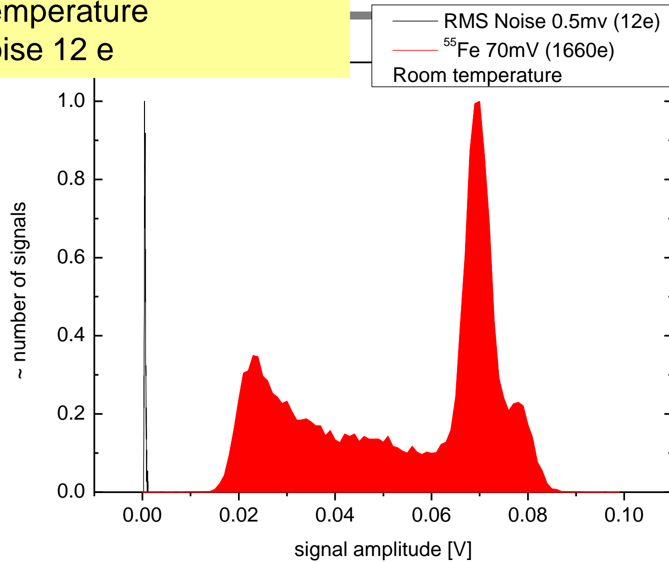
BUT:

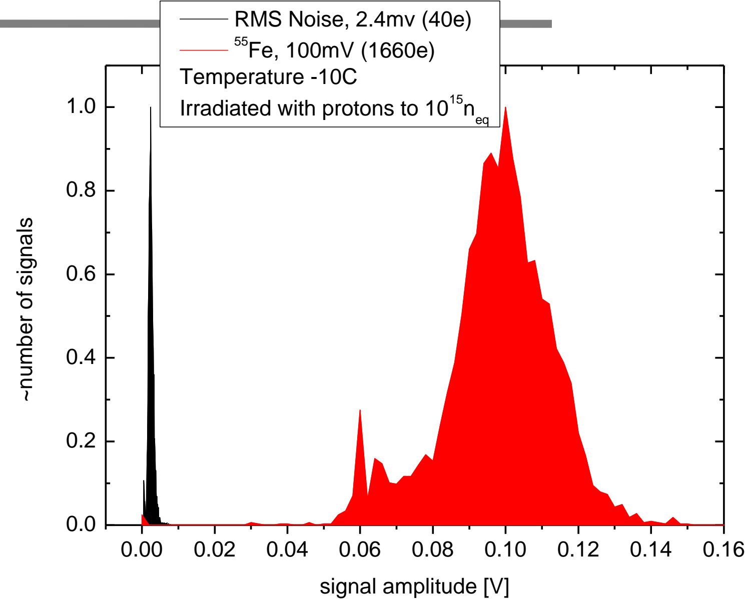
- PMOS and collection node share same bulk.
- Large size of collecting electrode.
- Not fully depleted.

Rad and read

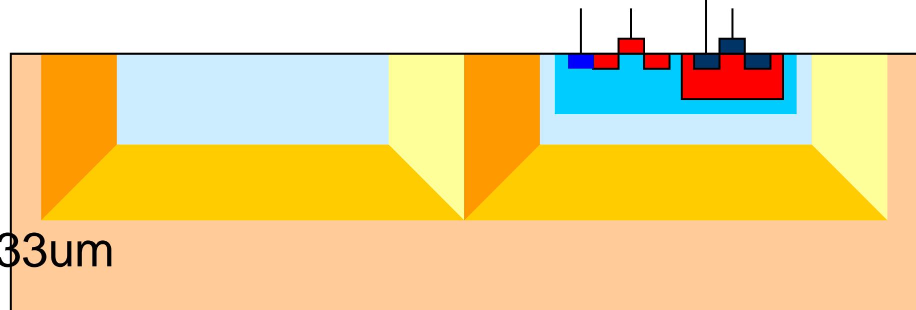
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e

^{55}Fe spectrum, RMS noise
Proton-irradiated 10^{15} n_{eq} / 300Mrad
-10C
RMS Noise 40 e





- Read by capacitive coupled pixels?
  - no bump-bond.
  - increased resolution.
  - commercial sensor techno.
  - sensor thinning.
  - bias < 60V.
  - 100% fill factor.



Conclusion

- LHC experiments now: the time of hybrid pixel technology.
- Still technologies used have aged, and hybrid pixel can benefit now from smaller feature size on FE side.
- But new technologies might be game-changer for HEP:
  - 3D integration.
  - Monolithic concepts.

time well your efforts wrt process maturity!

- Keep an eye on new technologies (new HV technology options which could solve HV-MAPS issues, use of HR wafers → 3 key words: integration, isolation, depletion).

- Not covered:
  - CMS upgrade efforts. R. Horisberger's talk
  - SoI developments, μ-pattern gas avalanche detector…

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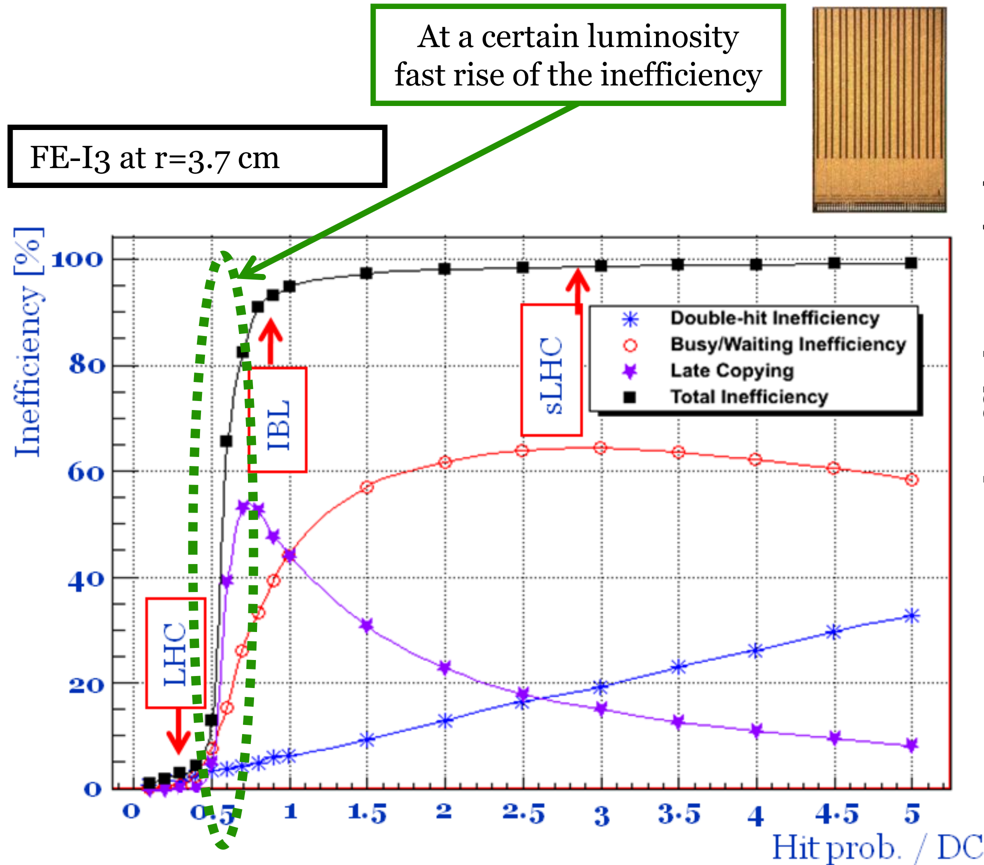
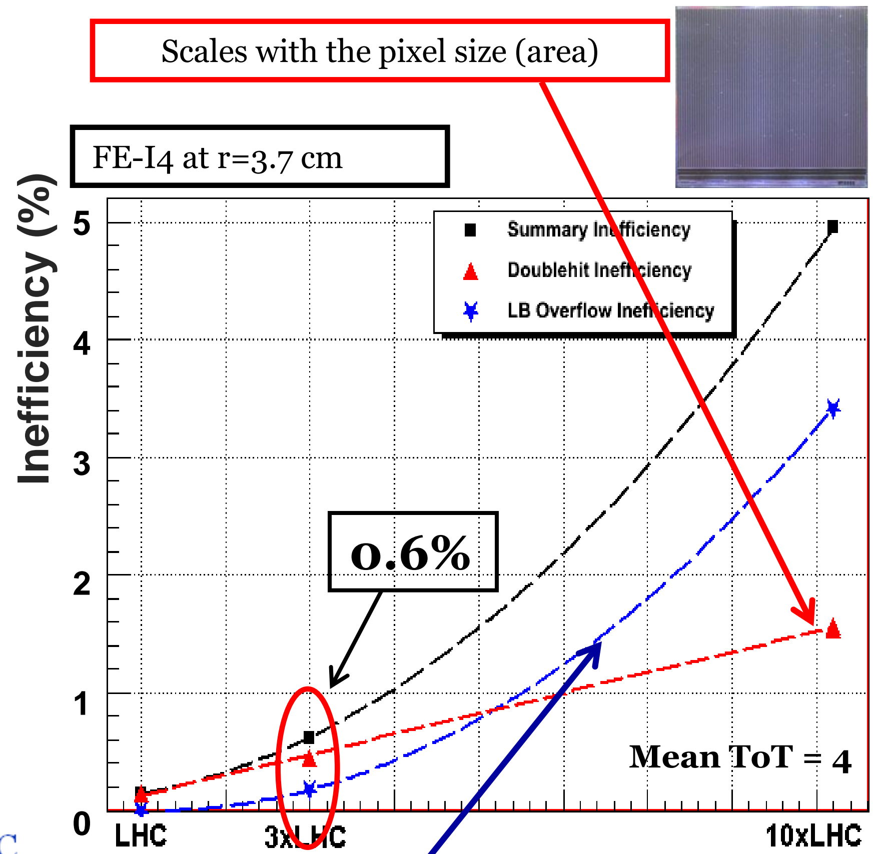
Backup

BACKUP

Hit rate

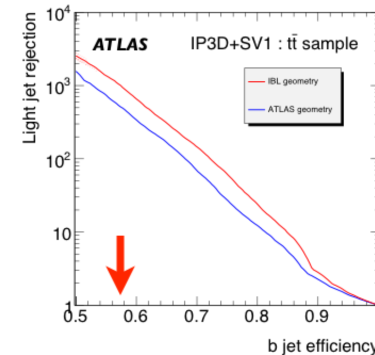


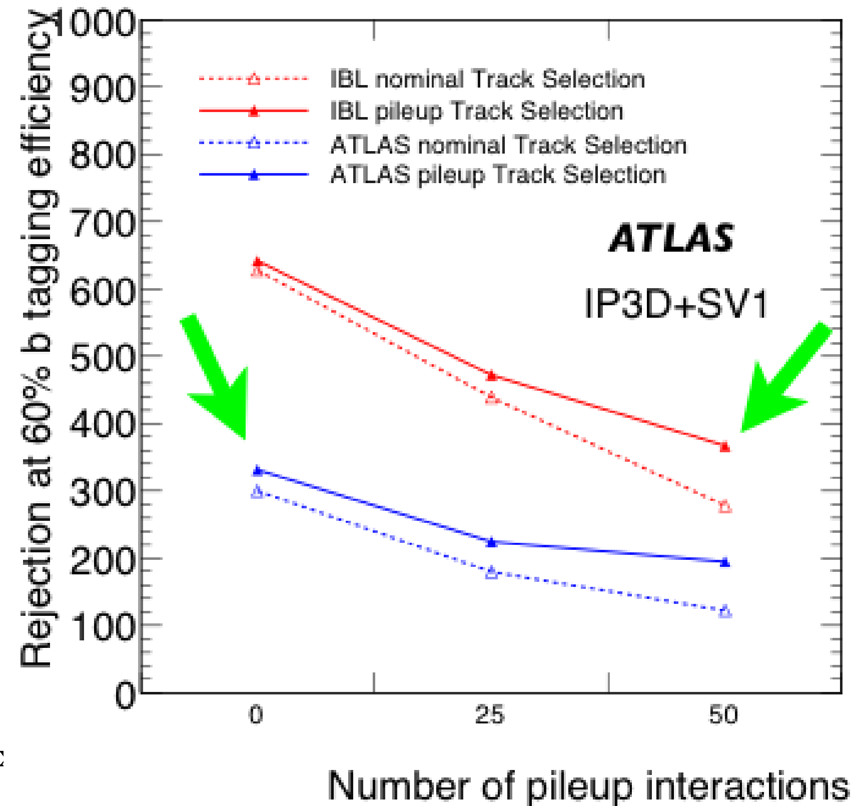


Can be kept low by storing more hits locally. Bigger memory size

B-tagging with IBL

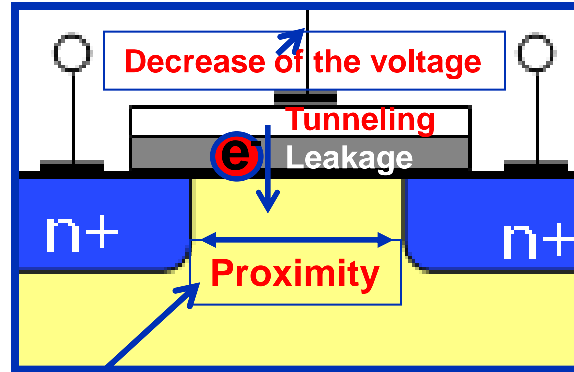
- Look at light-jet rejection at 60% b-tagging efficiency at different pile-up conditions:
- Rejection significantly increases with IBL
- "Restores" rejection for high pile-up events:
  - rejection at high pileup as good or better at current ATLAS without pileup
- Clear benefit from 4th layer
- The 4th Layer also provides redundancy against efficiency losses in other layers

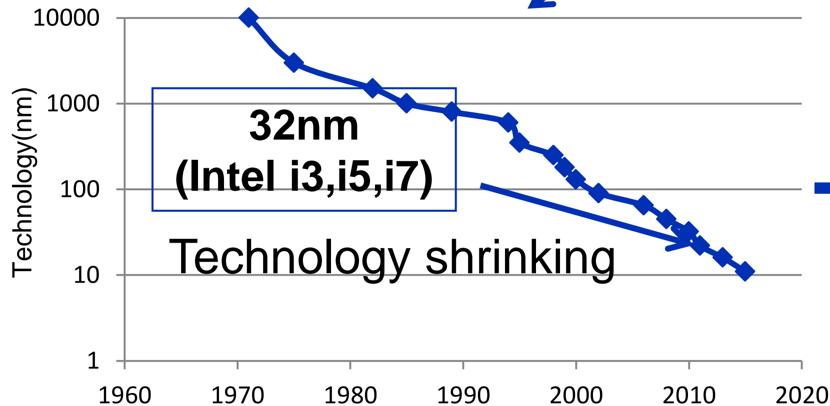


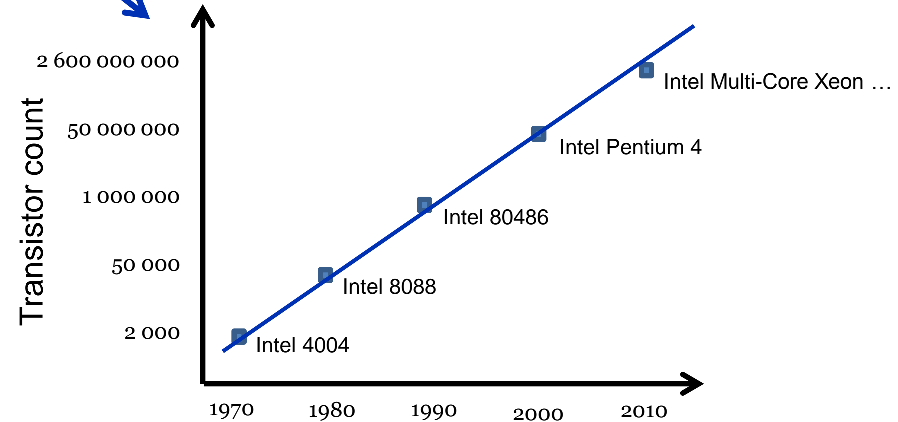


Chips and Transistors

•Nowadays chips contain millions of transistors.







- Smaller transistors ➔ More transistors per unit area ➔ More functionality
- But smaller transistor size ➔ new issues (smaller distance between "source" and "drain", thin gates, Smaller gate voltage, tunneling effect and leakages, higher doping profile)

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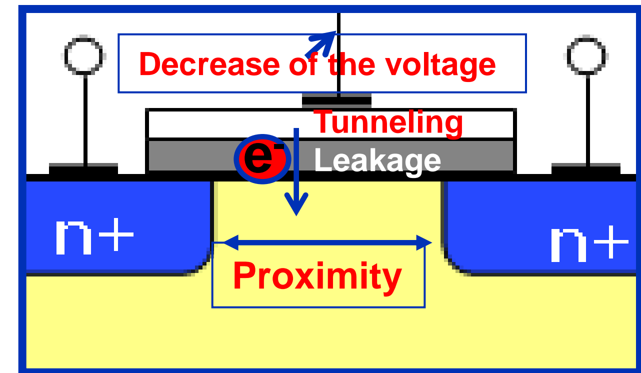
Limitations of scaling down

- Problems with feature size decreasing
  - New issues @ transistor level
  - Increase of interconnection density :
    - parasitic RC delays
    - parasitic inductances
    - increases heat dissipation
    - power consumption
    - noise coupling.

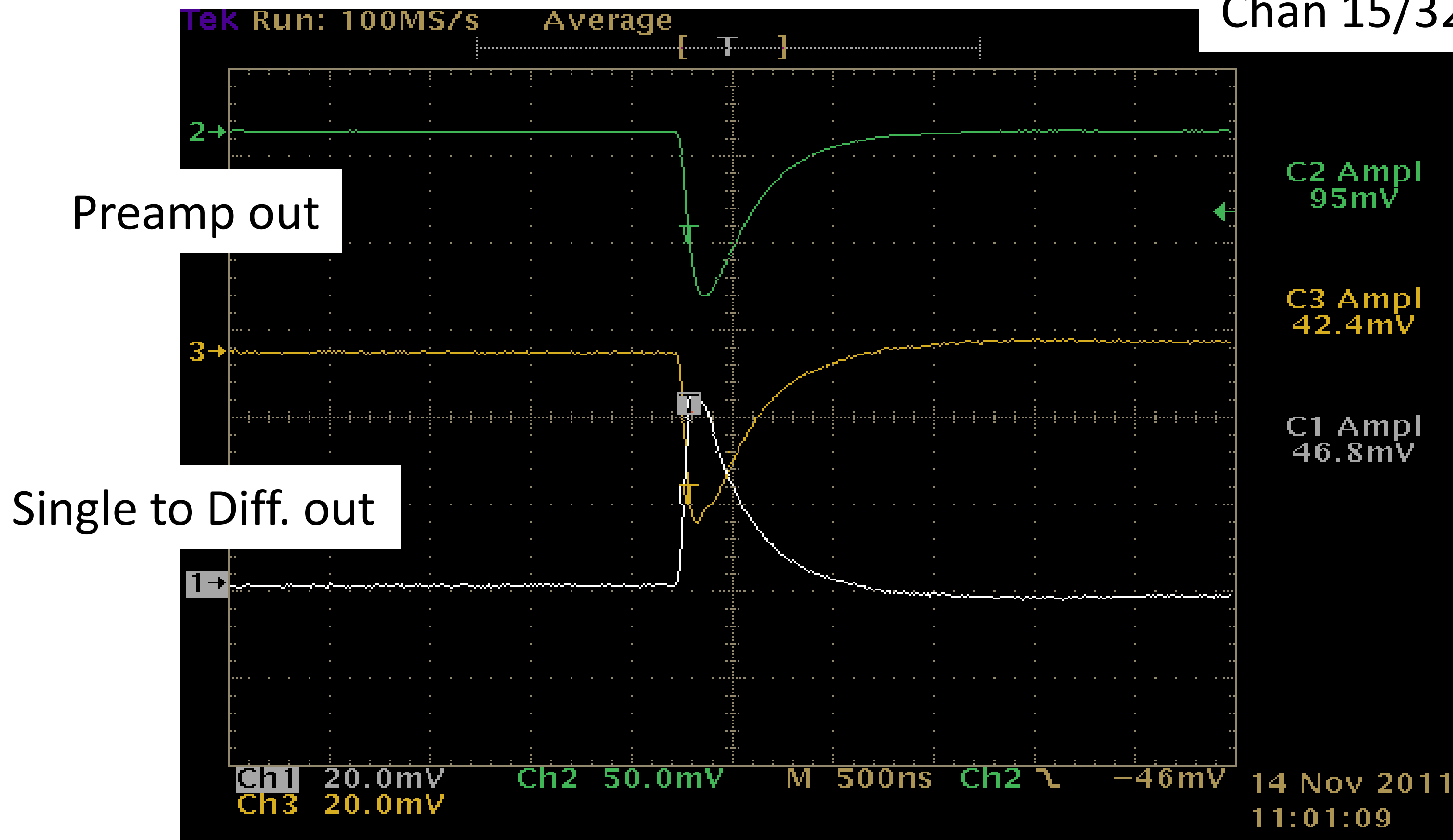


Wiring crisis

  - Even if the above limitations will be circumvented mixed signal designs could suffer from the small feature size: when for the digital part this would be a natural choice, "designers' conventional wisdom" → analog performance could degrade due to small transistor size.
- 3D packaging/integration could help
  - Possible solution could be to break the IC circuit into several layers, and stack them on top of each other:
    - More transistors per unit area without decreasing feature size.
    - Interconnect vertically. Shorter distance.
    - Different technologies for different layers.
    - Compact modules integration the sensor as well

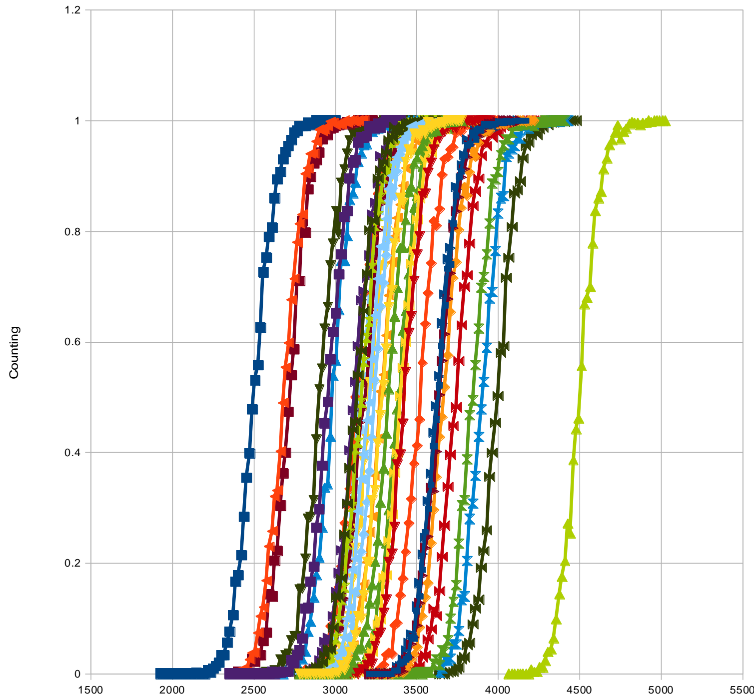
65nm array test results

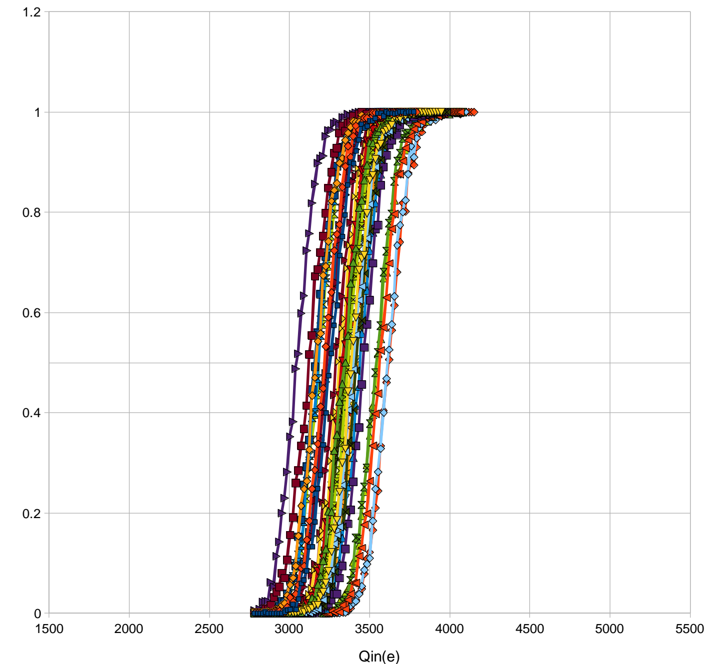
Chan 15/32 Qin: 2ke

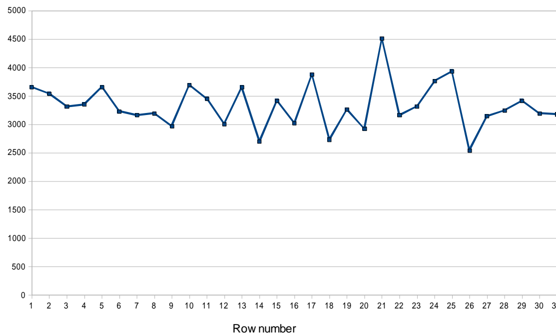


- Chip found to work as expected!
- VDD=1.2V
- I= 5 µA per pixel (can be as low as 2 µA)

65nm, threshold adjustment



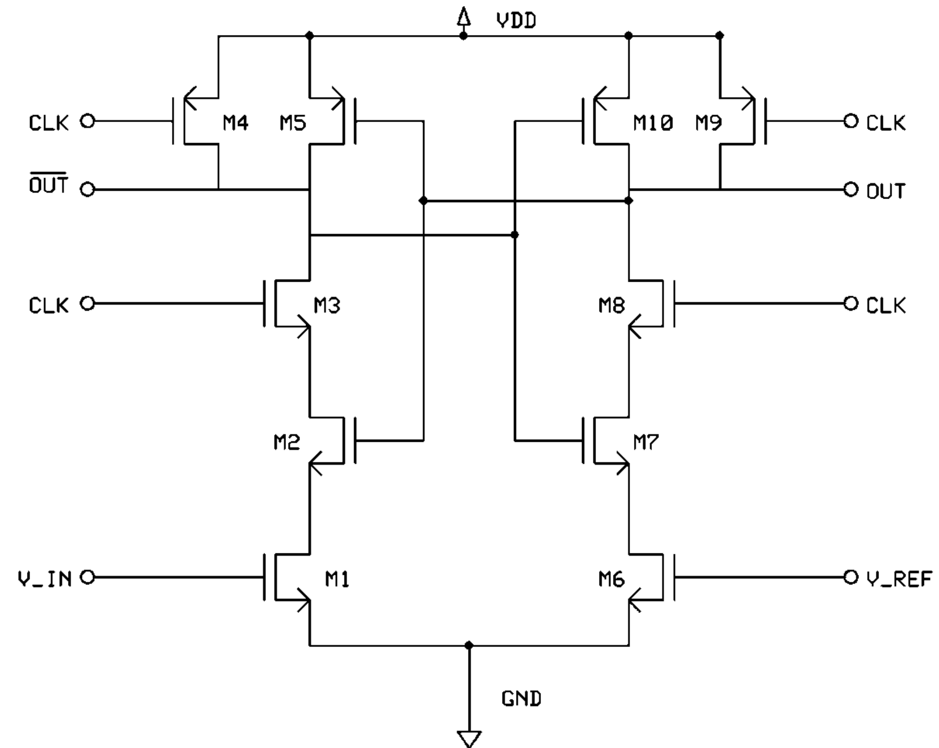




- Mean value : 3350 e-
- RMS value : 140 e-
- Peak to peak value : 560 e-

Dynamic comparator

- Motivation: reduce power consumption
  - comparator in FE-I4 has static power consumption of 5.6 µW
- Benefits of dynamic comparator:
  - high speed
  - nearly zero static power consumption
  - low voltage operation
  - rail to rail output
  - small chip area
- Drawbacks:
  - sensitivity to correct layout (symmetry)
  - sensitivity to symmetric load



Dynamic comparator – post-layout simulation data

- Static power: 3.18 pW
- Power at 40 MHz: 2.33 μW (digital buffer as a load)
- CLK-OUT delay: < 1 ns
- Voltage offset:

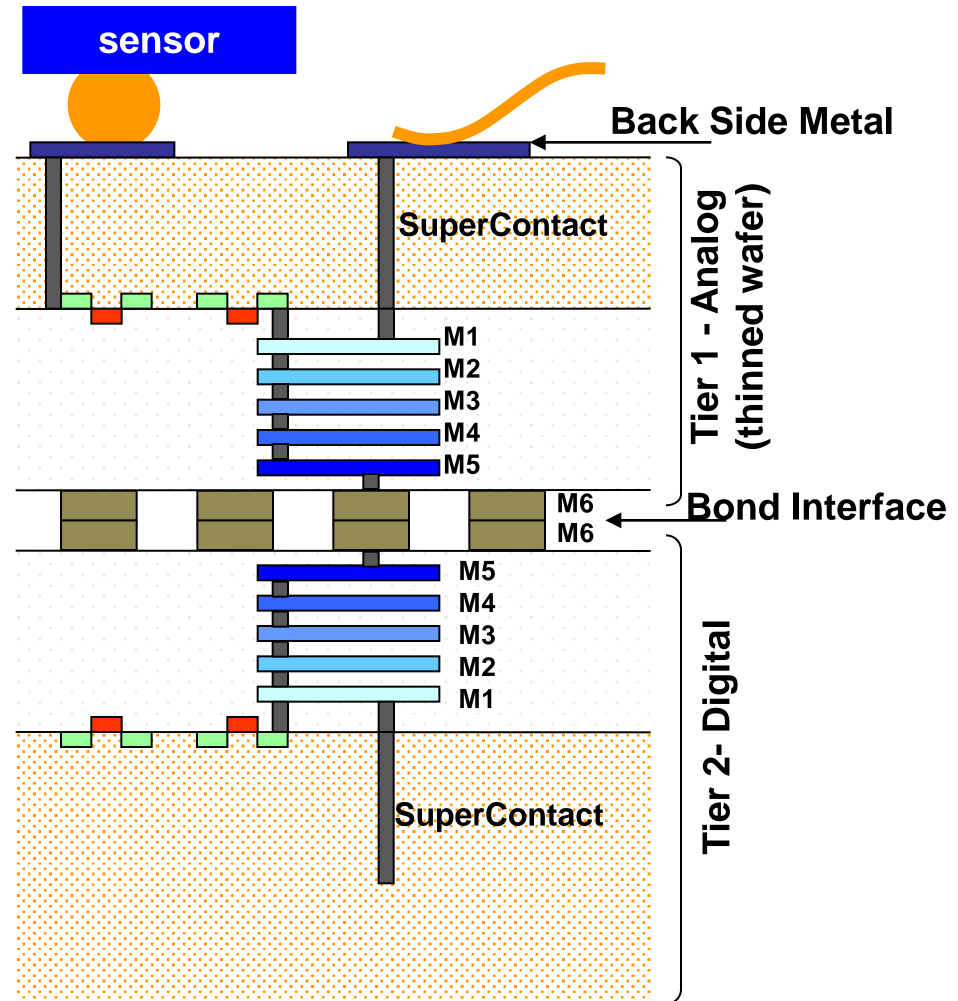
-1.2 mV	at Vref = 500 mV
-12.1 mV	at Vref = 800 mV
-28.2 mV	at Vref = 1000 mV

- Useful voltage range: 300 mV – 1V

  - low limit is given by decision time < 10 ns
  - high limit is given by |voltage offset| < 28 mV

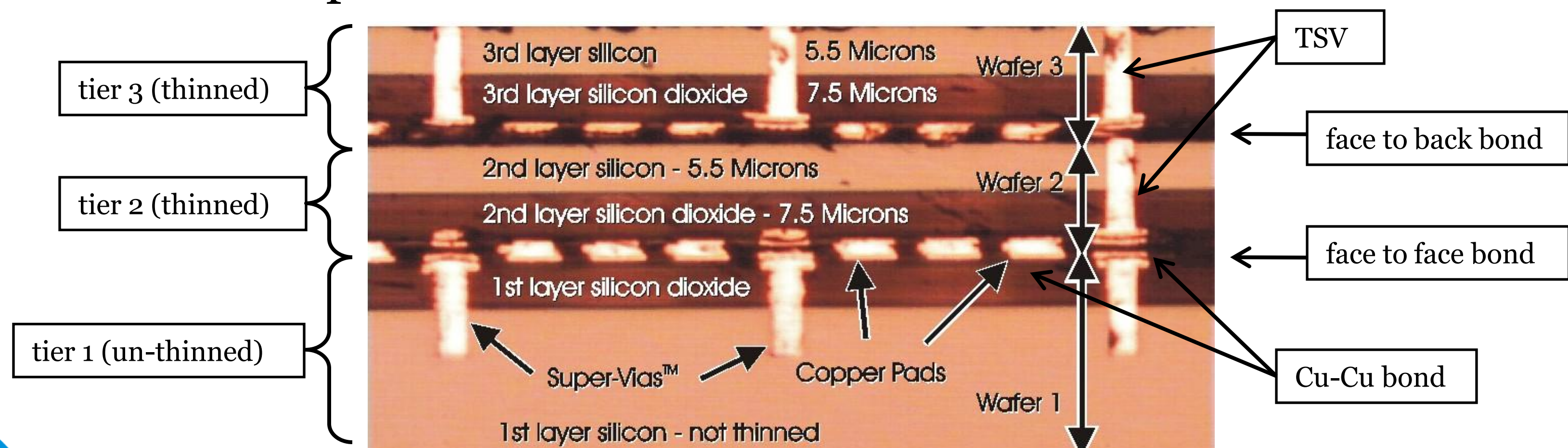
3D TC stack

- Tier 1 is thinned.
- IO of each tier are independent, each tier can be tested stand-alone.
- Digital tier comes in 2 versions.
- In the future, sensor can possibly be integrated tier on top of analog tier ➔ when (/If?) processing mature, very flexible technology with each tier adapted to your application



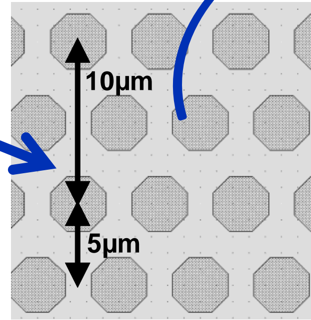
3D technology enablers

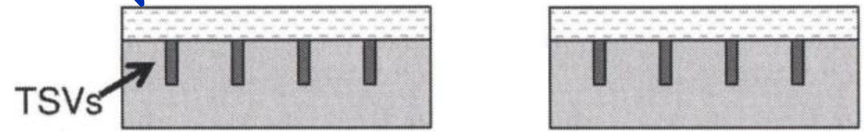
- Through Silicon Via formation, passivation and metallization.
- Wafer thinning: grinding, chemical etching…
  - via has aspect ratio (depth vs. width) □wafer thinning!
- High precision alignment tool: Die to wafer or wafer to wafer.
- Inter-Tier Bonding.
  - face to face / face to back.
  - polymer bonding, SiO2 bond, CuSn eutectic, metal direct DBI, Cu thermocompression…

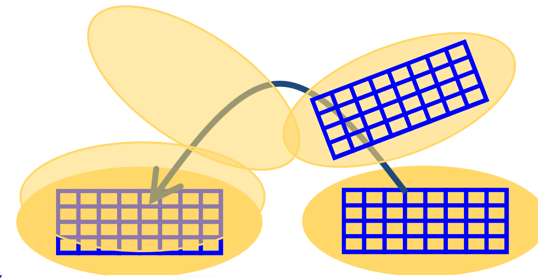


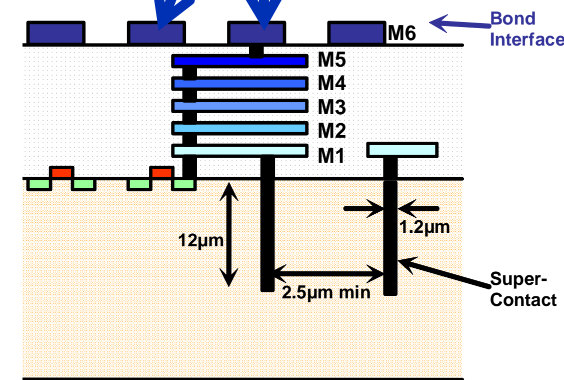
3D Tezzaron foundry process

Each wafer has special interface – "bond interface" - for electrical and mechanical inter-tier connection.



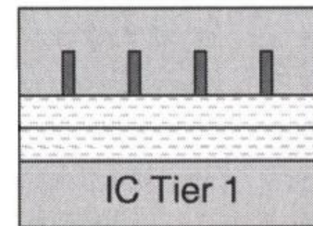






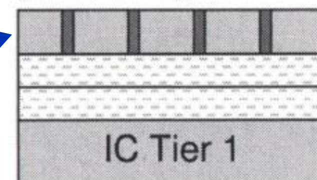
Wafers are placed one on top of another and aligned to match Bond interfaces of both tiers.

2. aligned F2F bonding



3. wafer thinning & backside processing

After bonding top wafer is thinned to 12 μm and diced. Thinning is needed to access TSVs



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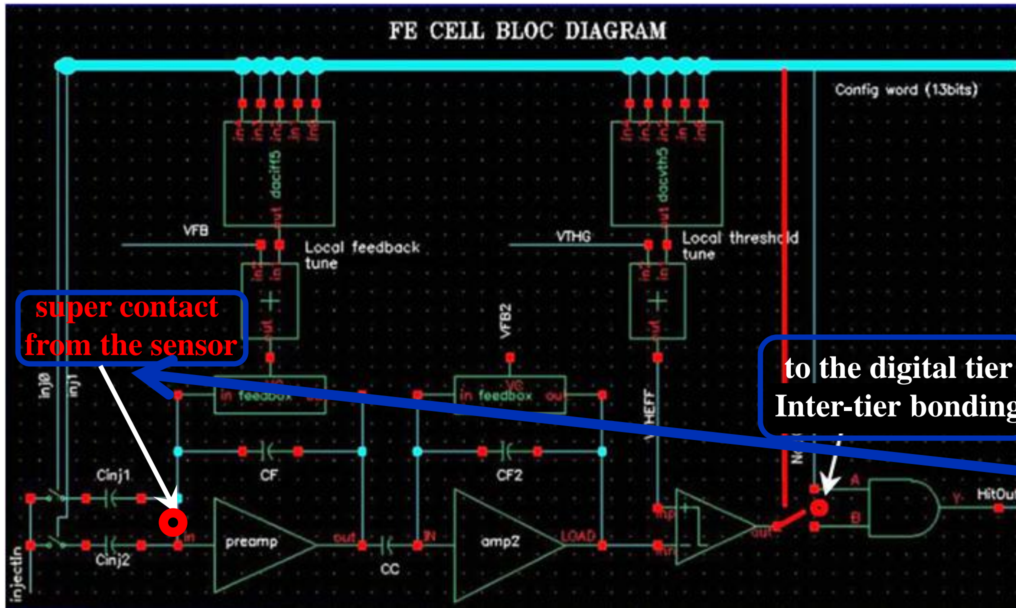
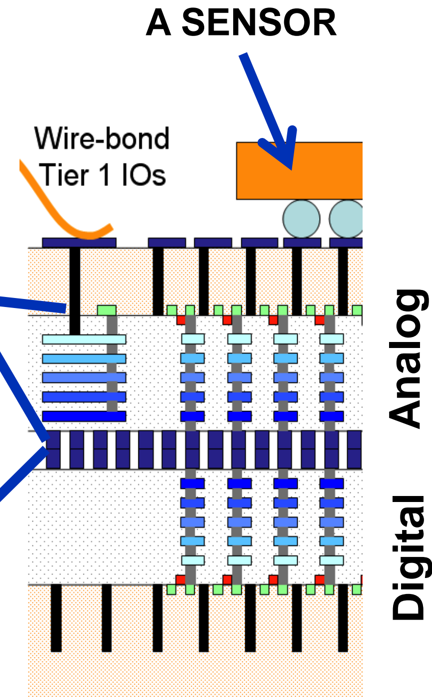
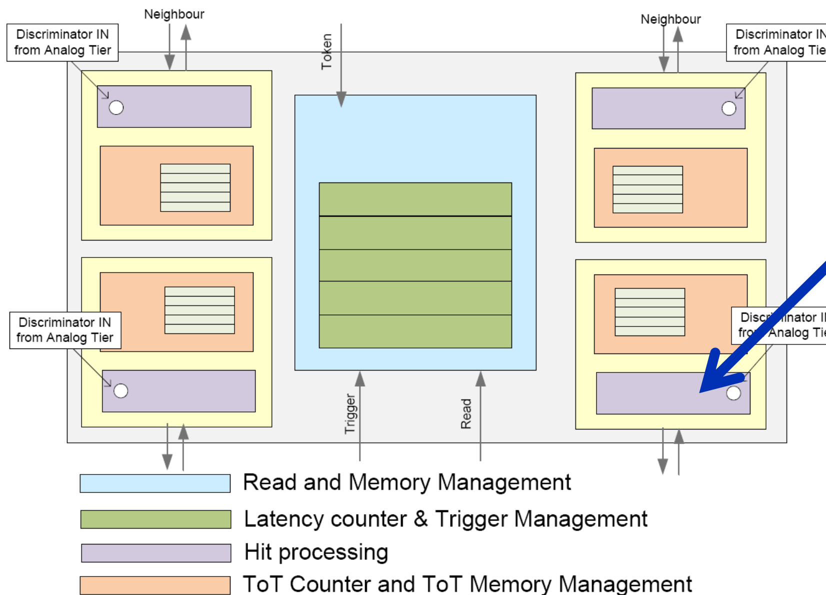
Analog and Digital Tier

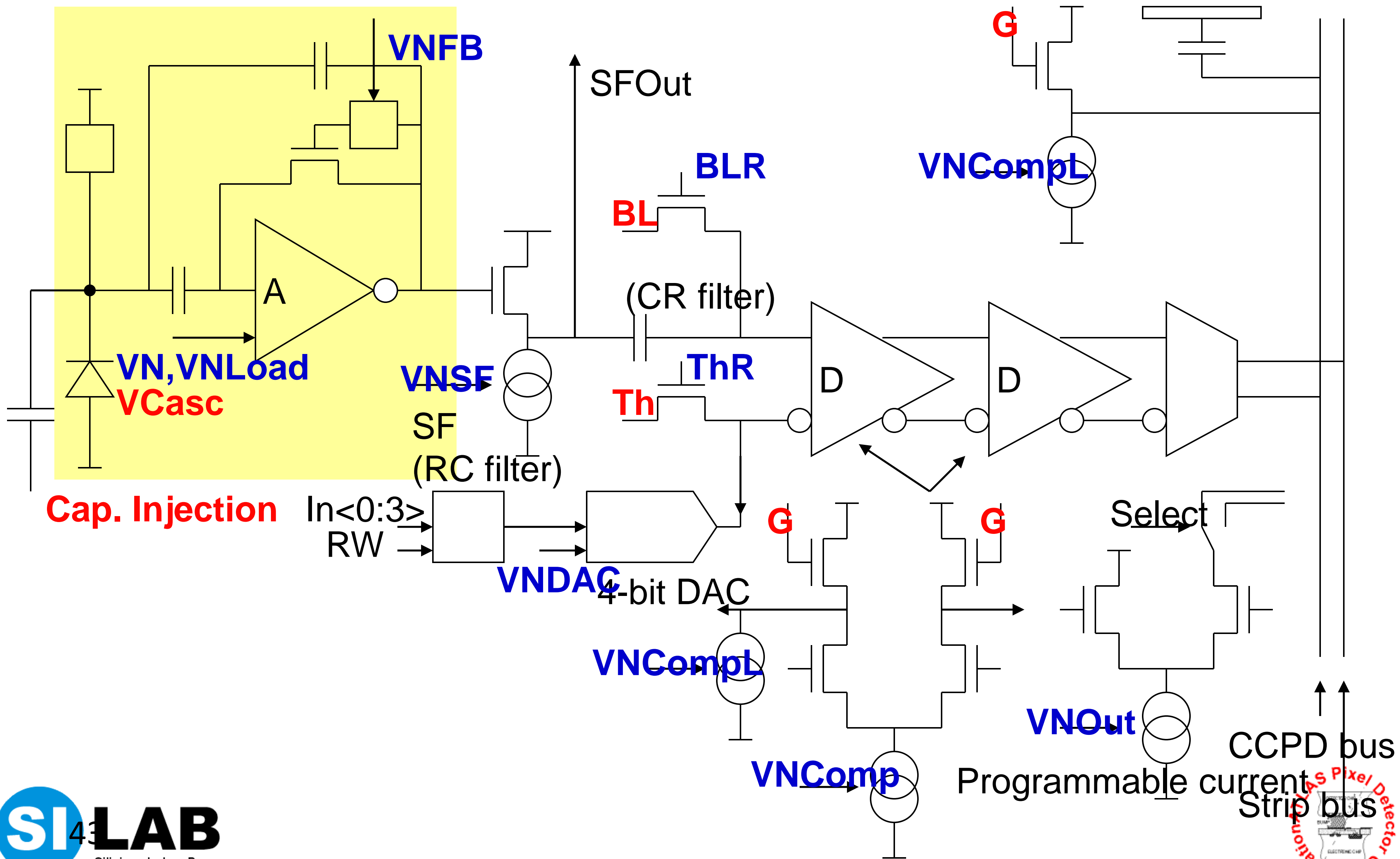




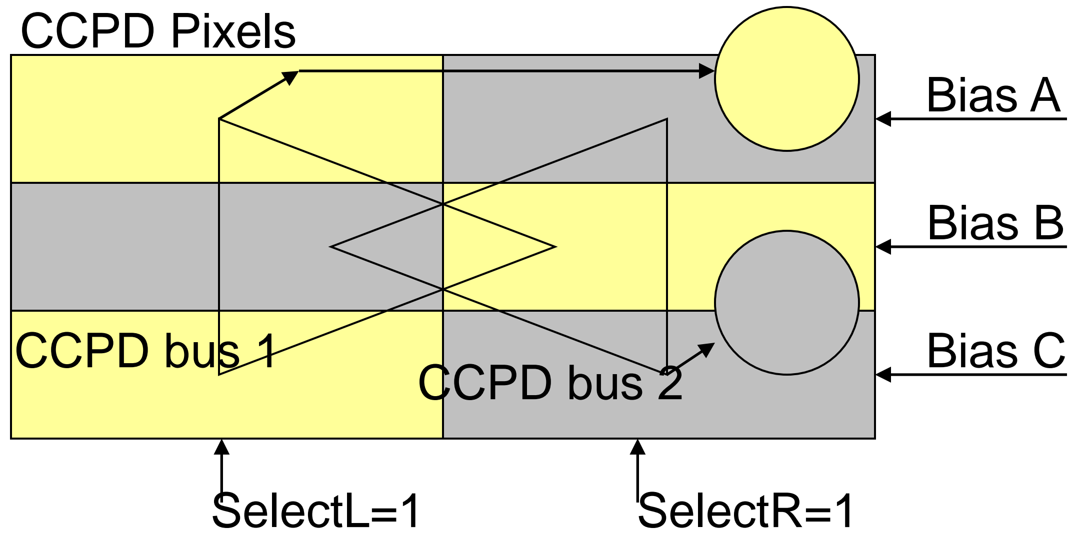


Analog pixel chain and 4-pixel Region derived from FE-I4

Pixel electronics - Normal



CCPD Operation



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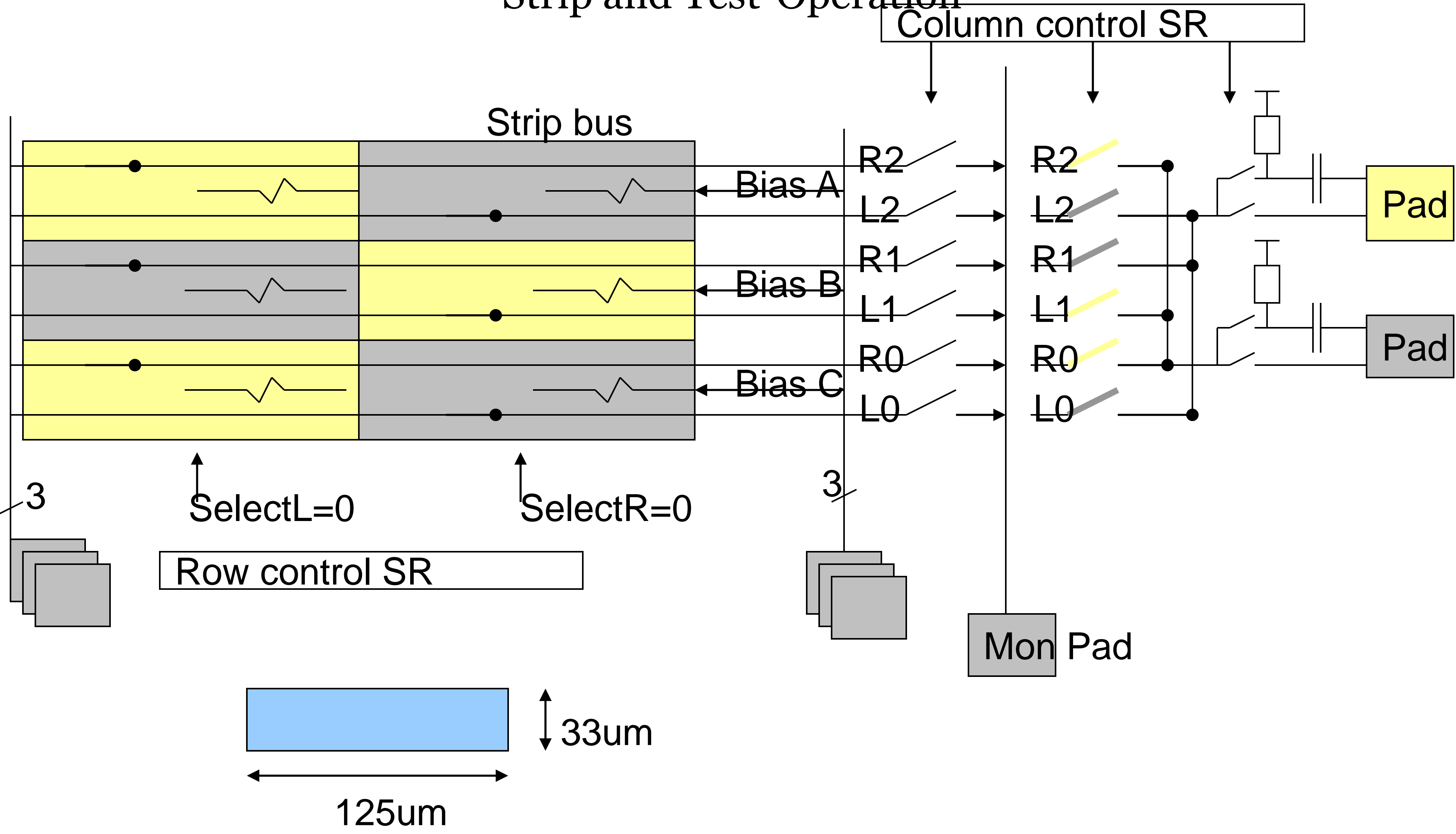
Strip and Test-Operation



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Simulation results

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