ATLAS low mass pixels

M. Barbero, L. Gonella, F. Hügging, H. Krüger, N. Wermes

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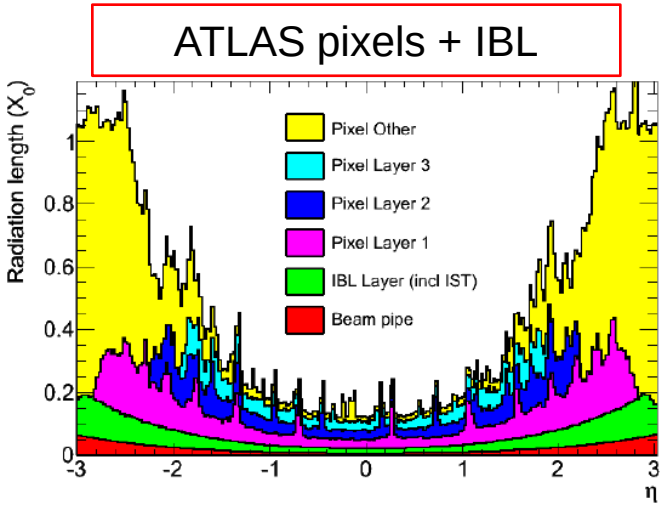
Introduction

- The ATLAS pixel detector @ LHC has a material budget of 3.5% X_0 per layer (*)
  - Modules: 1.0% X_0
  - Cables: 0.5% X_0
  - Mechanics + cooling: 2.0% X_0

- Vertexing and b-tagging require an upgraded pixel detector with lower material budget
  - IBL: 1.5% X_0
  - Target for Phase-I, HL-LHC: 1.0% X_0



(*) All X_0 numbers in the talk are per layer

Material budget reduction

- Different techniques are proposed/investigated to reduce the detector material

- Modules
  - Large thin FE electronics
  - Through Silicon Vias (TSVs)

- Services
  - Novel powering schemes
  - Al flex cables for services design
  - CO^2 cooling

- Mechanics
  - Carbon foam

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- Services
  - Novel powering schemes
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- Mechanics
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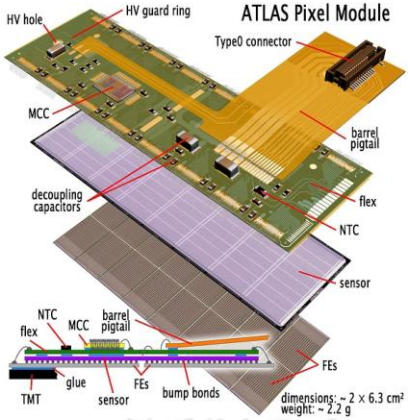
See also:
CO2 Cooling, H. Postema
CF materials, K.-W. Glitza

ATLAS pixel detector modules roadmap

LHC

- Sensor (250µm) = 0.33% X_0
- FE-I3 (190µm) = 0.26% X_0
- Flex + pass = 0.38% X_0
- Pigtail = 0.05% X_0

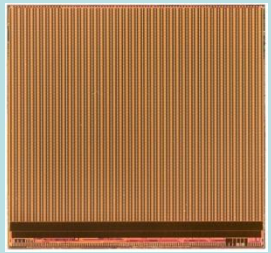
FE-I3
11.1 x 7.4 mm²

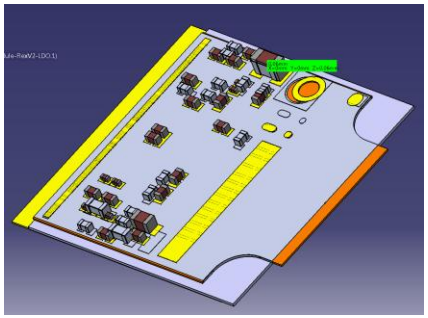


IBL

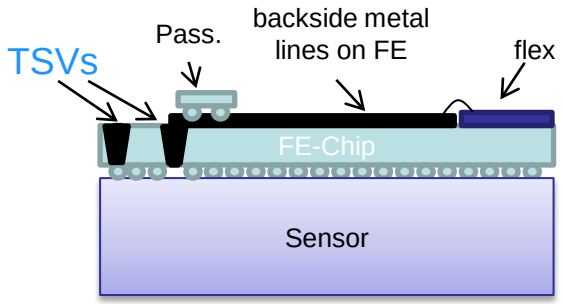
- Sensor (200µm) = 0.25% X_0
- FE-I4 (150µm) = 0.18% X_0
- Flex + pass = 0.27% X_0

FE-I4
18.8 x 20.2 mm²

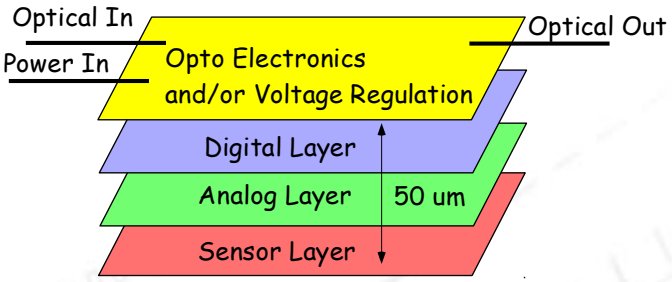




Phase-I & HL-LHC



Full 3D hybrid pixel module

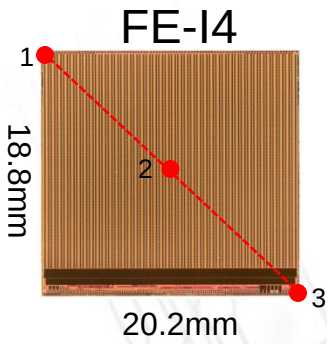


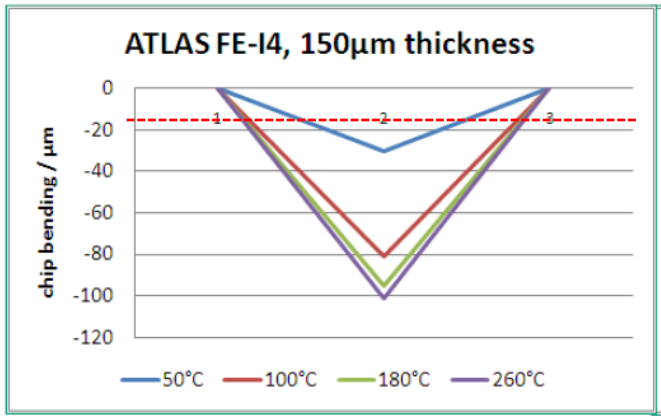
See also: 3D Integration and New Pixel Developments, M. Barbero

~1.0% X_0 ⇒ ~0.7% X_0 ⇒ <0.5% X_0

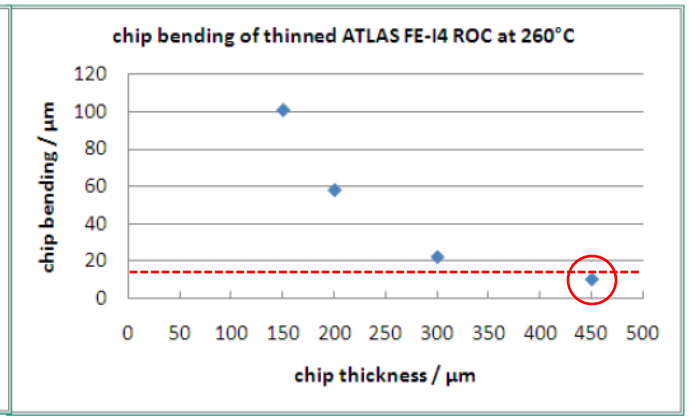
Thin chips: issue with flip chip

- Current flip chip technique: IZM solder SnAg
- During reflow T as high as 260°C
- The chip bends up at the top corners due to the CTE mismatch between metal layers and Si bulk
- Bending >15µm → disconnected bumps
- Required thickness for FE-I4: 450µm → 0.53% X_0 for IBL
  - IBL target: 1.5% X_0
- Need to use a handle wafer during reflow to keep the chip flat





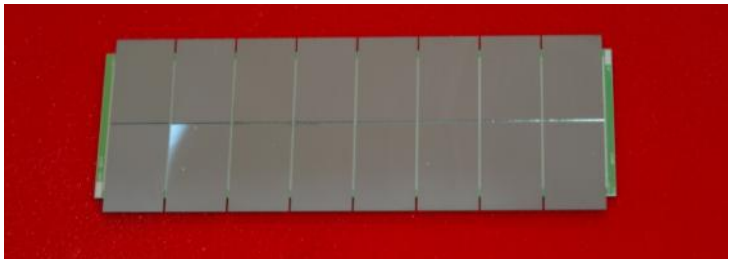
100µm @ 260°C



Chip bending measured on FE-I4 ROCs
Single chips thinned to several thicknesses

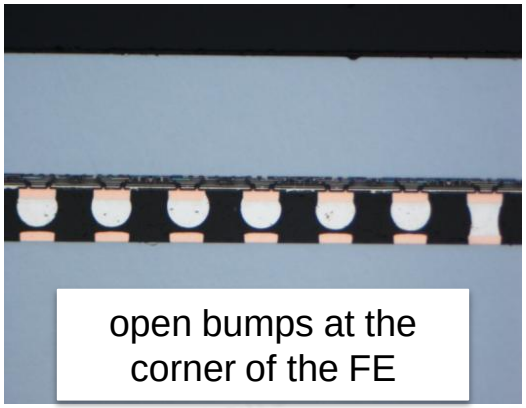
Alternative flip chip methods

- 3 methods tried together with IZM Berlin
  - Wax
  - Brewer glue
  - Polyimide glue



ATLAS pixel module with 90µm thick FE-I2

- Wax and brewer glue
  - Carrier removal is done with moderate heating process
  - Reflow temperatures are enough to partly melt the glue → handle wafer can move during reflow → unconnected bumps at the top corners of the chip

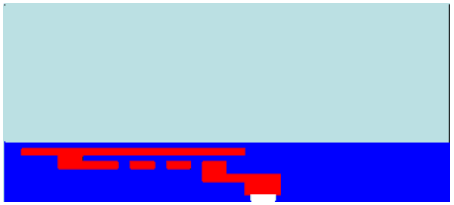


open bumps at the corner of the FE

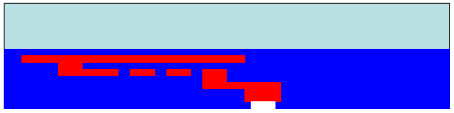
- Polyimide glue
  - Carrier removal is done via laser exposure (glass carrier used)
  - Reflow temperatures do not dessolve the glue → no bumps disconnected!

Selected to build IBL modules with thin (≤150µm) FE-I4

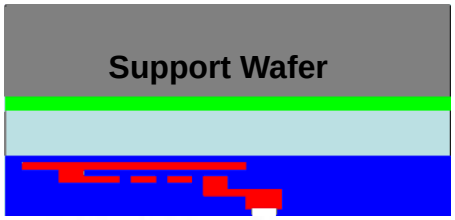
Thin chip modules – Process flow



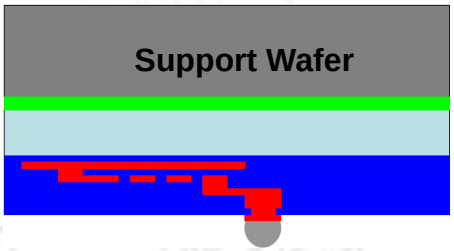
ROC
Wafer



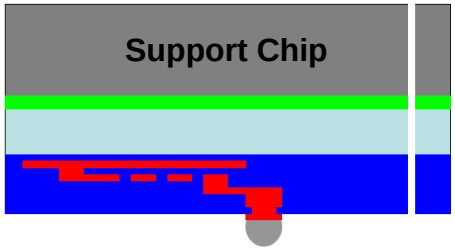
Wafer
Thinning



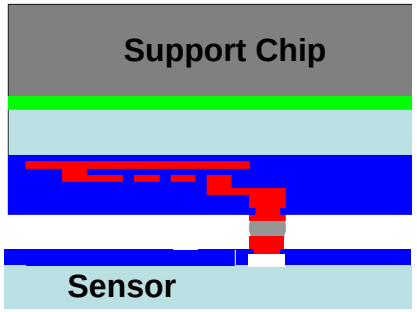
Temporary
Wafer Bonding
to support wafer



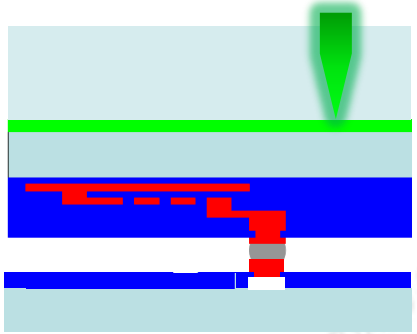
Contact
formation
(Micro-
Bumping)



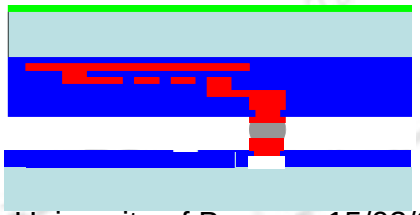
Dicing of Wafer
Stack



Bump Bonding



Laser exposure



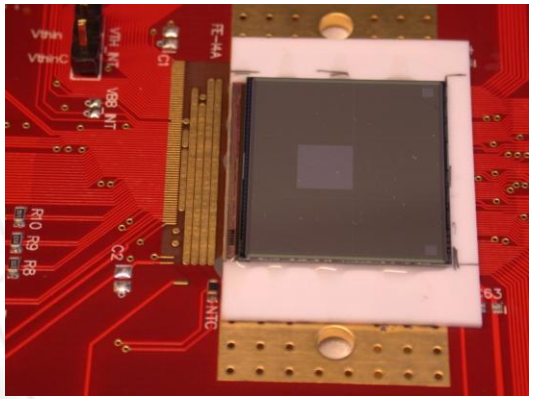
Support Chip
Release

IBL modules

- IBL pre-production modules
  - Sensor: 3D (single chip), planar (single and double chip)
  - FE-I4: 100µm, 150µm
  - Flex

- Electrical and mechanical tests demonstrated
  - Success of new flip chip method
  - No damage due to carrier removal, handling, thermal cycling

Module on SCC

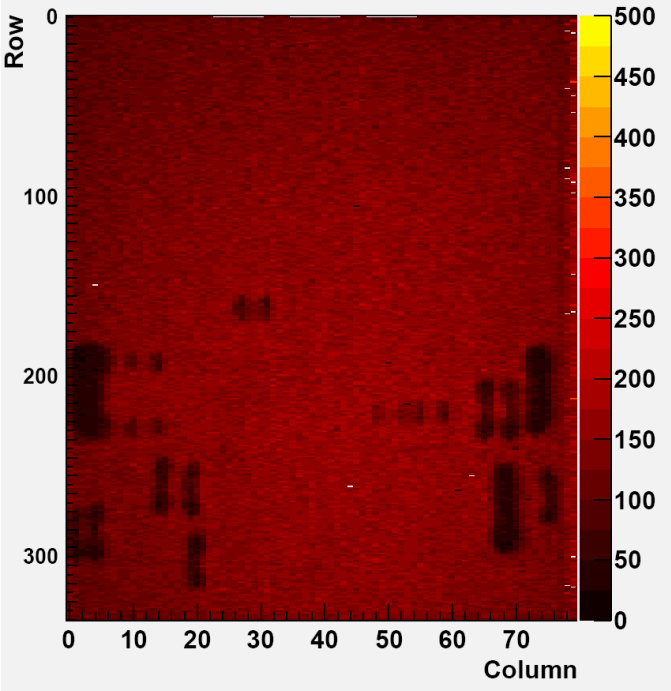


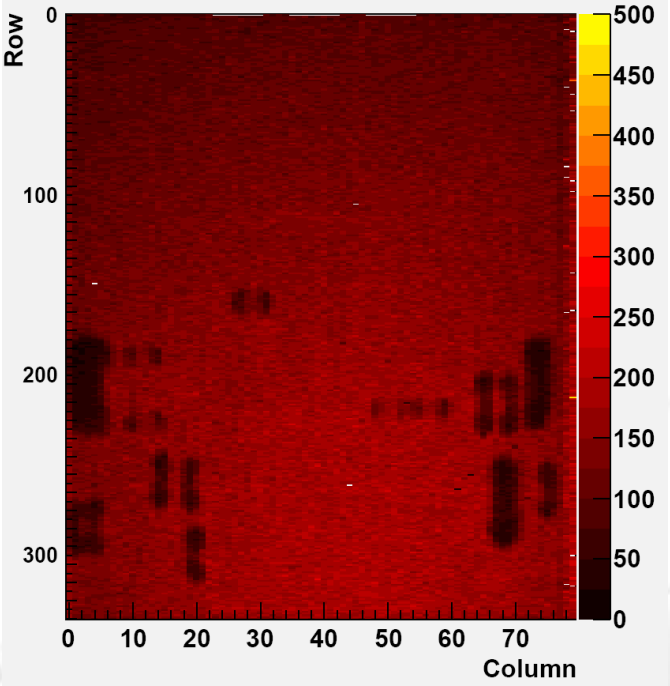
"Dressed" module

IBL modules: source scan results

Dressed module: planar, single chip, 150µm thick FE-I4

- Before thermal cycling
  - All pixels connected
    - Dark spots = passive comp on flex
  - No damage due to wafer removal and handling
- After 10 thermal cycles
  - -30ºC - +30ºC
  - No pixels disconnect during thermal cycling





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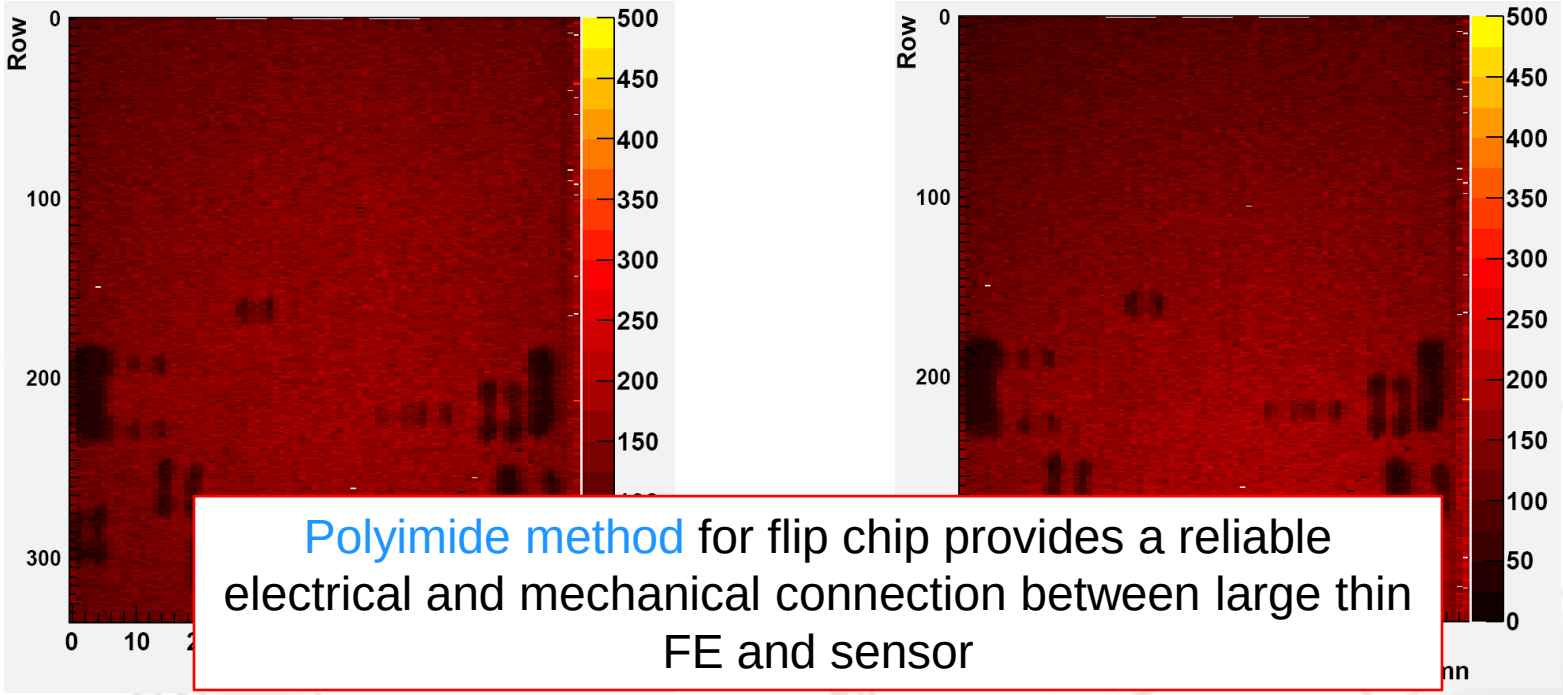
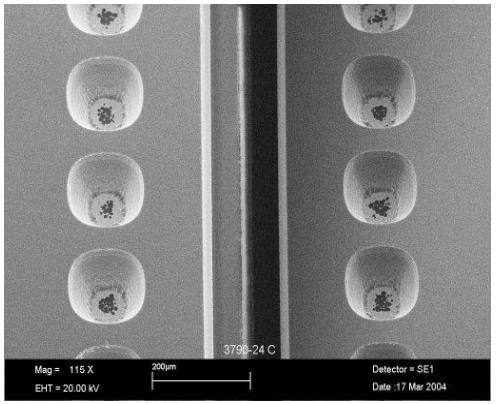
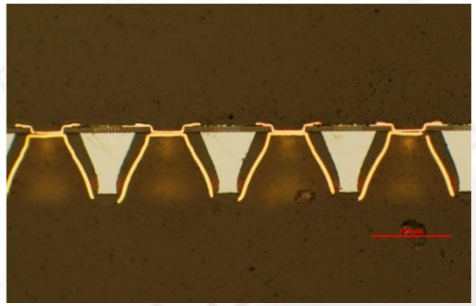


Polyimide method for flip chip provides a reliable electrical and mechanical connection between large thin FE and sensor

TSVs for hybrid pixel detectors

- UBonn started TSV (vias last) development with IZM three years ago based on FE-I2/3 (ATLAS Pixel) readout electronics:
  - IZM offers two TSVs processes: tapered side wall and straight side wall TSVs
  - IZM integrates the TSV process into the bump bonding process (make TSVs first and afterwards do BB)
  - We profit from ultra thin (< 100µm) flip chipping (developed for bumped FE-I4 chips for the ATLAS IBL)





- Status
  - Tapered and straight side wall TSVs tested on ATLAS readout and monitor wafers

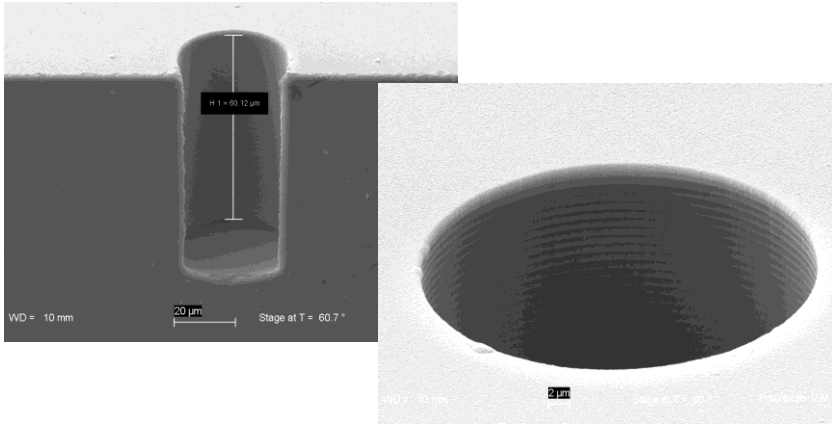
    → both processes work
  - Batch of 2 FE-I2 ATLAS wafer have been processed:
    - 1 wafer without bump bonding to test the TSV alone → finished, bare chips available
    - 1 wafer with bump bonding to ATLAS pixel sensors → finished, modules available

Straight and Tapered Side Wall TSVs

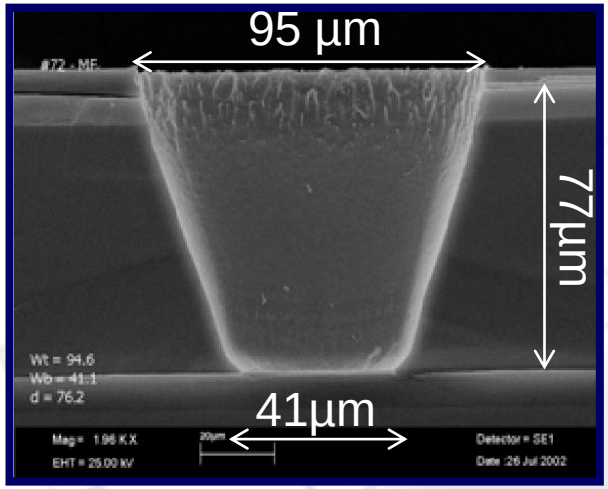
- Straight side wall TSV
  - Bosch process
  - Aspect ratio 2 – 5:1
  - Max Si thickness: 100 – 150µm

- Tapered Side Wall TSV
  - Vias are etched in one step and oxide is deposited after etching
  - Simpler deposition process of isolation layer using thin film polymers
- Tapered walls
  - Side angle 72°
  - In this example
    - Via diameter on the bottom: 41µm
    - Via diameter on the top: 95µm
    - Si thickness: 77µm
  - 150µm pad size (FE-I2) → 100µm max Si thickness

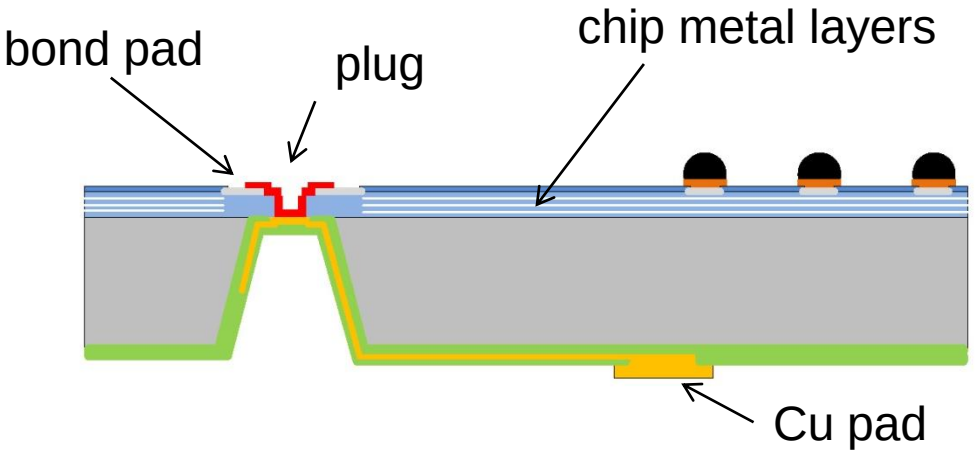
Straight side wall TSVs on monitor wafer



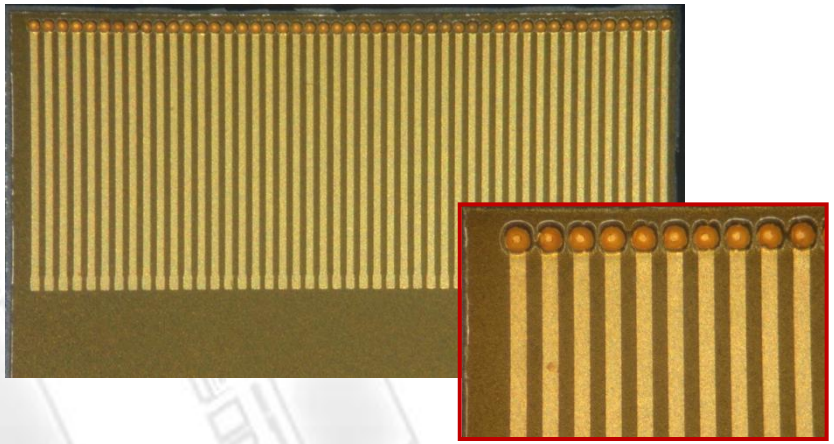
Tapered side wall TSVs on monitor wafer



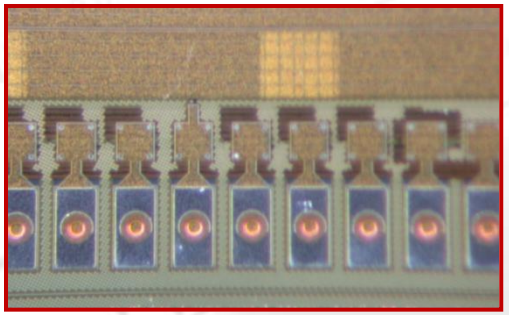
Tapered TSV for ATLAS Pixel FE-I2/3



- Backside processing
  - Thinning to 90µm
  - Silicon Via etching (tapered)
  - Passivation
  - Cu depostion
  - Re-Distribution Layer (RDL)



- Frontside processing
  - Cu pad to bond pad interconnect (plug)
  - Bump deposition
  - Dicing

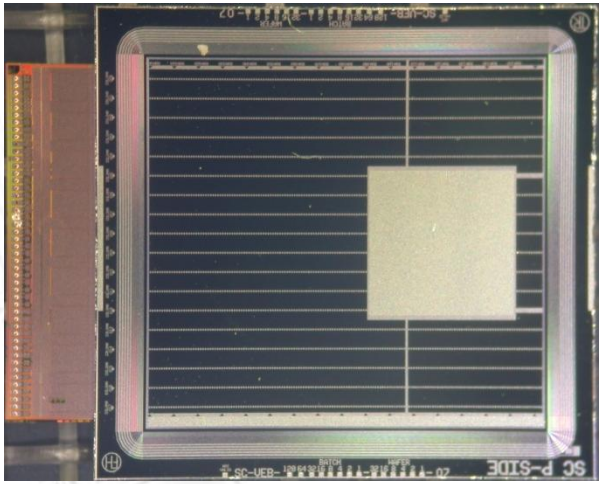


Tests: TSV modules

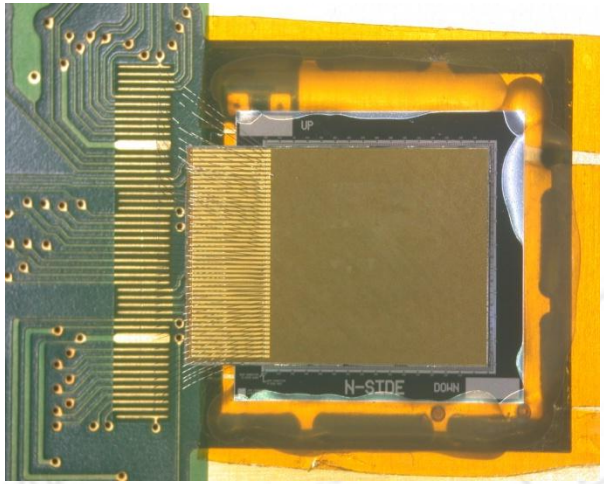
- Built 16 modules with
  - FE-I2 chips (wafer map available), 90µm thick, with tapered TSV and RDL
  - Planar n-in-n sensor

- 2 modules mounted on boards for electrical tests
  - Both modules work fine

Module front side



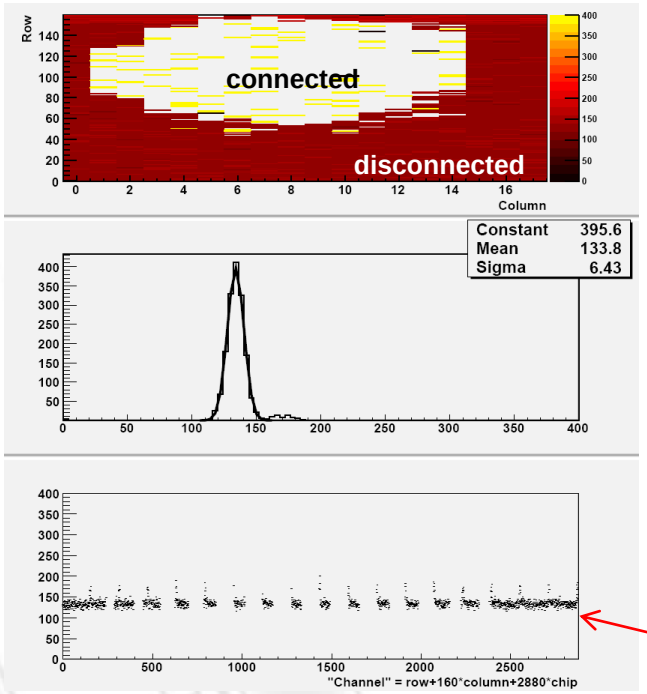
Module on board



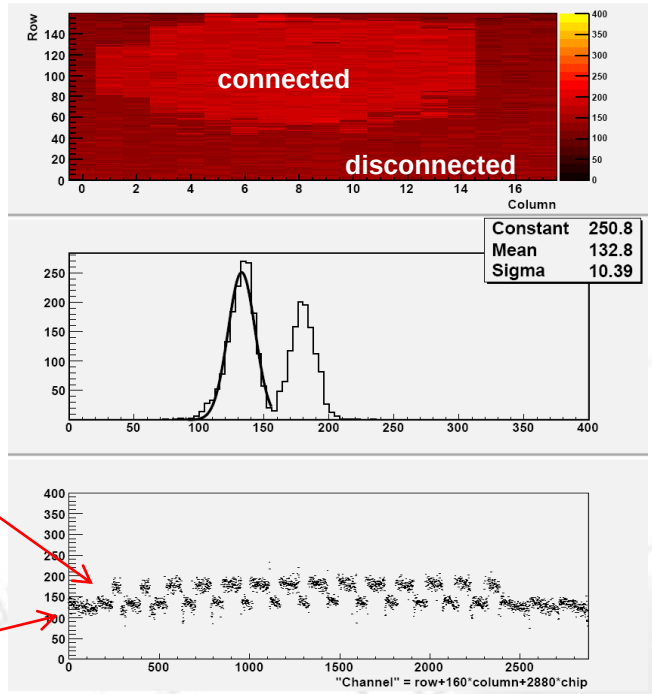
Tests: TSV module: wire bonds on backside (i.e. TSVs used for operation)

- Modules operated via TSV and RDL
- Noise measurement with and without HV shows disconnected pixels
  - Expected, the old flip chip method was used (i.e. no handle wafer during reflow)
  - For disconnected pixels the noise stays the same indep. of HV
- Module works fine → no indication of extra noise

Noise map, No HV



Noise map, HV = -80V

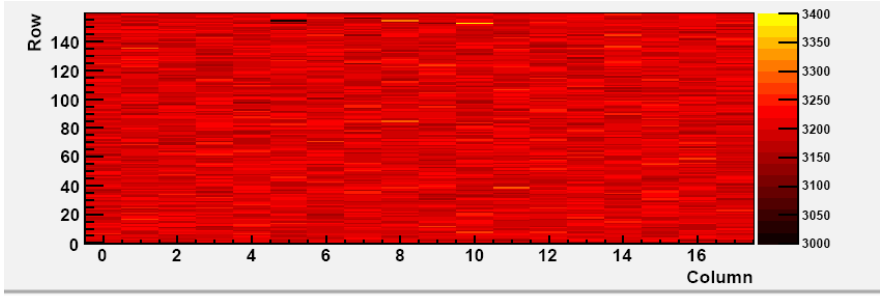


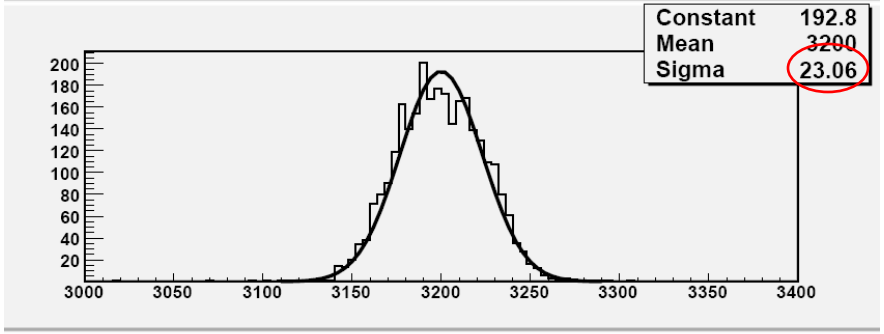
Connected pixels: **~180e**

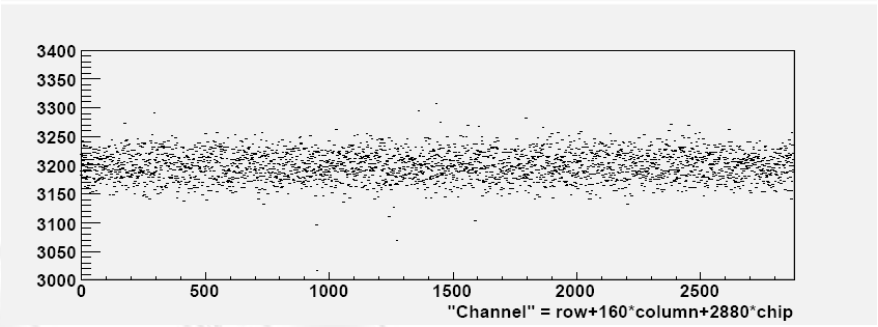
Disconnected pixels: **~130e**

Tests: TSV module: wire bonds on backside (i.e. TSVs used for operation)

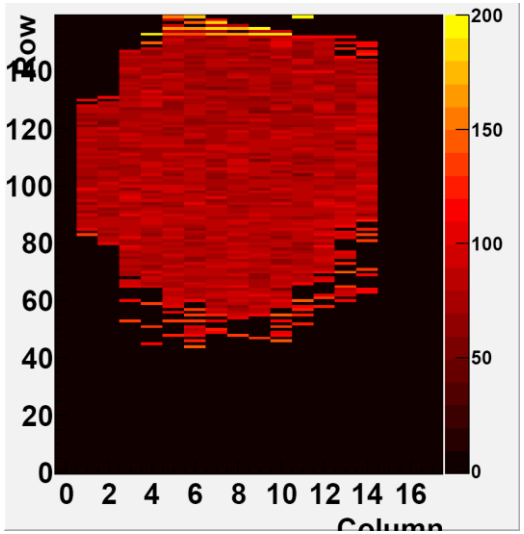
- Threshold tuning to 3200e

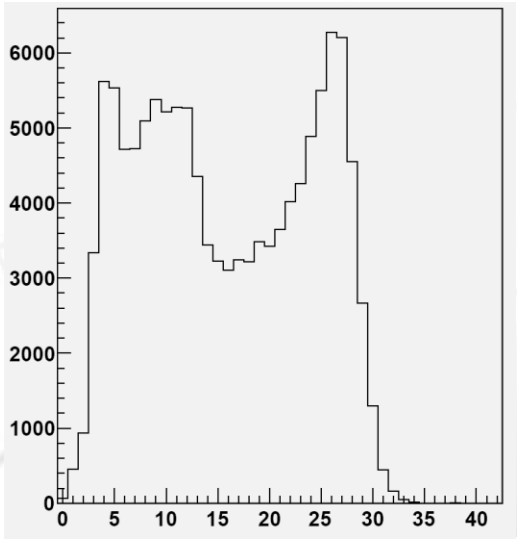






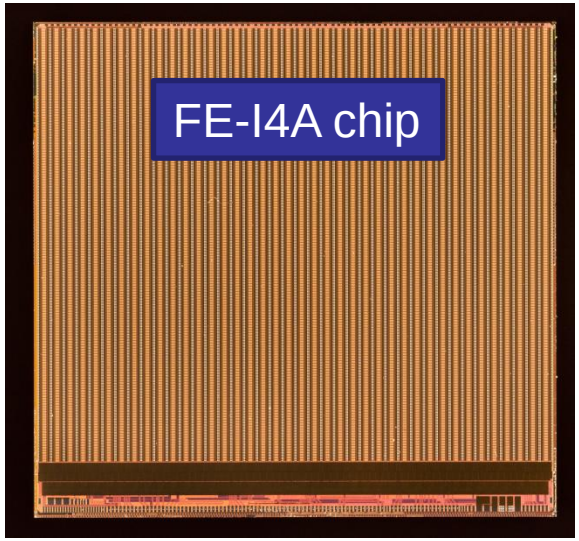
- Source scan with an Am-241 source

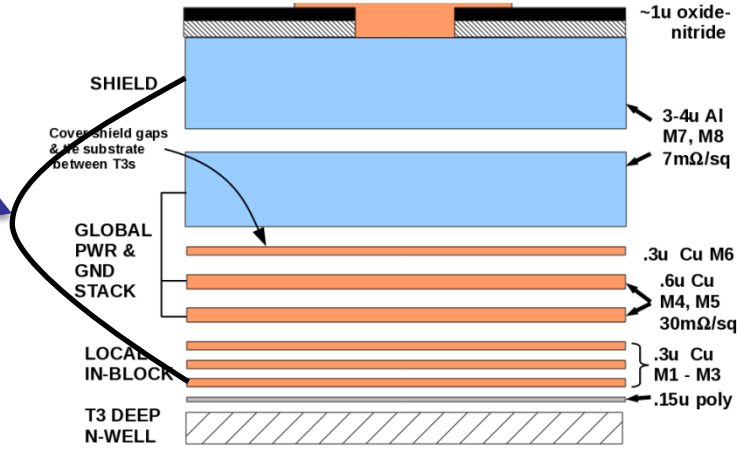




Immediate plan: FE-I4A modules with TSV i.e. chip plus sensor

- Next steps are to use a FE-I4A chip using the same process:
  - 6 times larger than FE-I2/3 but thickness must be 90µm (note: IBL chips have 150 µm)
  - Use thin flip chip method currently developed for IBL modules
  - Wire bond pads are already prepared for TSV usage:
    - Half of the pad is ‚empty' in BEOL layers
    - Top metal layer of the pad is connected to the first metal layer
    - No frontside processing needed
  - 3 FE-I4 wafers foreseen for the processing at IZM
    - 3 - 6 months process time at IZM, including bump bonding to sensors





FE-I4 BEOL layer stack

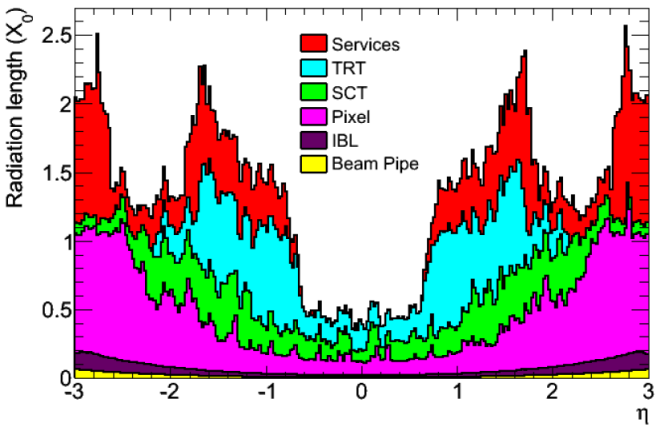
Light services

- Trackers services at LHC
  - Dominate the material budget at large η
  - Saturate cable channels
- Main contribution: power cables
  - ATLAS pixel detector: direct power, 8 cables/modules, 1744 modules

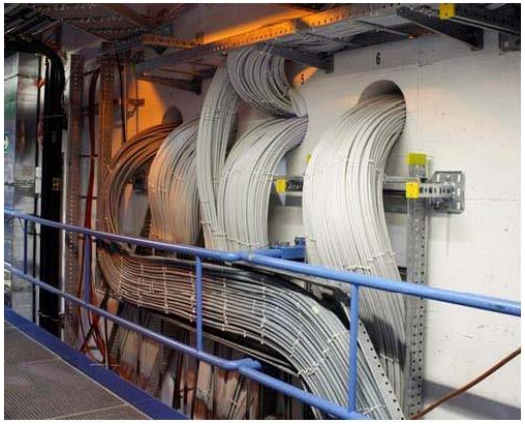
- Situation can get even worse for upgraded trackers
  - Higher FE I consumption, higher granularity → higher cable volume
  - Same cable channels

See also: Novel Powering Schemes, K. Klein

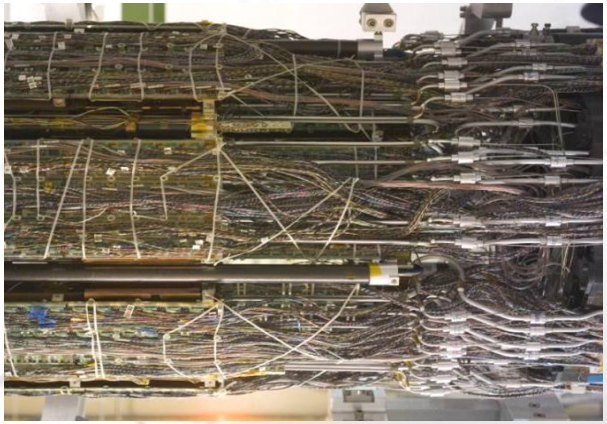
ATLAS inner detector: X0 vs. η



ATLAS Inner Det. Cables



ATLAS pixel detector services



Light services

- Trackers services at LHC
  - Dominate the material budget at large η
  - Saturate cable channels
- Main contribution: power cables
  - ATLAS pixel detector: direct power, 8 cables/modules, 1744 modules

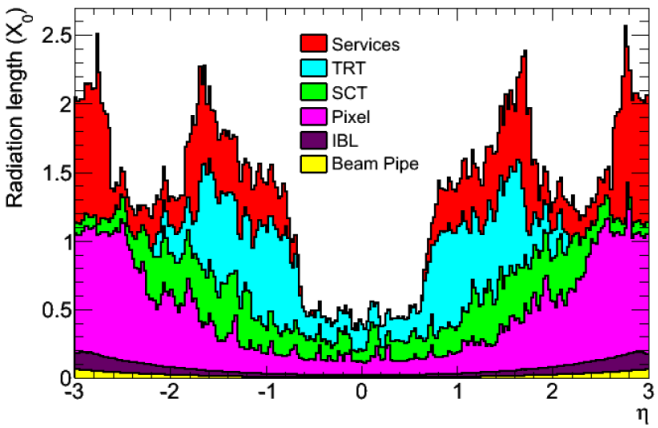
- Situation can get even worse for upgraded trackers
  - Higher FE I consumption, higher granularity → higher cable volume
  - Same cable channels

See also: Novel Powering Schemes, K. Klein

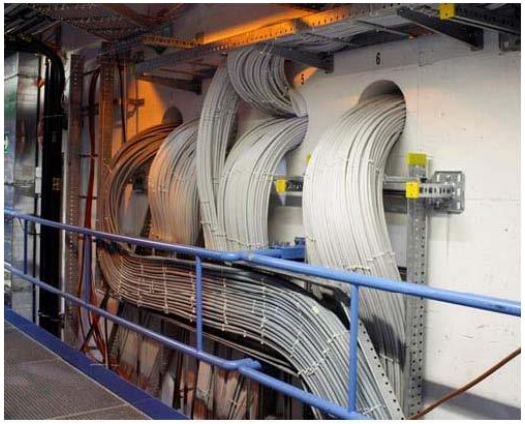
Light services for upgraded trackers:

- Novel powering schemes (serial powering, DC-DC conversion): low I, high V
- Use Al instead of Cu for cable design

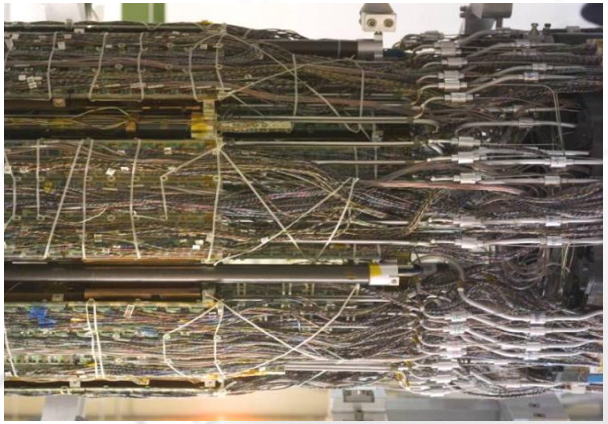
ATLAS inner detector: X0 vs. η



ATLAS Inner Det. Cables



ATLAS pixel detector services

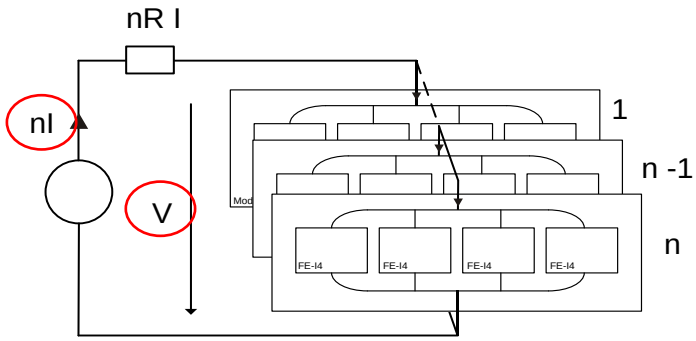


Serial powering: material reduction

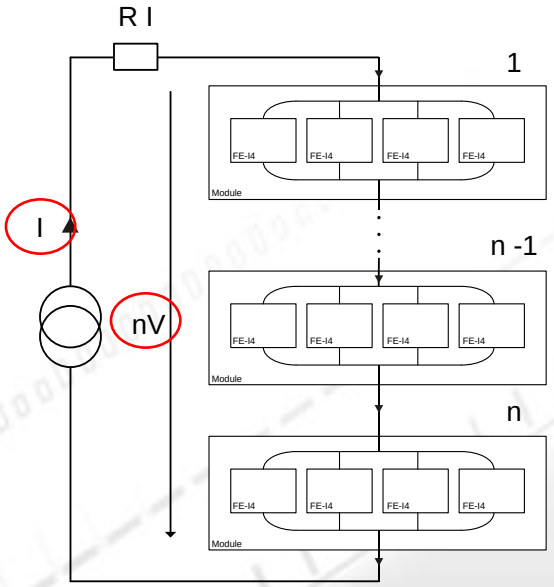
Cable x-section: $A \ \alpha \ \frac{I}{V_{drop}}$

- SP is a current based power distribution scheme that aims at reducing the transmitted current wrt to a conventional voltage based powering scheme:
  - $nI_{mod} \rightarrow I_{mod}$: A scales of a factor n
- Same current scaling factor could be obtained in a voltage based powering scheme with DC-DC conversion if conversion factor m=n

Parallel powering



Serial powering



Serial powering: material reduction

$$\text{Cable x-section: } A \;\alpha\; \frac{I}{V_{drop}}$$

- Further material reduction, SP specific
  - Differently from a voltage based powering scheme, the V_{drop} is limited only by the power density and the I source output voltage capability

    → a higher V_{drop} can be allowed in areas where the amount of material/space to fit the cables is critical to further reduce A

- Voltage based powering scheme
  - Need to prevent damage to the module during transients on the LV lines
  - Max V_{drop} on the LV lines between V source and the module is constrained
  - $V_{drop} \leq V_{max} - V_{nom}$ (V_{nom} = nominal operating module voltage, V_{max} = max V the chip module can sustain)

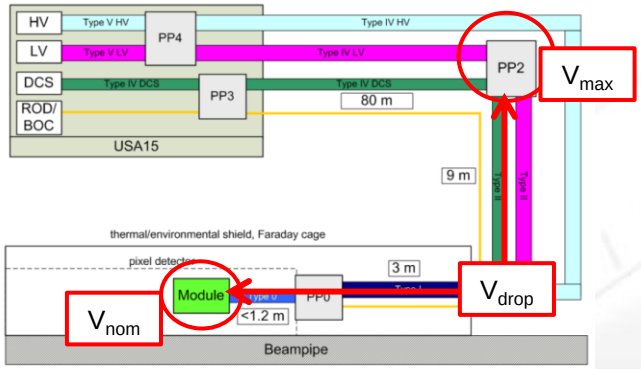
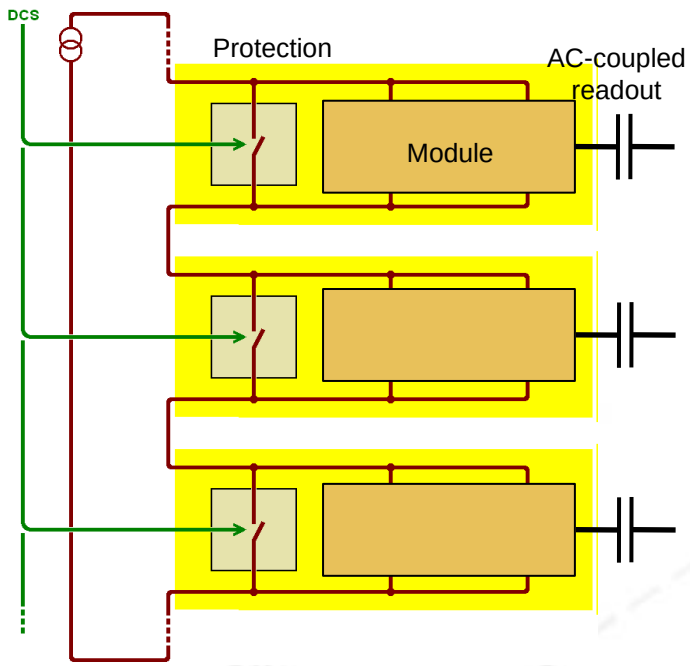


Figure 3.21: Simplified schematic view of the layout of the services for the pixel detector.

Serial powering: system aspects

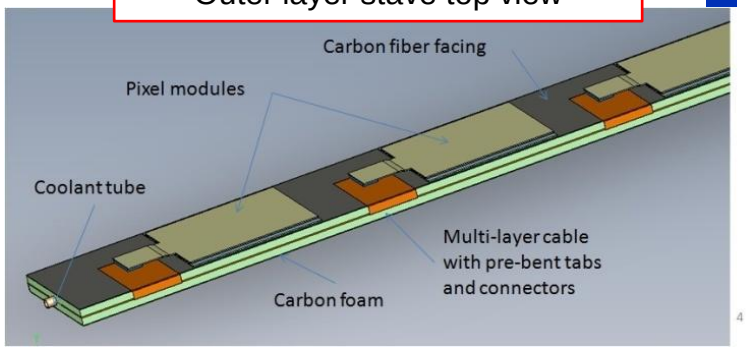
- At system level, a SP scheme requires some dedicated features
  - AC-coupled data communication
    - Modules have a different gnd potential
    - Widely used in telecommunication
  - Protection to avoid loosing all modules in a chain if one fails
    - Slow ctrl from the DCS to switch ON/OFF selected modules
    - Fast response against over-voltage
    - Non trivial:
      - When ON (mod OFF), low power density
      - When OFF (module ON), protection draws no power
      - Low material & rad hard
  - HV distribution
    - Should be designed to avoid shorting the SP chain
    - Should guarantee same HV to all modules



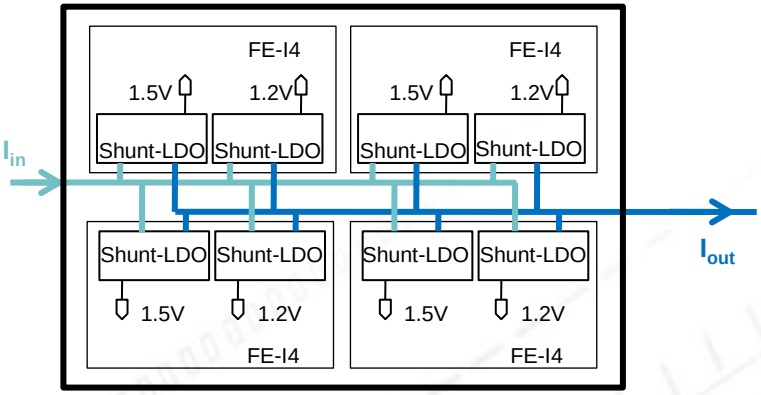
SP for the ATLAS pixels

- Conical layout, outer layers → SP chain of 8 modules
- On stave → I flows from module to module
- On module → I splits in parallel between the chips
- On chip → I to V conversion: Shunt-LDO regulator integrated in FE-I4 (no extra material!!!)

Outer layer stave top view



Current distribution on module



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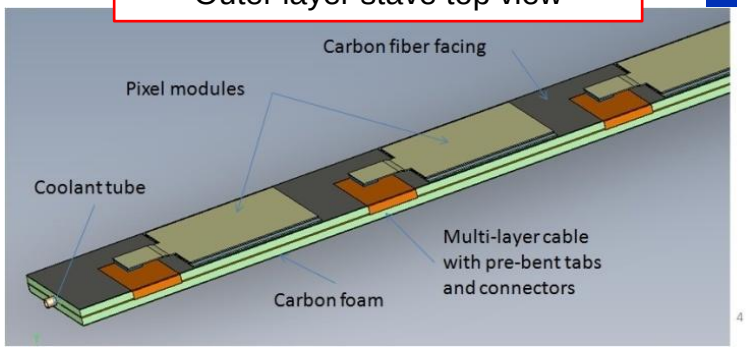
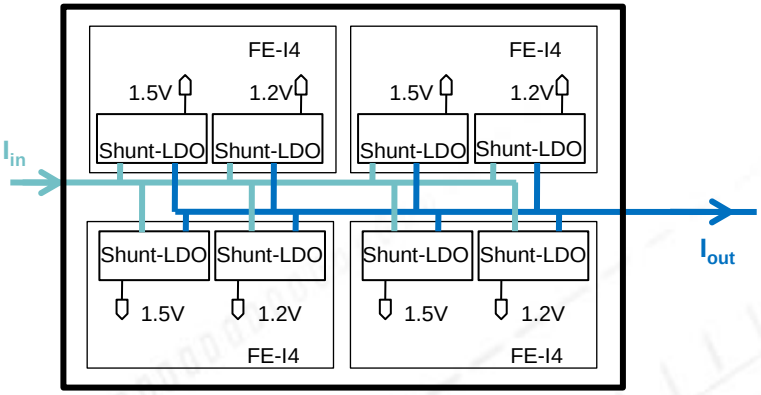


Current distribution on module



Direct power vs SP: X_0 on stave

Direct power

For V_{drop} = 0.2V on stave

→ P_{eff} = 88% (on stave), Al = 0.180% X_0

SP

For a P_{eff} = 88%

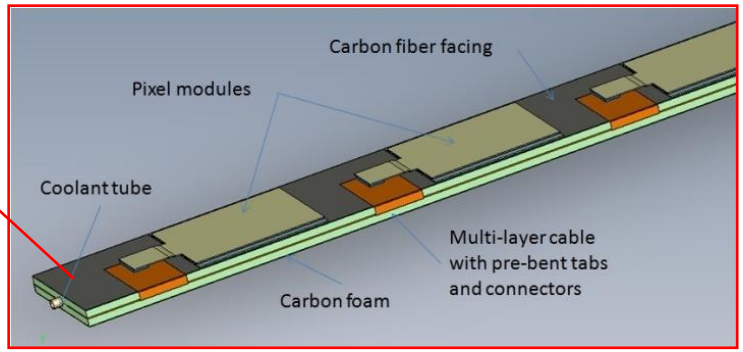
→ Al = 0.006% X_0

extra (AC-coup, prot) < 0.010% X_0

X_0 reduced of a factor 30 in active area!!!

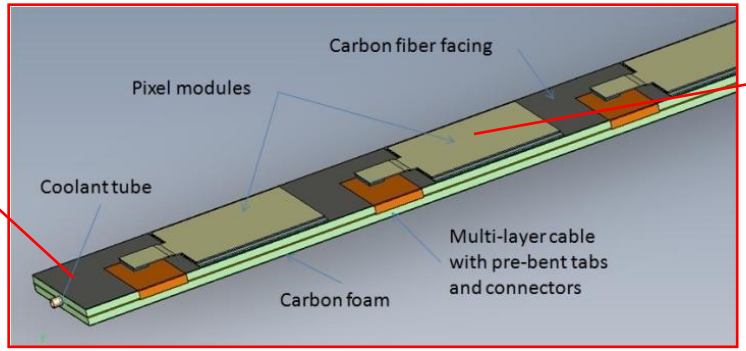
(at large η it can be even higher!)

SP stave prototyping



- Stave + multilayer cable for SP
  - Al layer for power
  - Cu multilayer for signals
  - Al layer glued on Cu layer, connection via TAB bonding

SP stave prototyping



- Stave + multilayer cable for SP
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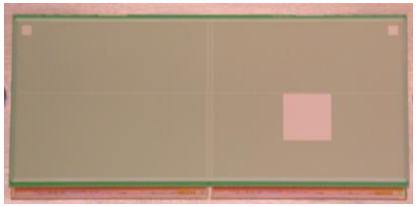
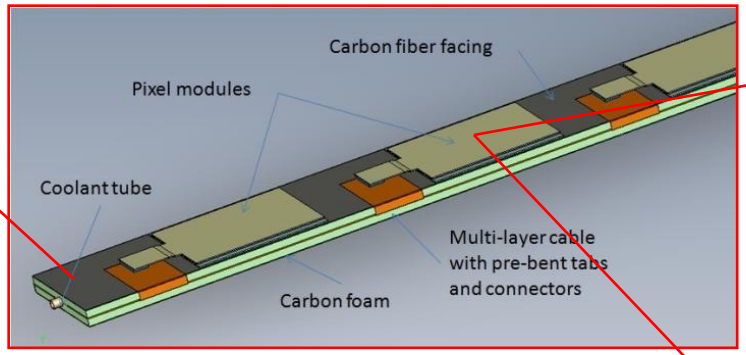
- 4-chip FE-I4 modules
  - Not yet available
  - For this 1st SP stave prototype use 2-chip FE-I4A modules



SP stave prototyping



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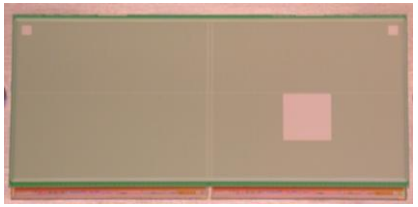
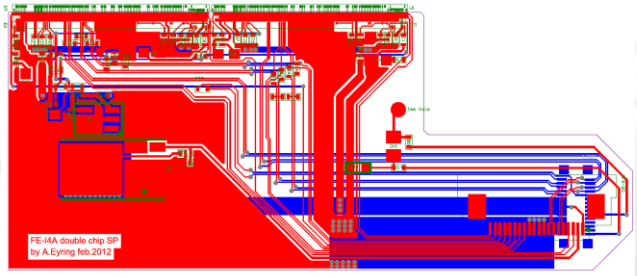
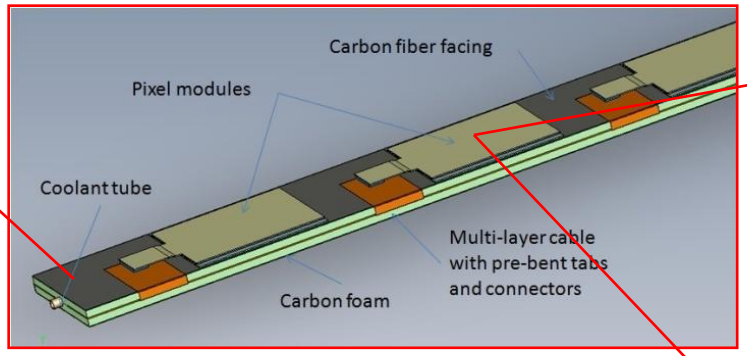


- Stave + multilayer cable for SP
  - Al layer for power
  - Cu multilayer for signals
  - Al layer glued on Cu layer, connection via TAB bonding

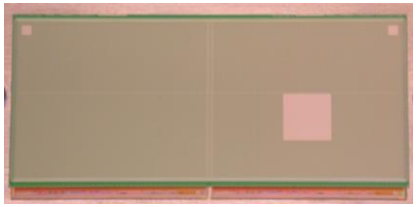
- Module flex for 2-chip FE-I4A modules
  - Received last week, passives being soldered
  - Features
    - AC-coupling for clk and cmd lines
    - HV distribution scheme for SP
    - Vref generation for Shunt-LDO (not integrated in FE-I4A)
    - Commercial OV protection



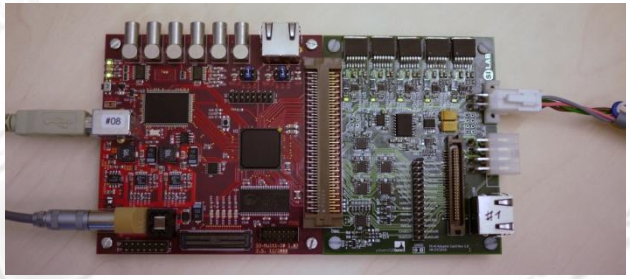
SP stave prototyping



- 4-chip FE-I4 modules
  - Not yet available
  - For this 1st SP stave prototype use 2-chip FE-I4A modules



- Stave + multilayer cable for SP
  - Al layer for power
  - Cu multilayer for signals
  - Al layer glued on Cu layer, connection via TAB bonding
- Readout: USBPix
  - New adapter card
  - Cfg 4 chips at the same time
  - Read back one chip at a time



- Module flex for 2-chip FE-I4A modules
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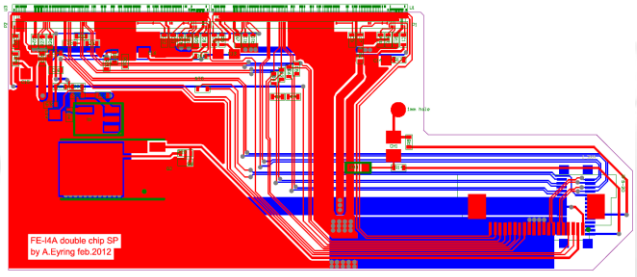
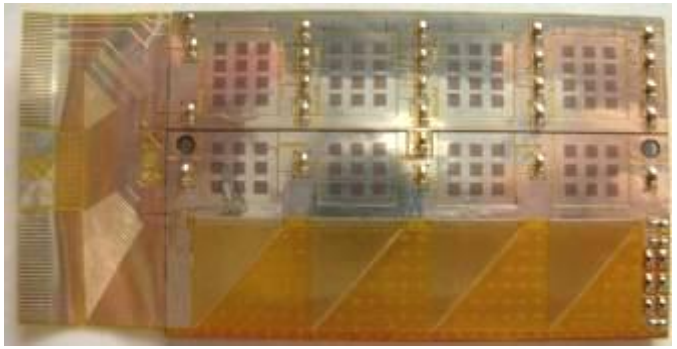


Aluminum flex technology

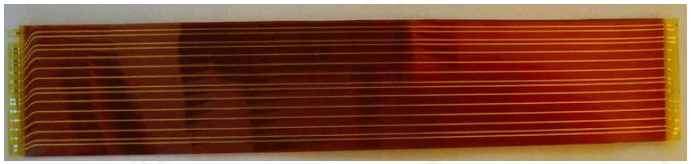
- Proposed an alternative design for the IBL detector services with this technology
  - Baseline: multilayer Cu-Al flex with wings
  - Alternative: laminated stack of single sided Al flex with wings

ALICE SSD hybrid flex



- UBonn investigated an aluminum flex technology to design services for the upgrades of the ATLAS pixel detector
  - Low material solution
  - Mechanical flexibility & electrical robustness
- Technology choice: full aluminium “chip on flex” technology from SE SRTIIE, Ukraine
  - Already in use in the ALICE Silicon Strip detector (SSD)

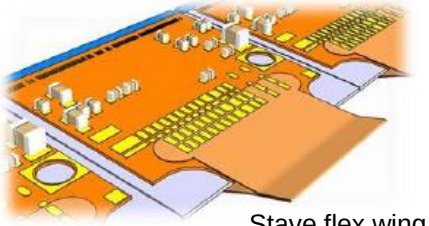
ALICE SSD HV flex



- Proposed an alternative design for the IBL detector services with this technology
  - Baseline (conservative approach): multilayer Cu-Al flex with wings
  - Alternative: laminated stack of single sided Al flex with wings

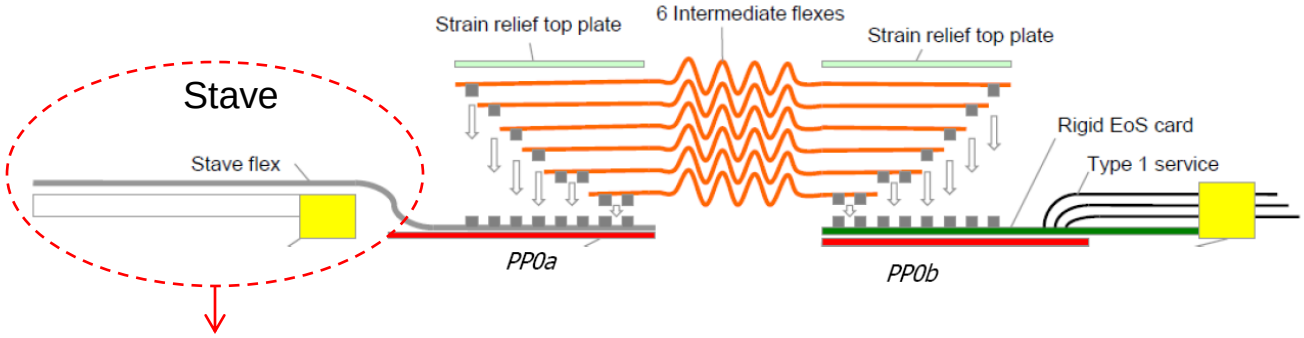
IBL services

Stave flex to module

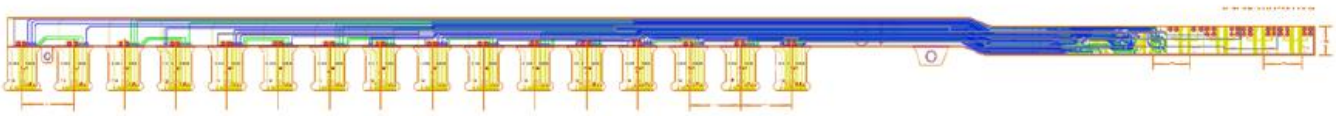


Stave flex wing

IBL services scheme

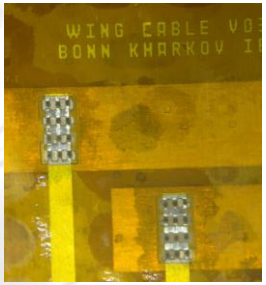


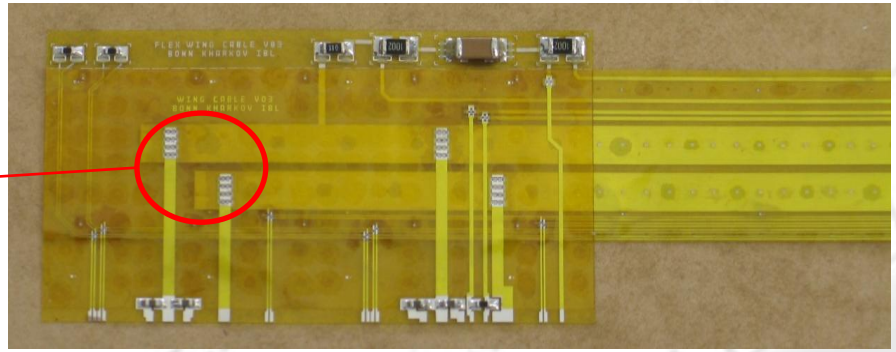
IBL services: Multilayer Cu – Al with vias→ **0.188% X_0**



Bonn proposal: Single sided Al flex with TAB bonds→ **0.098% X_0**

TAB bonds





Conclusion

- UBonn is actively investigating techniques to reduce the material budget of the ATLAS pixel detector for IBL and future upgrades (Phase-I and HL-LHC)
- The effort concentrates on reducing material from the modules and the services

	LHC				Upgrades
• Modules	1.0% X_0	→	Large thin FE, TSVs	→	<0.5 % X_0
• Cables in active area	0.5 % X_0	→	Al flex	→	0.1 % X_0
– LV cable	0.114 % X_0 (P_{eff} = ~70%)	→	SP	→	0.004-0.008 % X_0 (P_{eff} = 80-90%)

An ATLAS pixel detector featuring large thin FE, TSV, serial powering, and Al flex services would have ~1% X_0 less than the present detector

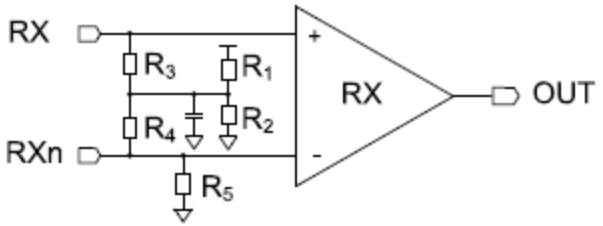
AC - coupling

- AC-coupled data transmission is needed for serially powered detector systems as every module is on a different ground potential
- An AC-coupled link requires
  - RX inputs self biased
  - DC balanced data

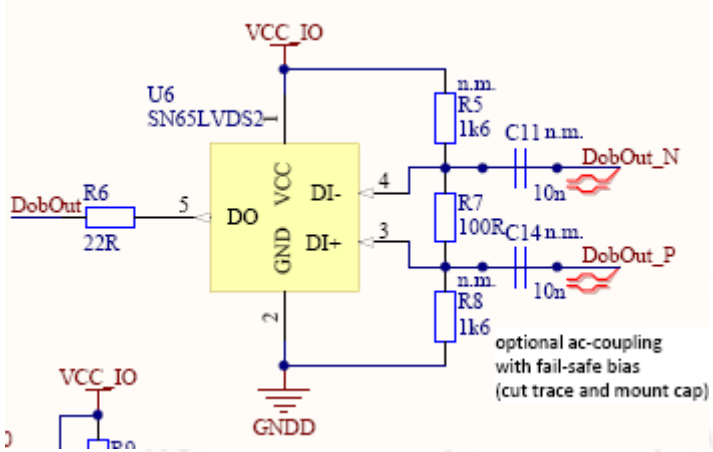
- RX
  - FEI4A: Integrated fail safe
  - USBPix adapter card: external fail safe

- Data
  - Clk is inherently DC-balanced → OK
  - DO is 8b10b encoded → OK
  - Cmd is not DC-balanced → needs manchester encoding

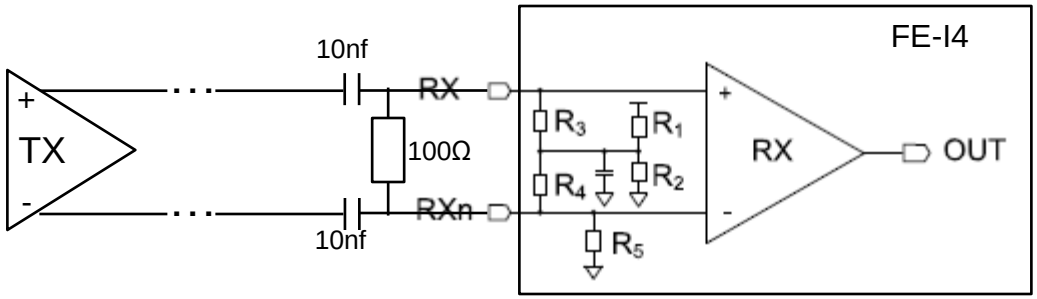
RX in FE-I4A



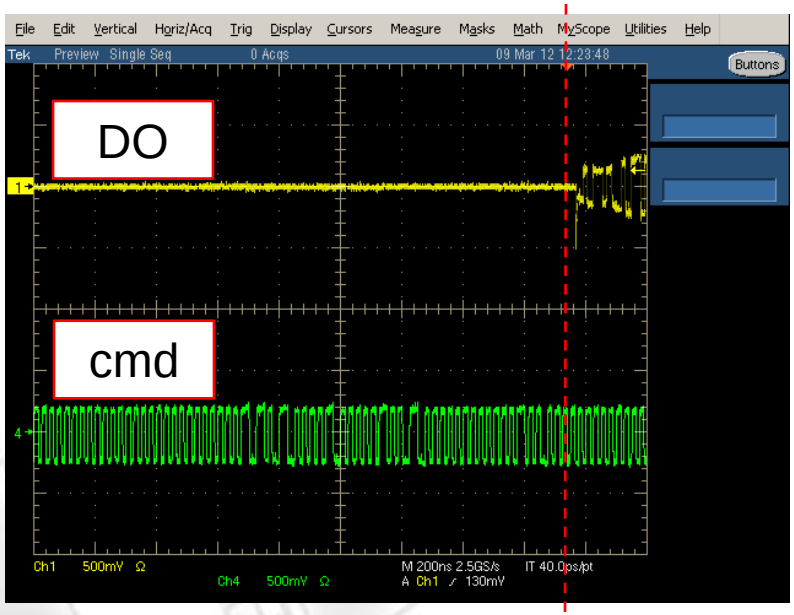
RX on adapter card



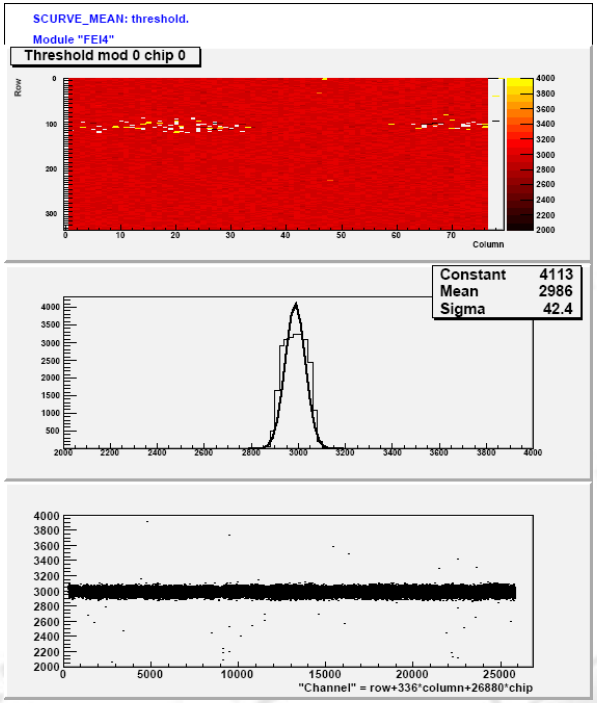
AC –coupling tests



- Cfg sent to the chip
- Configured chip sends 8b10b enc IDLE
- Chip configuration works!

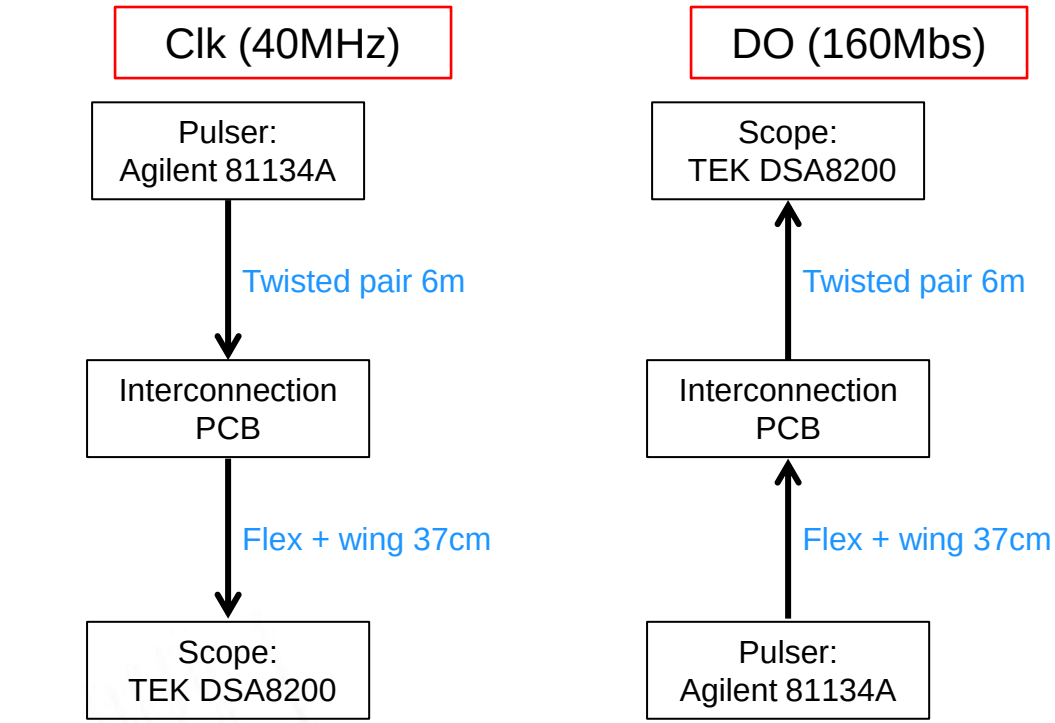


- Threshold tuning to 3000e

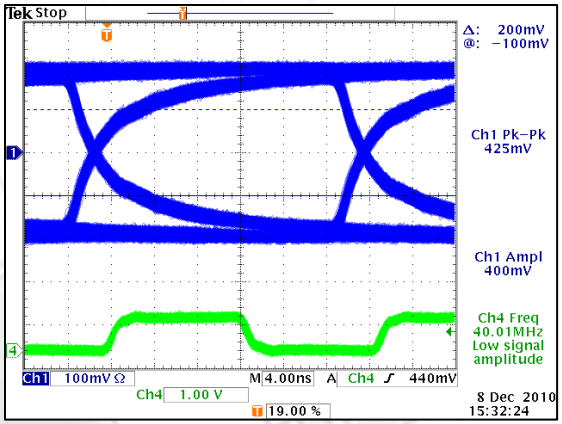


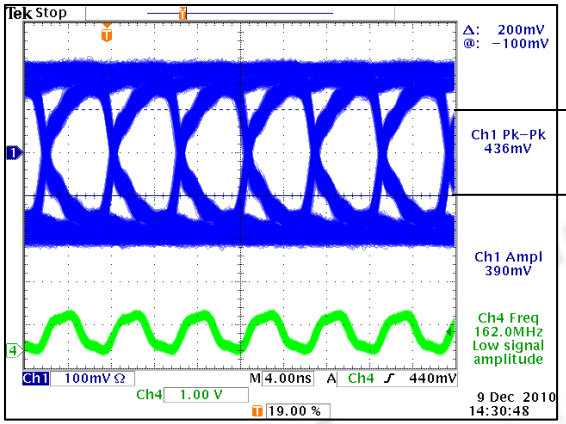
Noise:
196.2 (17.41)

Al flex technology: electrical performance



- LV lines
  - V_{drop} = 310 mV @ 1.2 A
  - Agreement with design value
- BERT
  - Runs error free for 28 hours
  - 1.6 x 10^{13} bits sent





+/- 100mV