Si-D Consortium
Bonn projects: status and plans

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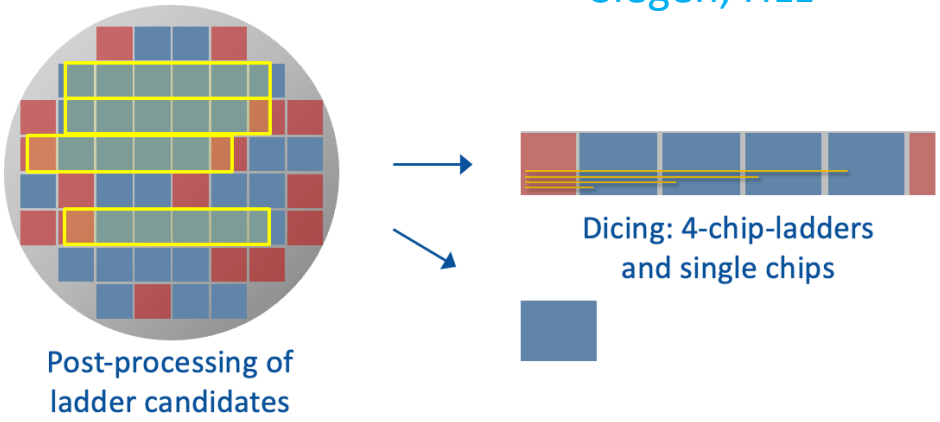
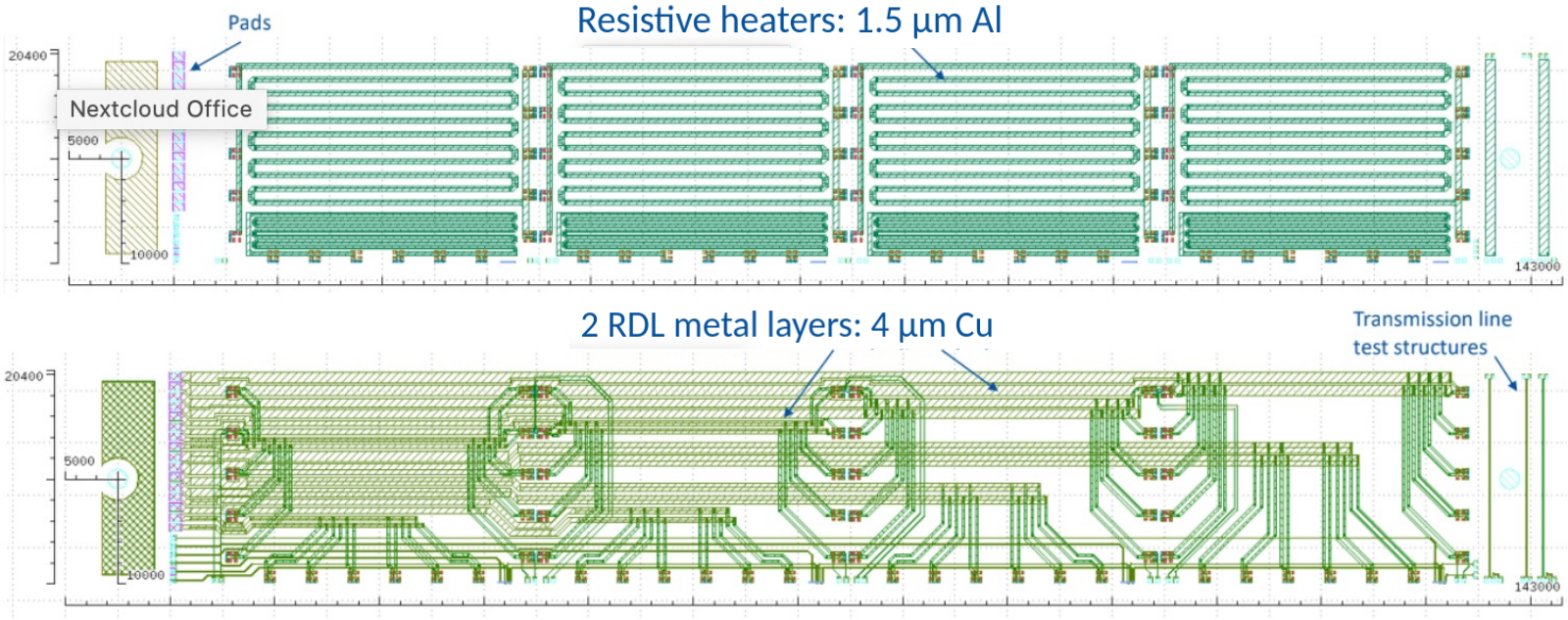
All-silicon modules

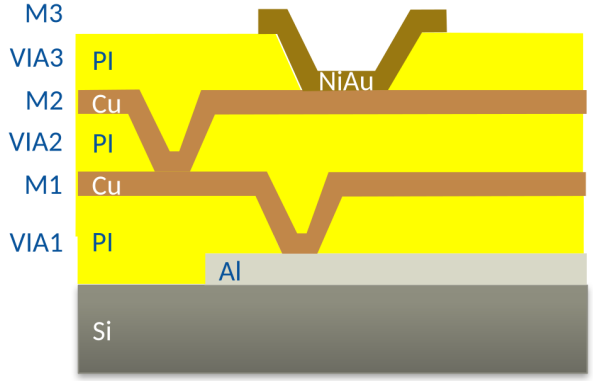
Bonn, Göttingen, Siegen, HLL

All-silicon modules with monolithic pixel chips

- Ultra-light module design
- Integration of power and readout lines directly on wafer (RDL)
  - Test measurements with RDL demonstrator modules (thermal and electrical measurements with TDR)
  - Processes established at FTD: Al sputtering and etching, polyimide deposition







All-silicon modules: Plans for next FP

Current timeline (2024-2027)

WP-1 All-silicon module	2024		2025				2026				2027	
Milestones	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
Design finished and fully simulated		o										
Wafer frontside processing finished				o								
Backside cavity etching finished						o						
Process qualified with dummy prototype							o					
Processing of CMOS wafer								o				
Characterization of CMOS ladder finished										o		
System integration and application testing												o

RIE at FTD, HLL?

wait for availability of OBELIX chip?

→ Next FP

Plans for 2027-2030

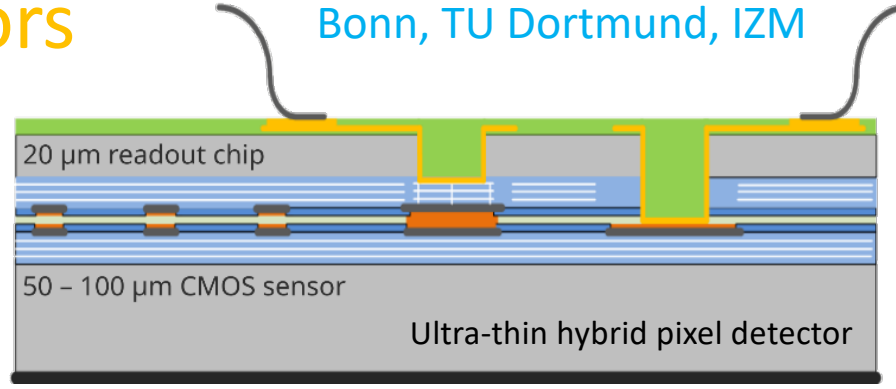
- RDL processing: further characterizations and optimizations, e.g.
  - alternative dialectric material (BCB)
  - Manufacturing techniques for best trace characteristics, vary trace width/spacing and dielectric thickness
- Produce module with CMOS sensors: OBELIX (TJ 180 nm), 65 nm TPSCo chip, …
- System integration for concrete detector design (flex, readout system, mechanical integration, cooling, …)
- Characterization (electrical, thermal, mechanical stability)

Resources (BN)

- 1 PhD (067%)
- Material costs (photoresits, metal for sputtering, …): 30 kEUR

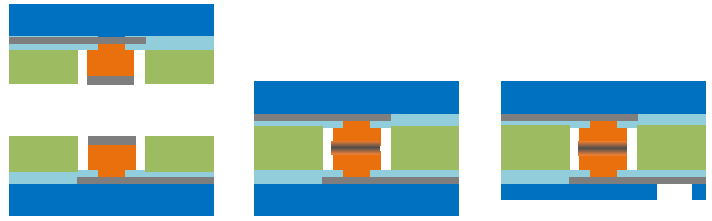
Thin hybrid pixel detectors

Bonn, TU Dortmund, IZM



Idea

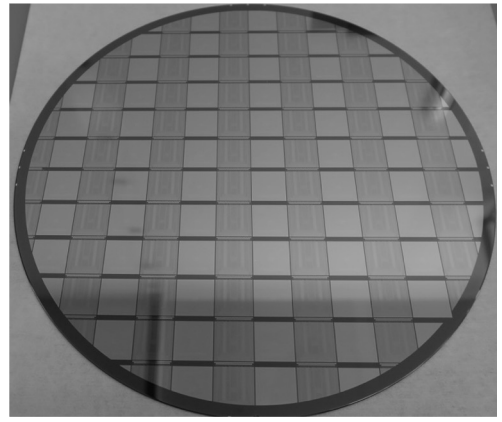
- Separate development of sensor and R/O electronics (can be separately optimized for radiation hardness)
- Wafer-to-wafer bonding for interconnection (IZM)
- Thinning of R/O chip and sensor to minimum:
  - 50 – 100 µm pixel sensor
  - 20 µm R/O chip



Wafer to wafer bonding alignment | Wafer to wafer bonding | ROC wafer thinning and TSV etching

Status

- CMOS sensor wafer layout designed and manufactured (Loundry)
- R/O chip: Timpix3 wafer (for now)
- Wafer-to-wafer bonding process established by IZM using daisy-chain wafers
- Optimized process parameters, achieved good ohmic connection across full wafer



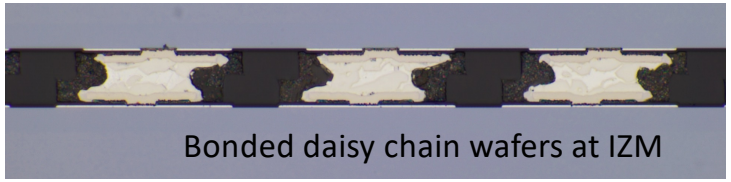
Daisy chain wafer from IZM

Next steps

- Bond sensor wafer to Timepix3 wafer
- Evaluate bonding quality and yield
- Test electrical performance at wafer level and for single- or multi-chip assemblies

Application areas

- Radiation-hard, low-material pixel detectors (e.g. for inner vertex layers)
- Large-area modules
- Detector with almost gapless coverage



Bonded daisy chain wafers at IZM

Thin hybrid pixel detectors: Next FP

Plans for 2027-2030

- Further development of wafer-to-wafer bonding, including
  - Thinning of sensor and electronics wafers
  - Dedicated wafer layouts, e.g. electronics wafer for multi-chip module (four-side buttable chips)
  - Investigating further W2W bonding technologies (e.g. metal-hybrid bonding instead of solder-polymer bonding)

Resources (BN)

- 1 PhD (067%)
- Submissions:
  - Electronics chip: 250 kEUR
  - Sensor chip: 150 kEUR

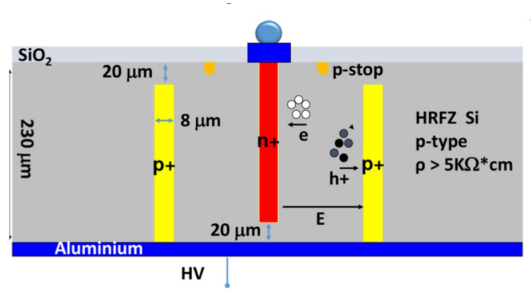
→ make it a DRD3 project (BN, Do, HLL?, international groups) to share submission costs

Design of readout chip

Bonn, Freiburg, KIT, Thessaloniki

3D Sensors for timing applications (FR, KIT, DRD3 partners)

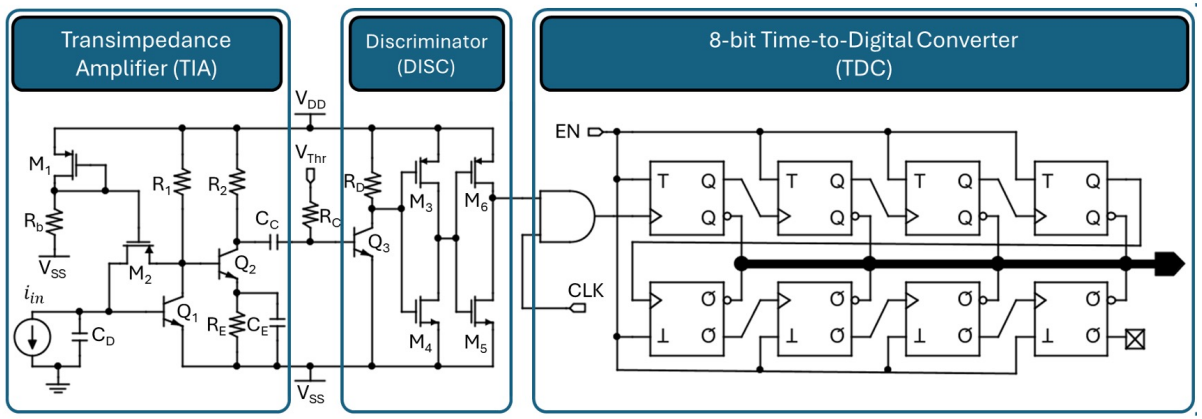
- 3D sensors produced by CNM (RD50 common project sensors + old IBL 3D sensors)

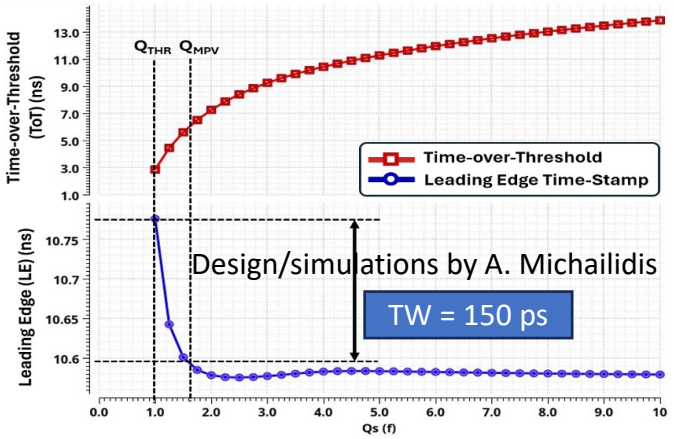


- Readout chip design (BN, Thessaloniki)

  Dedicated readout ASIC with high-bandwidth analog FE adapted to large sensor capacitance

  - 130 nm SiGe BiCMOS technology
  - Performed initial design studies in simulation
  - Tape-out of first test structures in August 2025 → ready for characterization in spring 2026





Contributions to design of R/O chip for next-generation vertex detector

- e.g. as part of OCTOPUS project (65 nm TPSCo)