Fachhochschule
Dortmund
University of Applied Sciences and Arts

Si-D Meeting

Strategy Discussion

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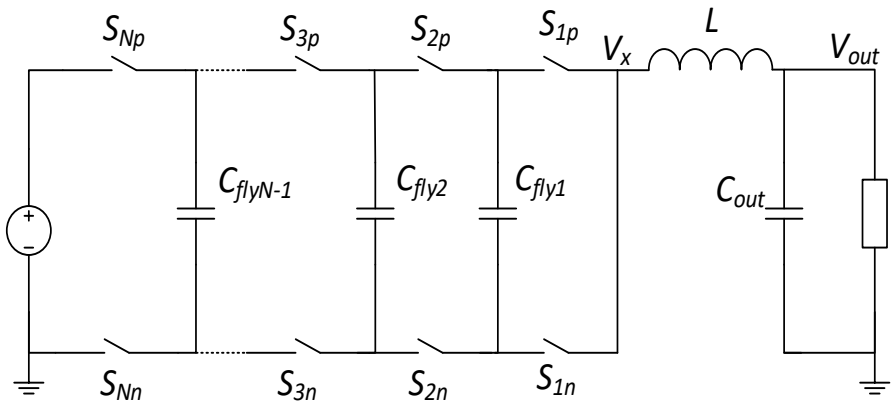
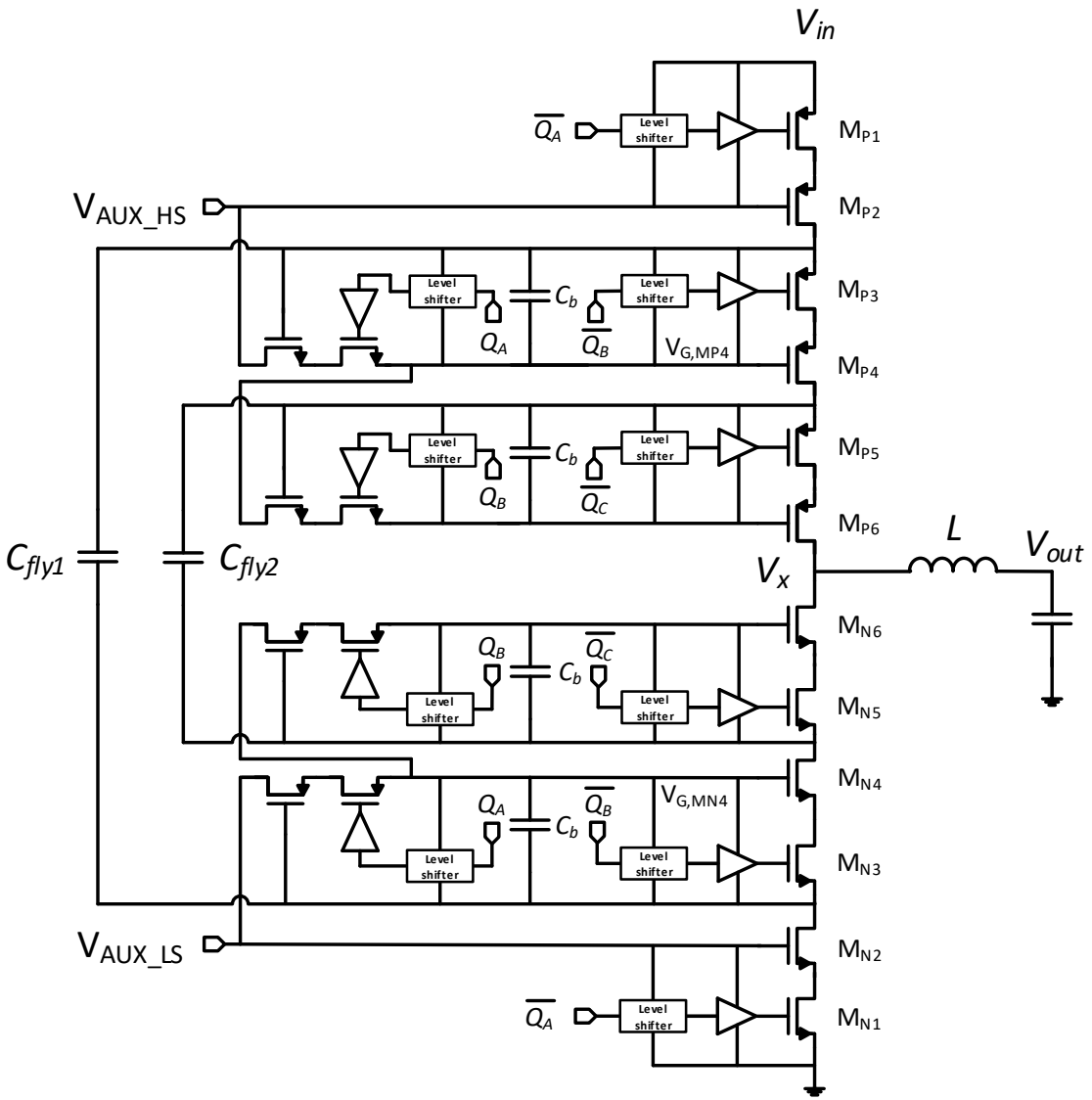
Flying Capacitor Multi Level Converter (FCML)

- Better utilization of passive components compared to conventional buck topology
- **5 – 10 MHz** switching frequency allows use of **external small volume air core inductor**s
- Cascoding & flying capacitors allows higher V_{in}
  - using thin gate oxide transistors only (**no HV-devices necessary**)
- **Main challenges:**
  - Reliable control of power switches when $V_{in} > V_{device,nom}$
  - Startup required to pre-charge the flying capacitors
  - Balanced flying capacitor voltage in steady state

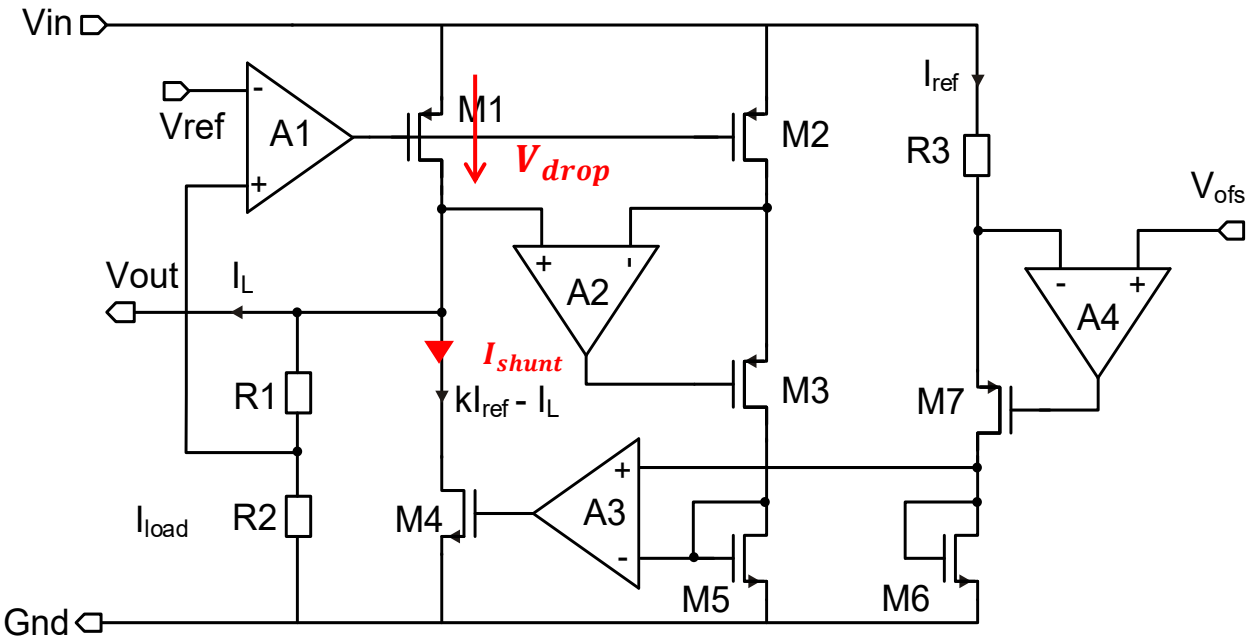


4L-buck with additional cascode transistors

- Max. input voltage up to 6 x V_{DD}
- Control system provides signals $\overline{Q_A}$, $\overline{Q_B}$ and $\overline{Q_C}$ for:
  - M_{n1}, M_{n3} and M_{n5}
  - M_{p1}, M_{p3} and M_{p5}
- Gate voltage of M_{n2} and M_{p2} are fixed to V_{AUX_LS} and V_{AUX_HS}
- Driver circuit with bootstrap capacitor C_b necessary to control gate voltages of
  - M_{n4} and M_{n6}
  - M_{p4} and M_{p6}



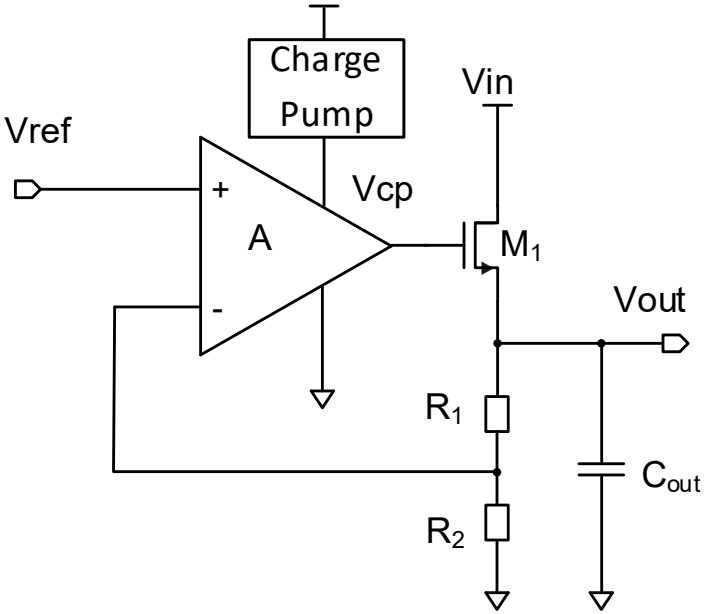
Efficiency Improvement



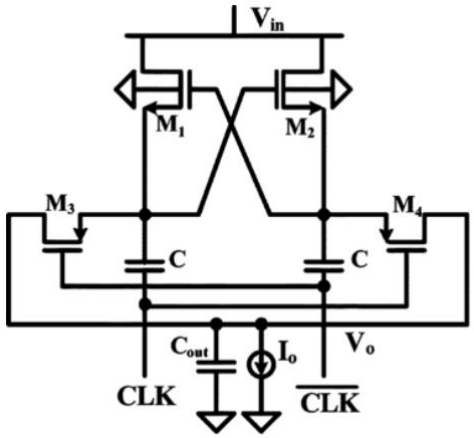
$$\eta = \frac{V_{out} I_{load}}{(V_{out} + V_{drop})(I_{load} + I_{Shunt})} = \frac{1}{\left(1 + \frac{V_{drop}}{V_{out}}\right)\left(1 + \frac{I_{Shunt}}{I_{load}}\right)}$$

Drop out voltage and shunt current main sources of inefficiency

Ultra-Low Drop Out Regulator with NMOS Pass-Device and Charge Pump

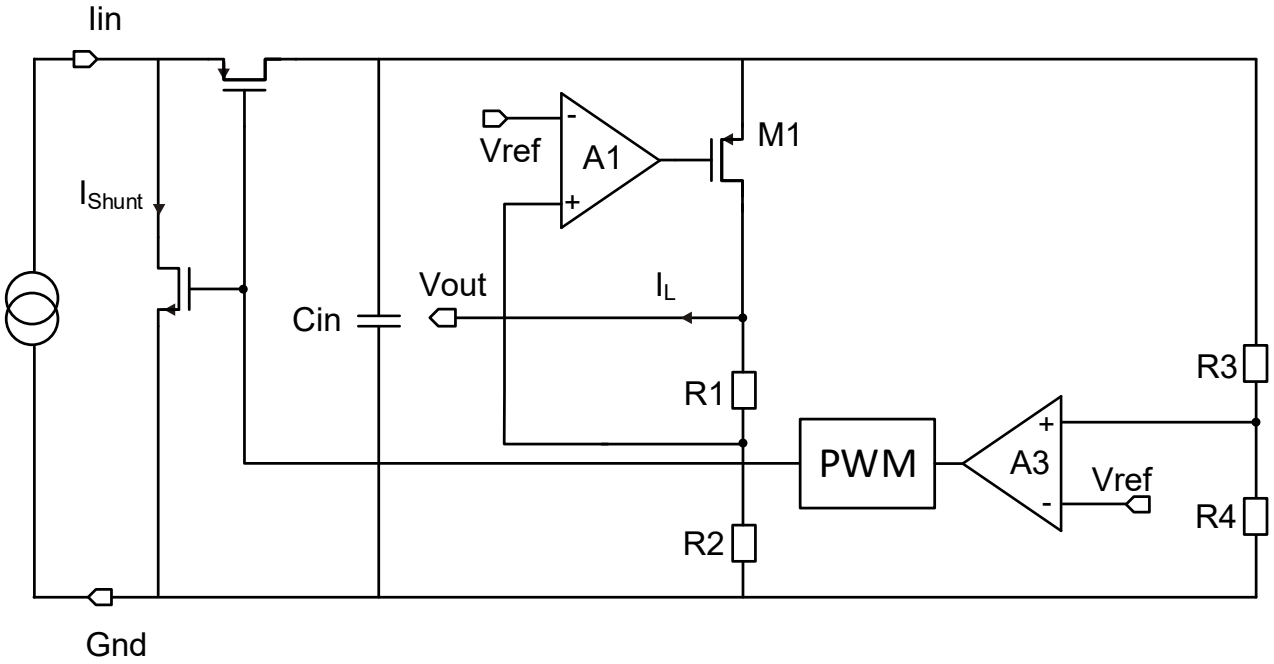


CMOS Voltage Doubler



- At ultra low drop-out the pass-device is in linear region
- More gate-source voltage overdrive or wider transistors required
- NMOS has higher transconductance
- NMOS is more radiation tolerant
- Requires charge pump for error amplifier supply voltage

Switch-Mode Shunt Regulator



Shunt Losses: $P_{Shunt} = U_{Shunt} \times I_{shunt}$

→ To shunt high current efficiently low voltage required

→ switched-mode regulation required

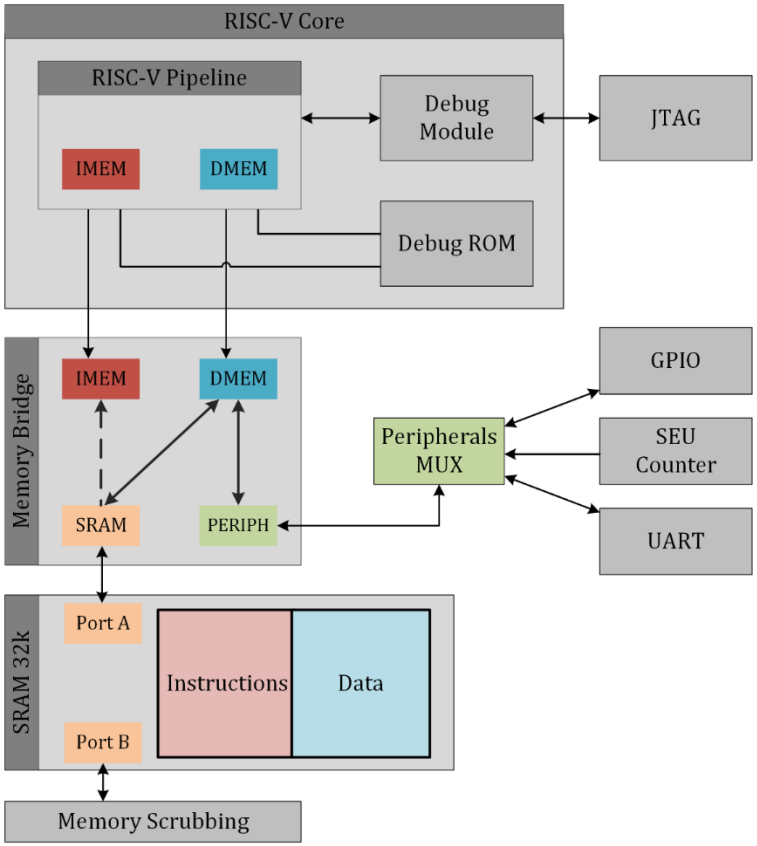
→ Shunt element has to move from output back to input

→ Shunt current balancing has to be studied

→ Pulsing module voltage may cause system problems

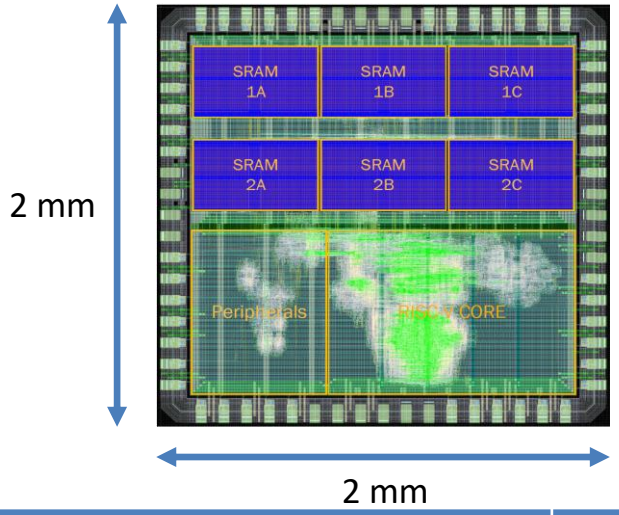
Radhard RISC-V Microcontroller

- AIRES RISC-V core from Fraunhofer IMS
  - RV32-IMC Core
  - 3 stage pipeline
- JTAG Interface
  - JTAG TAP & debug module
  - Non-volatile debug ROM with debug ISR
- Peripherals
  - Memory mapped registers
  - UART
  - GPIOs
  - SEU Counter
- full TMR applied to core and periphery
- triplicated dual port SRAM 3 x 32KByte
- Scrubbing controller connected to second port

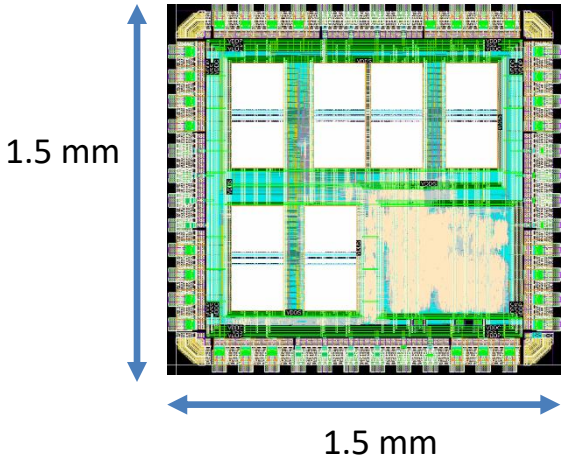


STRV-1/2 Microcontroller Features

STRV-1 (65nm)



STRV-2 (28nm)

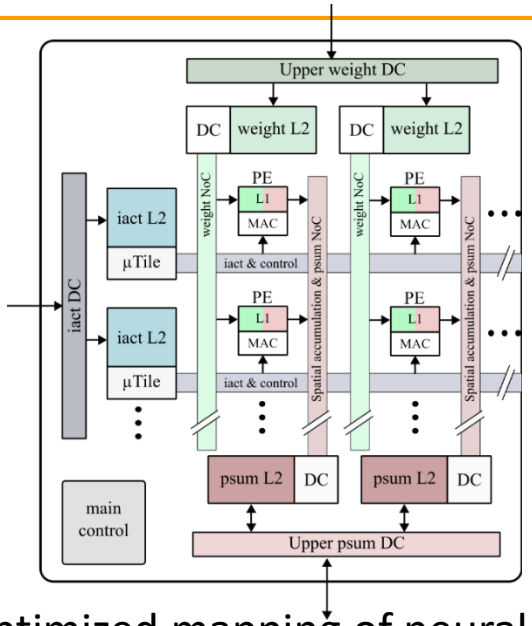


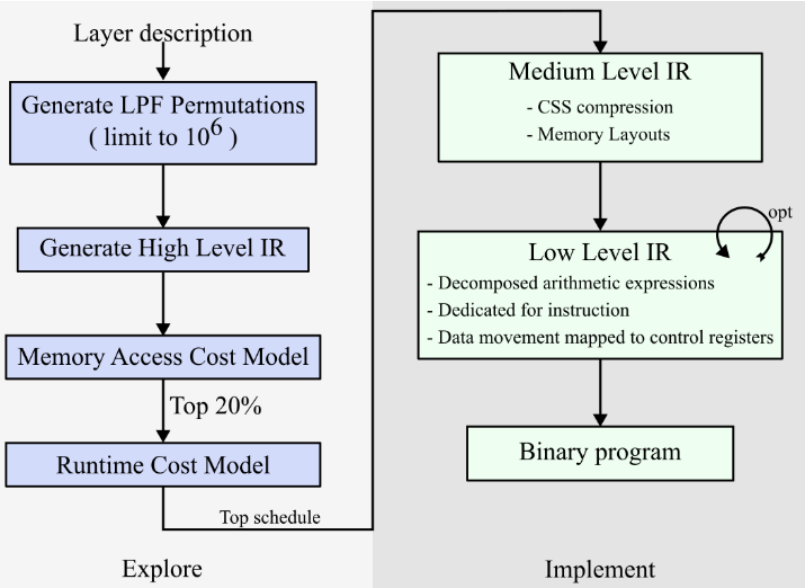
- functional under lab conditions
- detailed characterization ongoing

	STRV-1	STRV-2
Frequency	50 MHz	100 MHz
Supply Voltage	1.2V	0.9V
Power with Scrubbing	20 mW	-
Power without Scrubbing	15 mW	-
TID hardness	1 Gigarad	-
SEE hardness	2.2 SEFI/h @ 10^9 p/cm²/s	-

Dataflow Optimized Flexible AI/ML Accelerator

- Process element matrix scalable in X and Y direction to define parallelism
- Scalable L1 /L2 memories sizes to influence locality of data processing and meet bandwidth requirements
- Programmability of the processing sequence during runtime e.g. spatial/temporal distribution
- Data coding that restricts flexibility is avoided e.g. bitmaps instead of RLC, CSS in the feature maps





- automatic optimized mapping of neural networks to custom hardware
- compiler translates configurations into intermediate representations
  - MLIR Framework (Multilevel Intermediate Representation)
- Evaluation using cascaded cost models e.g. for memory accesses, peak bandwidth, runtime, pre- / post-processing,

AI/ML accelerator performance metrics

- inference accuracy for ImageNet (classification 1000 classes)
  - AlexNet: top 5 accuracy, 80.1% (float32: 79.5%)
  - MobileNetV2: top 5 accuracy, 89.4% (float32: 92.7%)
  - post training 8 bit quantization
- hardware performance in 28 nm TSMC:
  - area requirement IP core: < 0.5 mm²
  - power consumption: ~ 10 mW / 4.4 TOPS/W
- Throughput:
  - AlexNet: ~ 10 FPS, MobileNet ~ 30 FPS
- Dataset: ImageNet / ILSVRC2012 :
  - 1000 classes, 250x250 px
  - No. of images: 1.3 million
- Model: MobileNet v2
  - 50 layers
  - weights and feature maps 1 kB - 1 MB per layer with 8-bit quantization