More ROC Tests

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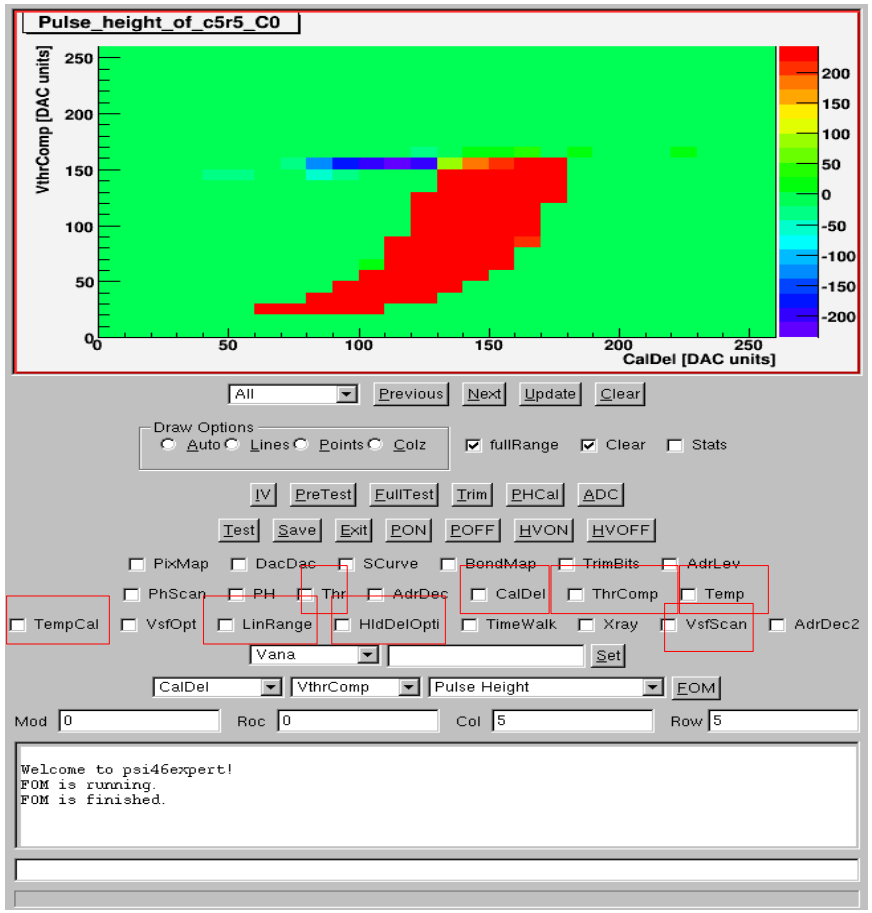
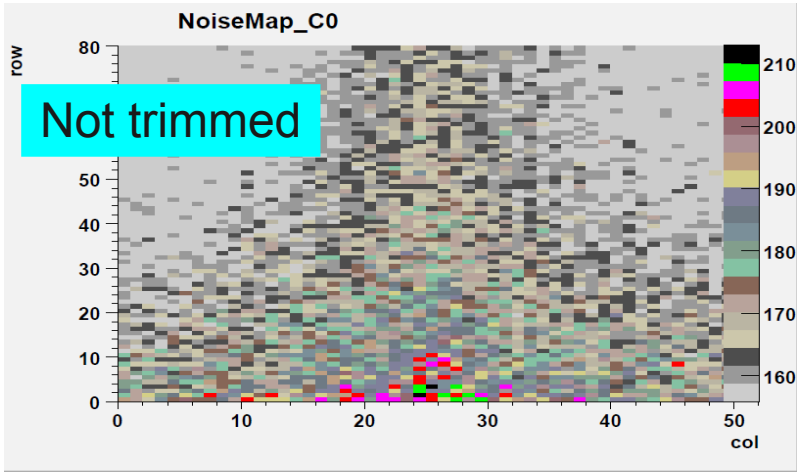
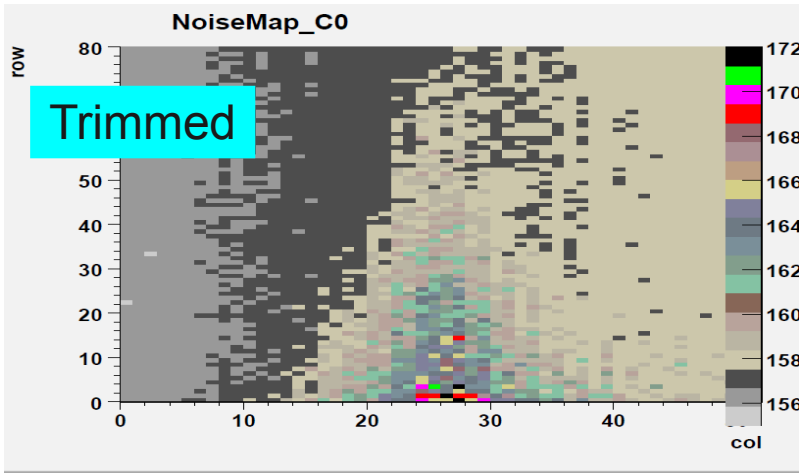


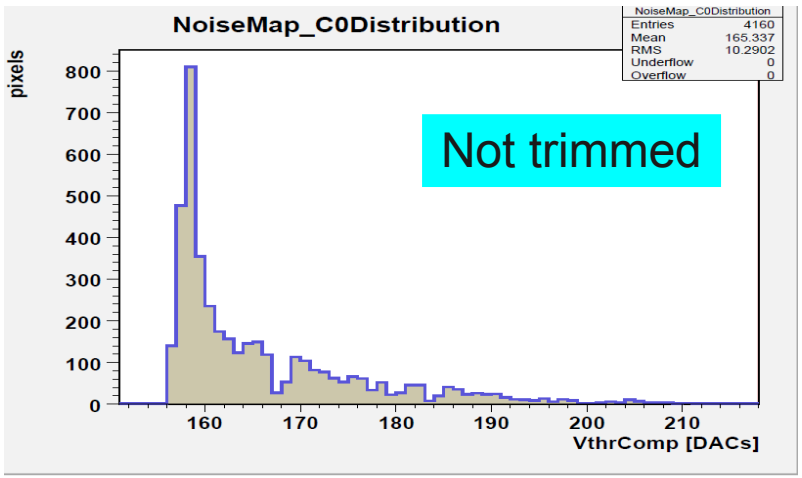
- Noise test
- CalDel efficiency
- VthrComp efficiency
- Temperature tests
- VhldDel optimization
- Vcal linear range
- Vsf scan

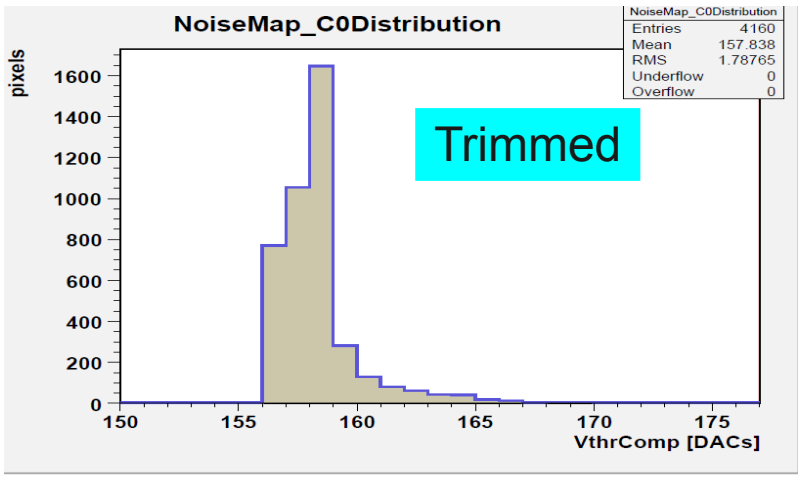
Noise map (Thr)

- Set Vcal = 200. Read Trim parameters (optional)
- Pulse pixels and scan VthrComp DAC close to noise (High VthrComp = low threshold ⇒ noise area)
- Plot thresholds. ~1 min test.









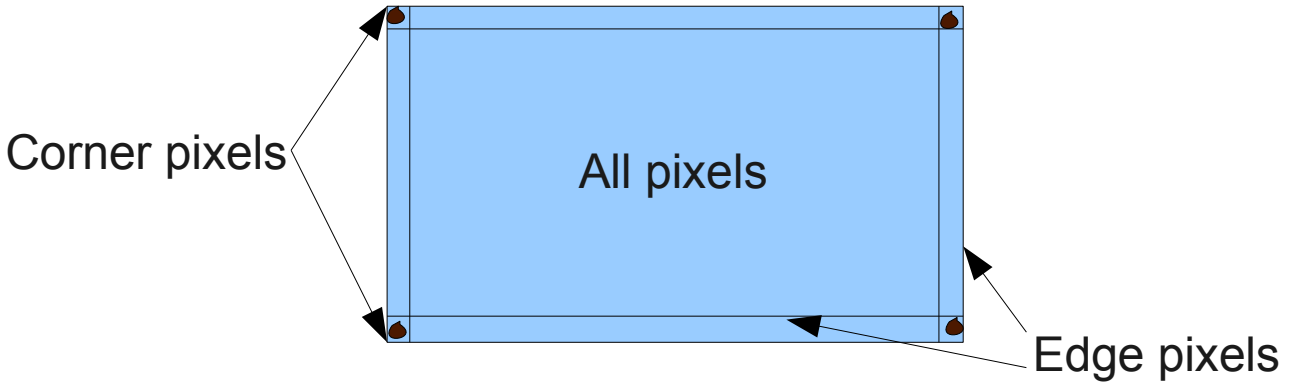
Noise Mean stays but RMS reduced by factor of 5 after the Trimming

Efficiency test 1 [CalDel]

- For Vcal from 60 to 250 (CtrlReg=0) and Vcal from 50 to 200 (CtrlReg=4, amplitude of injected signal is 7 times higher) scan CalDel from 0 to 255, rough step=10
- Use ChipEfficiency: read scurve dataBuffer=sdata[pixels]/nTriggers, nTriggers=10. sdata[pixels] : measure PH for each pixel (fast reading of FPGA data)
- Calculate efficiency for each bin in Vcal and CalDel space:

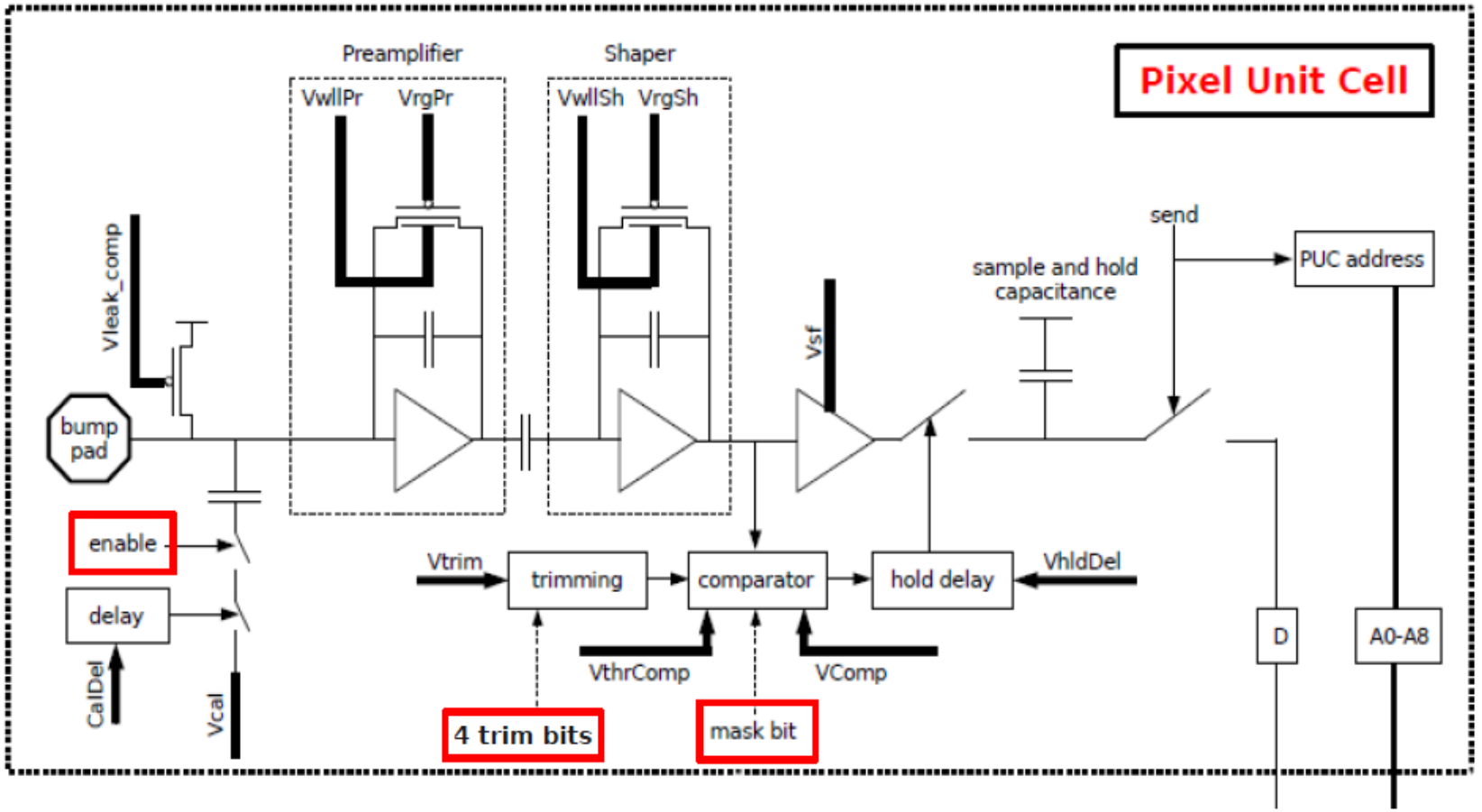
$$eff\left(Vcal, CalDel\right) = \frac{\sum sdata\left(pixels\right)/10}{4160}$$

- If efficiencies of 2 neighboring bins in CalDel are differ by >5% → start with fine steps=1 and calculate efficiencies for them
- Plot efficiencies for 3 different cases: all pixels, edge pixel, corner pixels:



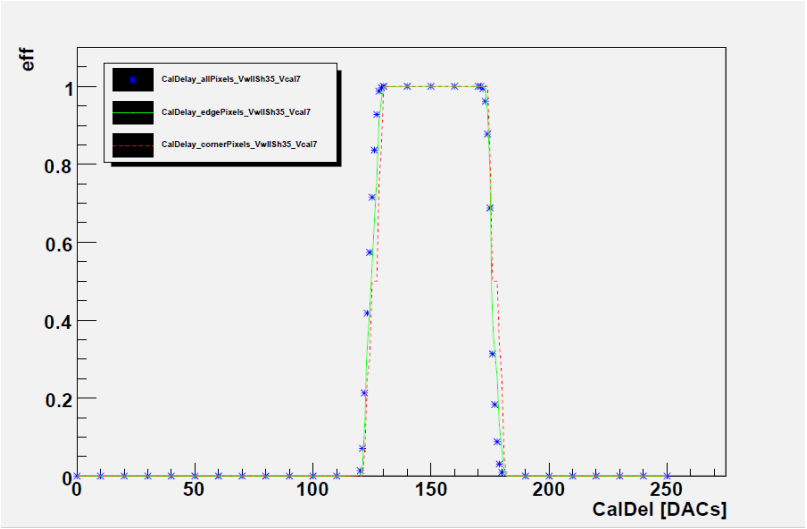
~2 hours test

Psi46 Pixel Readout Chip

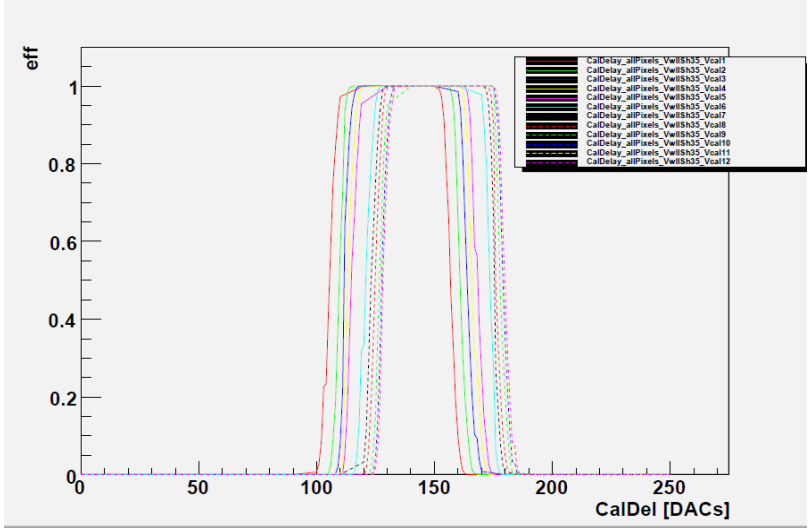


Efficiency test 1 results

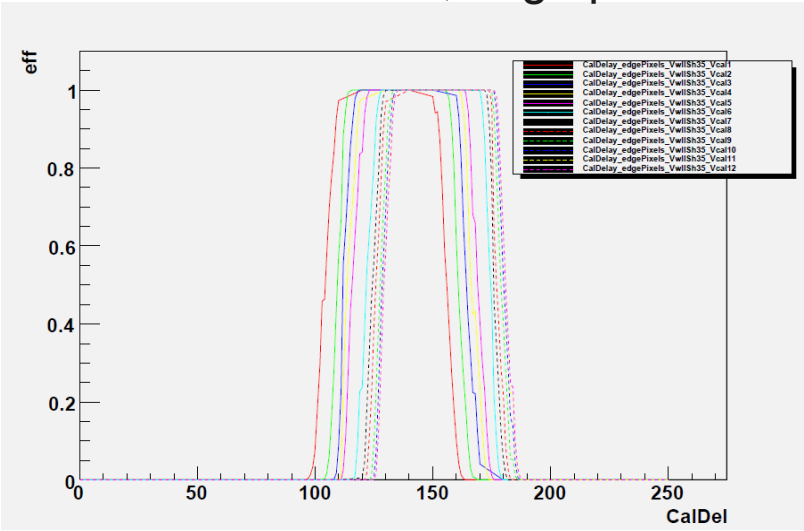
Vcal = 200



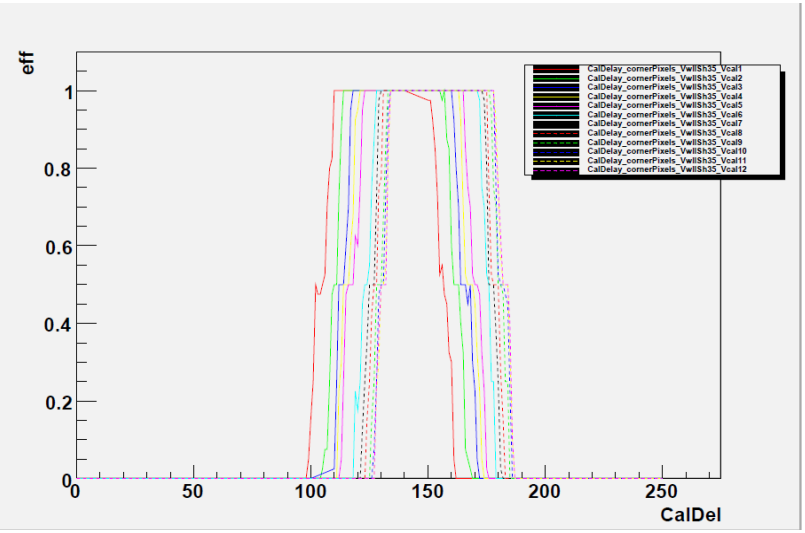
Vcal = 60 – 250, all pixels



Vcal = 60 – 250, edge pixels



Vcal = 60 – 250, corner pixels



Plateau of efficiency shifts to larger CalDel values if Vcal increases (time walk). Similar behavior for all pixel types.

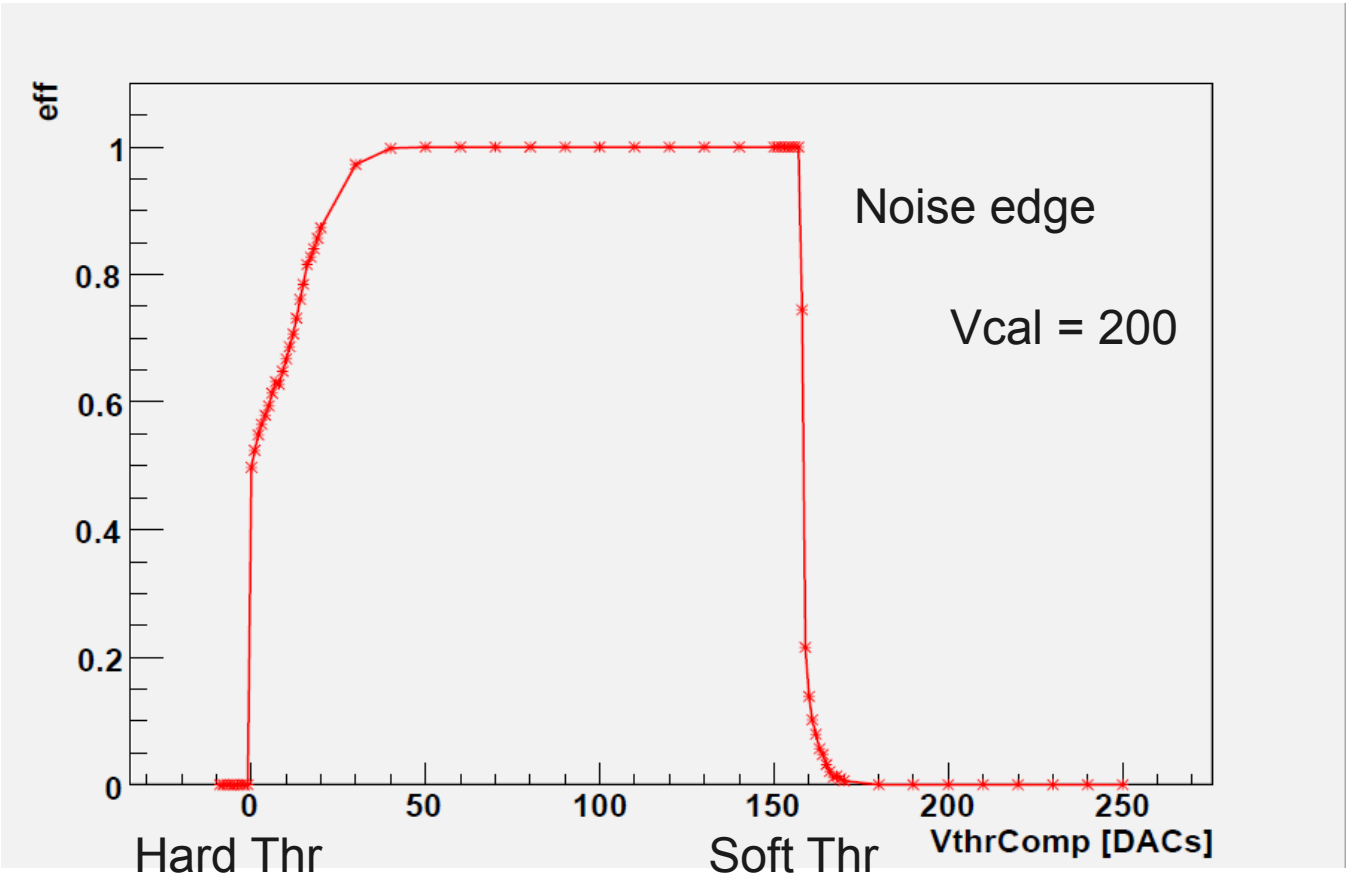
Efficiency test 2 [ThrComp]

- For Vcal = 200 and CtrlReg = 0 scan VthrComp from 0 to 255, rough step=10
- For each VthrComp scan CalDel from 0 to 255 with a step=25. Use ChipEfficiency: read scurve dataBuffer=sdata[pixels]/nTriggers, nTriggers=10.
  Choose for each pixel the highest dataBuffer value from these 11 steps in CalDel
- Calculate efficiency for each VthrComp:

$$eff\left(VthrComp\right)=\frac{\sum sdata\left(pixels\right)/10}{4160}$$

- If efficiencies of 2 neighboring bins in VthrComp are differ by >10% → start with fine steps=1 and calculate efficiencies for them
- Plot efficiency vs VthrComp DAC

Efficiency test 2 result



Time consuming test: ~40 min. per ROC

Temperature test [Temp]

- The CMS pixel readout chip has a built in temperature sensor designed to measure temperatures in the range [-30°C, +70°C]

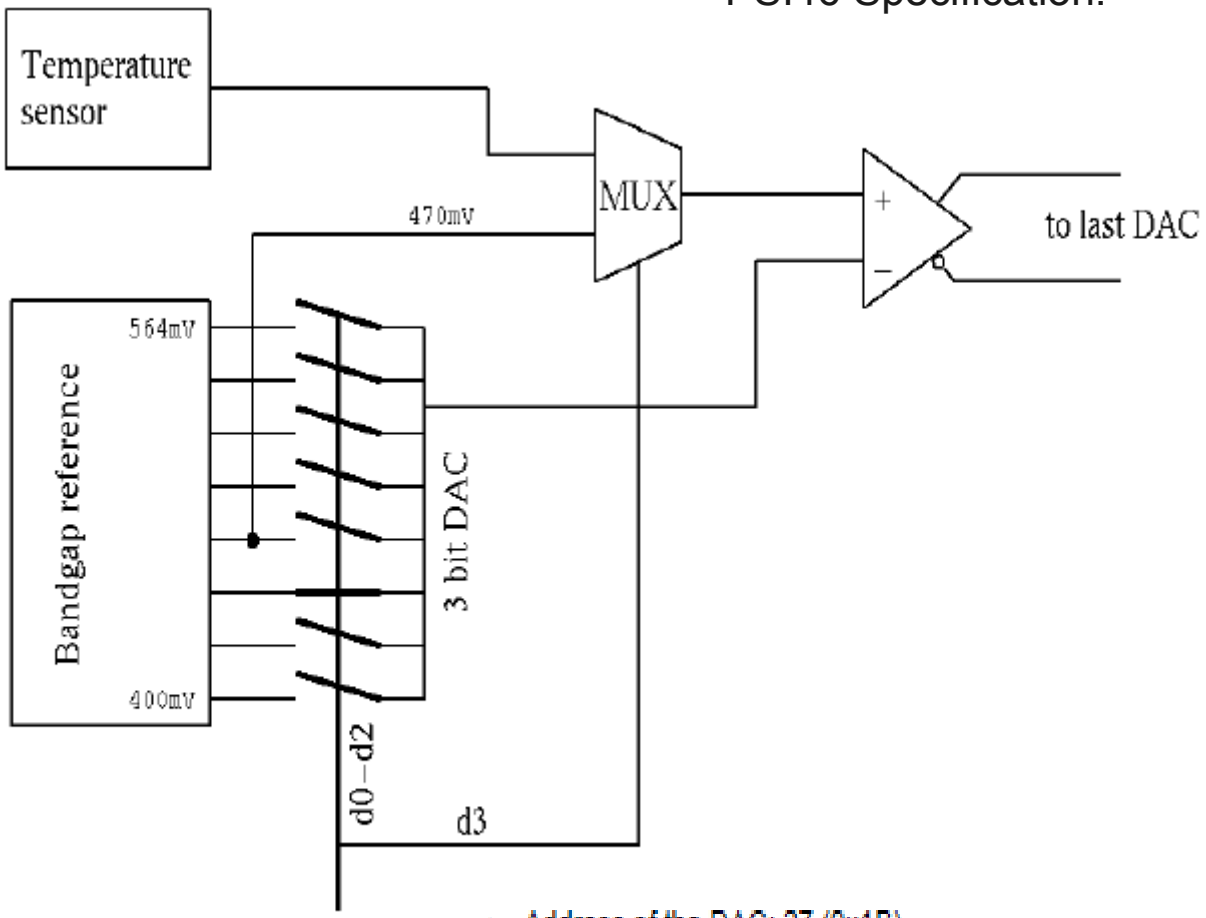
- Test signal is a LastDac ADC signal (LD) ~ to voltage difference between T sensor (temperature dependent) and reference (temperature independent)

- For better accuracy 8 different windows (reference voltages 400 – 564 mV) of measurement are defined: one part of T° measurements compared to one V window, another part to another V window etc. Windows are programmed by register 27 'RangeTemp'

- Calibrate output signal to extract the voltage difference from the measured LD ADC value. The sensor output signal is replaced by 470 mV for calibration. Make a linear fit to the calibration points differ from the ROC Black level. This fit is used to determine the measured voltage difference, which is finally added to the known reference V to get a sensor voltage

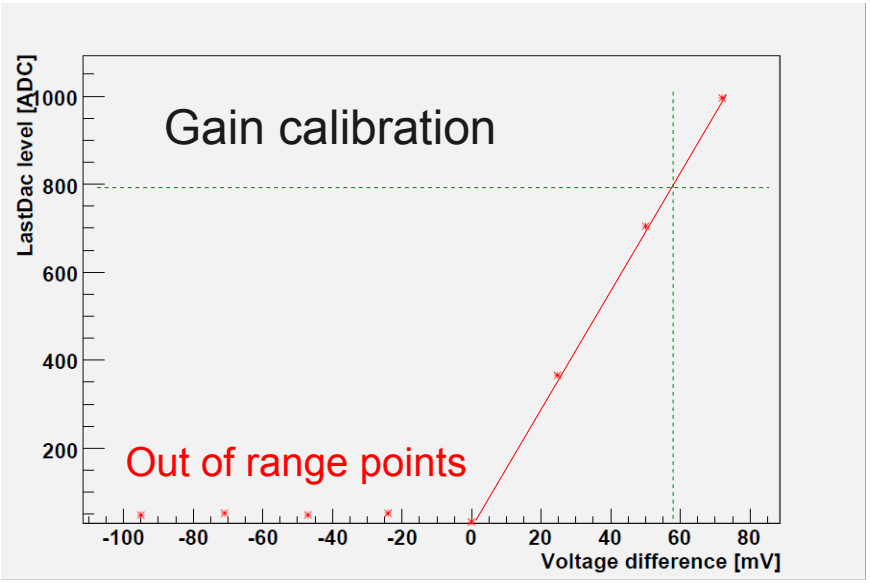
T measurements

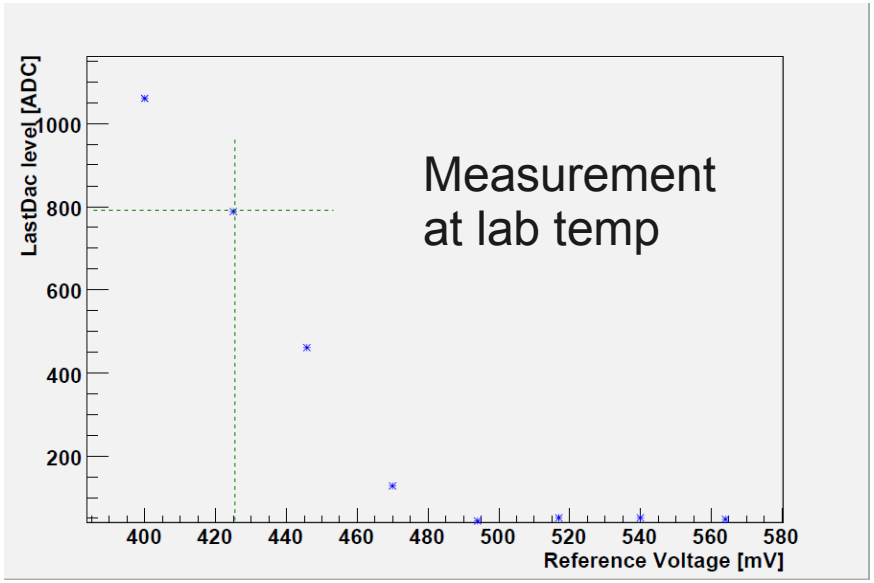
PSI46 Specification:



- Address of the DAC: 27 (0x1B)
- The first 3 data bits set the reference voltage in the range [399.5mV, 564mV] in steps of 23.5mV (unirradiated).
- Bit 4 switches between the temperature sensor output voltage (bit cleared) and a fixed voltage of 470mV (bit set).

Temperature test results





Voltage difference = Vref – 470 mV

- Example chip 2:
  - Look at ref. Voltage = 425 mV
  - measure LD = 800 ADC,
  - => V difference = 58 mV
  - Sensor Vtemp = 425 + 58 = 483 mV
  - T = 0.625 (Vtemp – Vmid)

Average temperature (°C) measured by different ROCs

Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8
17	16	21	19	17	21	20	17	16

Temperature may increase by 3°C during test

Temperature calibration test [TempCal]

- PSI code uses an interface to JUMO software. It produces T sensor and calibration table for known temperature values from JUMO
- JUMO is one of the leading manufactures in the field of industrial sensor and automation technology including the entire measuring chain from sensors to automation solutions for temperature, pressure, humidity etc.
- The company provides hardware and software solutions for temperature control, regulation, monitoring and visualization.

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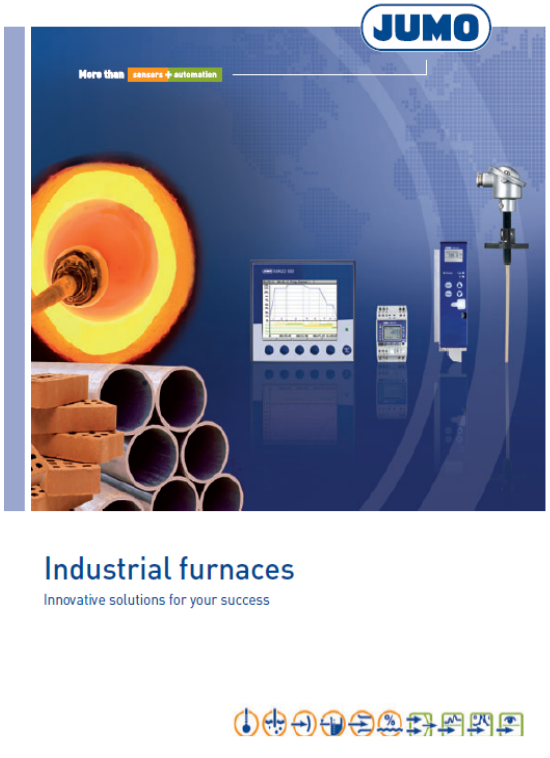
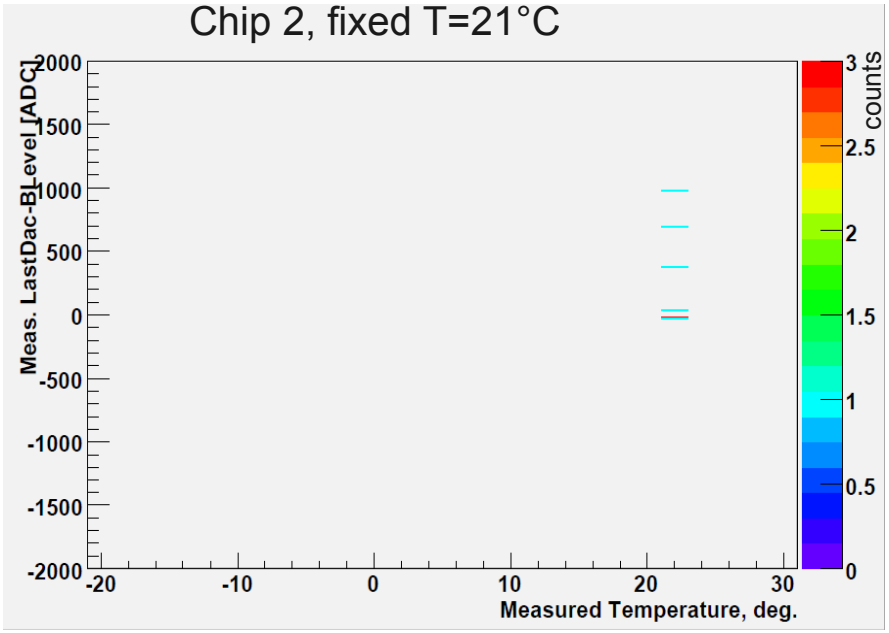
  E-mail: mail@jumo.net

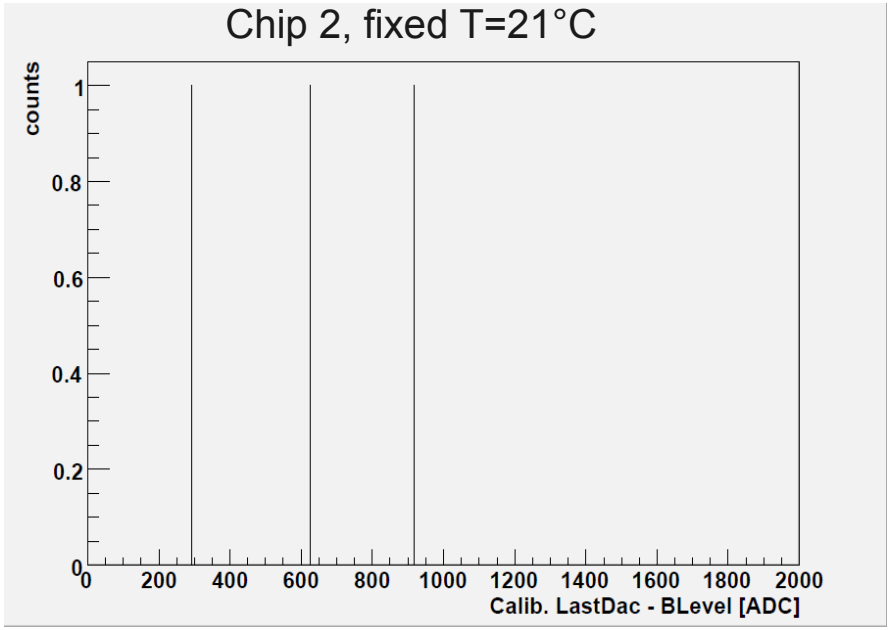


Temperature calibration test [TempCal]

- Program can send commands to JUMO to cool-down or heat-up to the known T with a known step and time delay
- Initialize JUMO controller of cooling box, flush N_2, wait until actual T = target T
- Check temperature every 10 sec. When the target T is reached → measure T sensor and calibration ADC values. Make a table for known temperature values from JUMO:

T = +21 : blackLevel = 72, Vcalibration = { 916 624 292 -40 -20 -20 -20 -16 }, Vtemperature = { 972 692 376 36 -20 -28 -20 -20 }





VhldDel optimization [HldDelOpti]

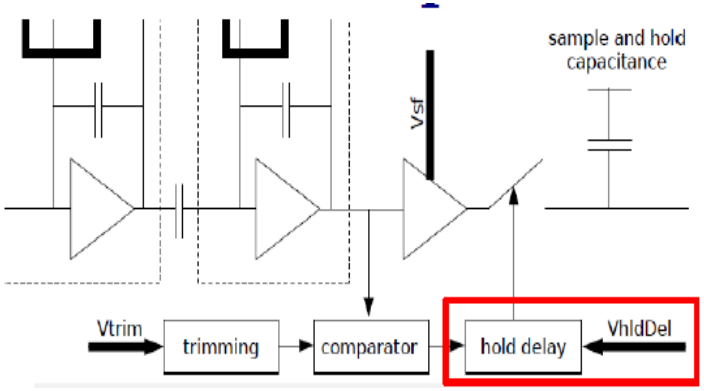
- If signal exceeds the reference voltage in the comparator, it is passed on to the sample and hold capacitor with an adjustable delay (VhldDel). Signal is stored in the capacitor until the double-column periphery starts the readout and writes the address, PH and BC into the data buffer
- VhldDel should be set in such a way that for different Vcal the signal is sampled with a maximum PH

- Fix optimal Vsf (DAC responsible for PH linearity) and scan VhldDel (0–200) with step=10

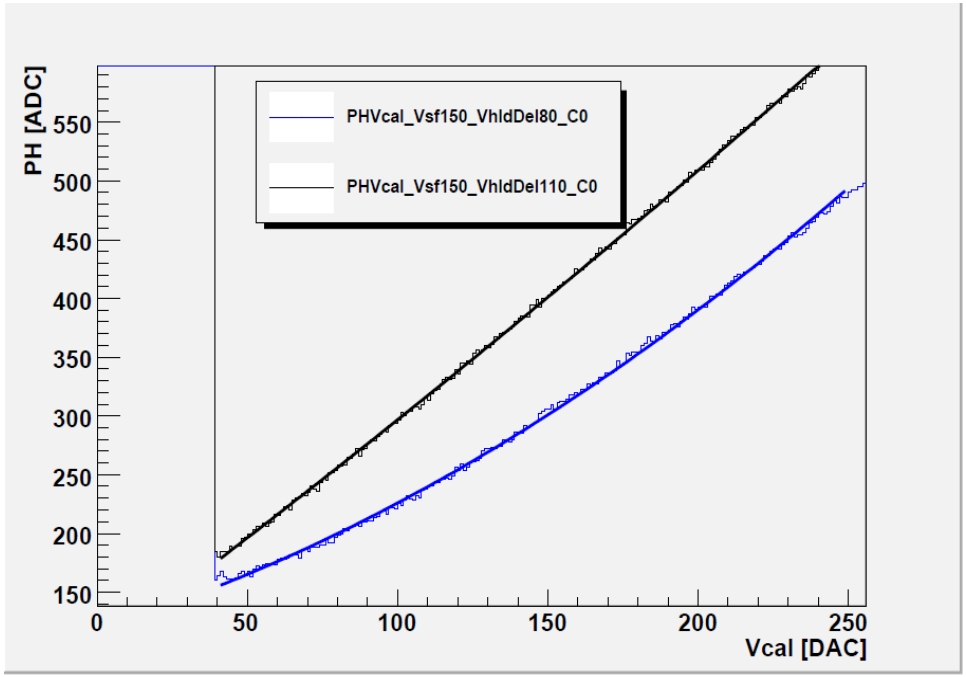
- For each VhldDel step find PH linearity quality:
  - Fit PH Vcal curve from 0 to 255 by quadratic polynomial
  - Linearity quality LQ= –par(2) / par(1)
  - Best linearity = min(abs(LQ))

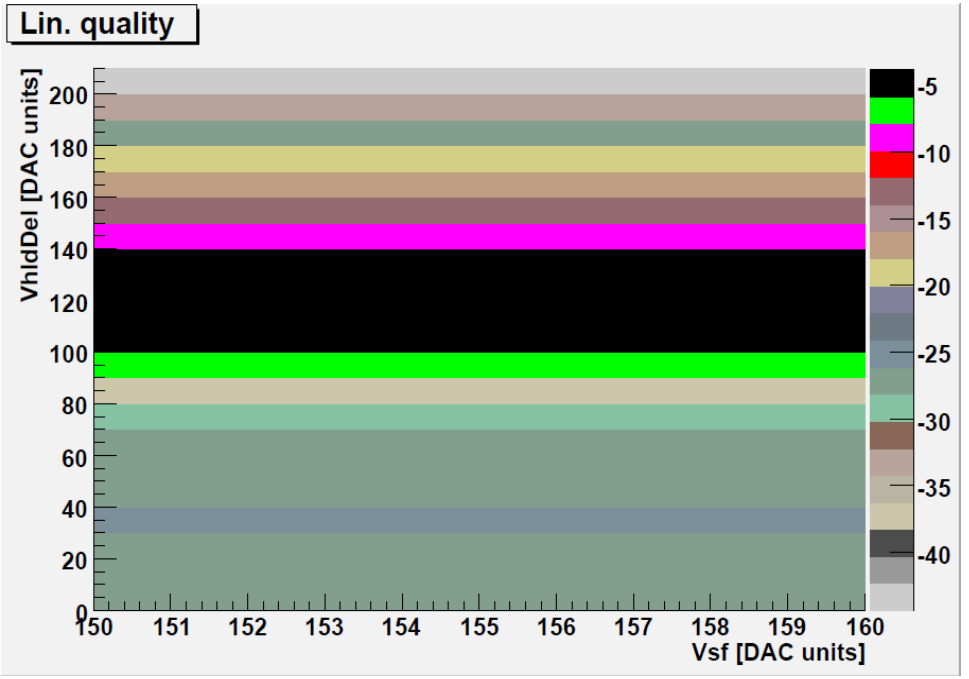
- Save VhldDel with the Best linearity – this is an optimal DAC value

- Check of one row and column: ~20 sec.



VhldDel optimization results



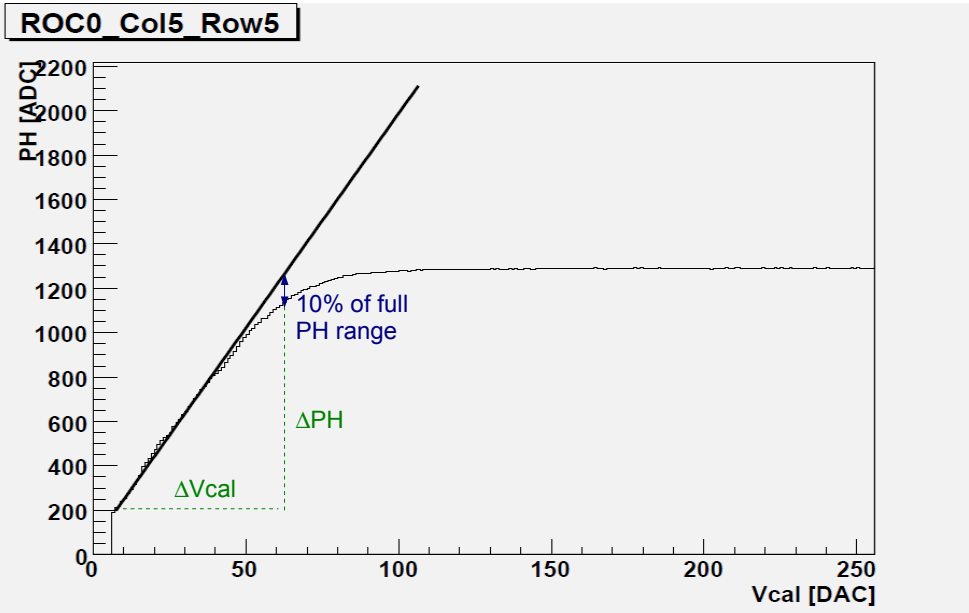


- PH linearity depends on VhldDel value
- Better linearity for VhldDel=110 (example)

- Choose Vsf=150, VhdDel=130

Vcal linear range [LinRange]

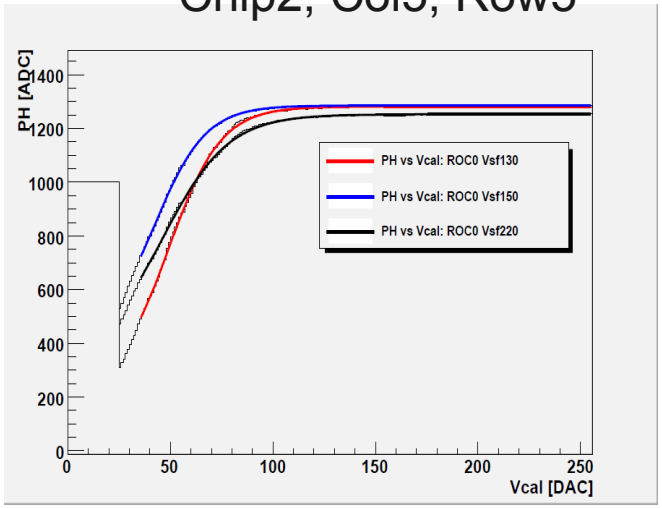
- Linear dependency of the Pulse Height and the injected charge on a pixel is
- important for spatial resolution
- Check a linear range for each ROC separately:
  - Use high Vcal (450 e/DAC)
  - Pulse one pixel and plot PH
  - Make a linearity check:
    - Define start, stop points and inflection point by analyzing of polynomial of deg. 4 fit (use derivatives)
    - Beginning from the inflection point in both directions, the PH-difference between the tangent (from start to stop) and the polinom. fit is calculated
    - The curve is not linear if PH-difference > 10% of total PH range
    - Linear range is a combination of linear parts in Vcal and in PH directions: $LR = \sqrt{(\Delta Vcal)^2 + (\Delta PH)^2}$
    - Example: LR=960
    - May vary from pixel to pixel by 8% in one ROC

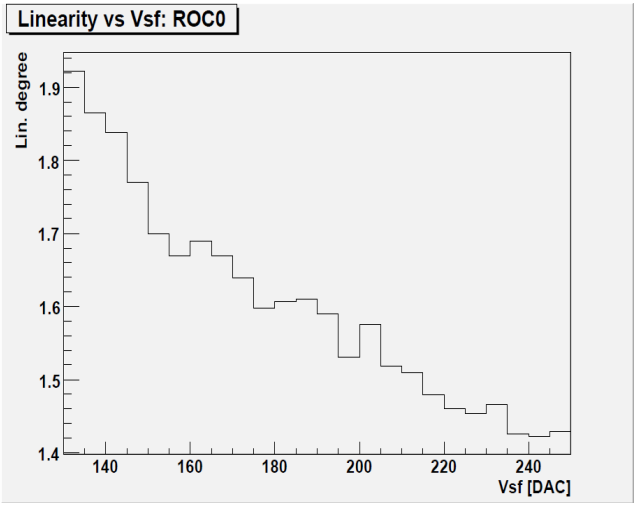


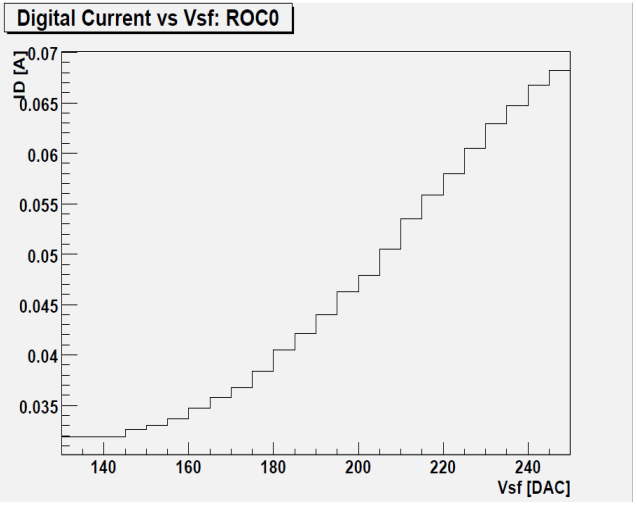
Vsf scan [VsfScan]

- Set high Vcal (CtrlReg=4) and default Vsf
- Fix 1 row. Check 5 columns in the row and find the one with a smallest deviation of linearity parameter from its mean (calculated from 5 col.)
  - Measure PH for Vcal [25 – 256]
  - Fit the curves with hyperbolic tangent function $y = P3 + P2 * \tanh(P0 * x - P1)$
  - Par(1) is a linearity degree (=1 if linear)
  - Find col. with a min. difference between mean and linearity parameter
- Arm one pixel in chosen column. Scan Vsf [130 – 250] with step=5
- Measure PH for Vcal [25 – 256] for each Vsf value
- Fit the curves with hyperbolic tangent function
- Plot linearity degree and ID since Vsf affects the digital current
- ~1 min. test

Chip2, Col5, Row5



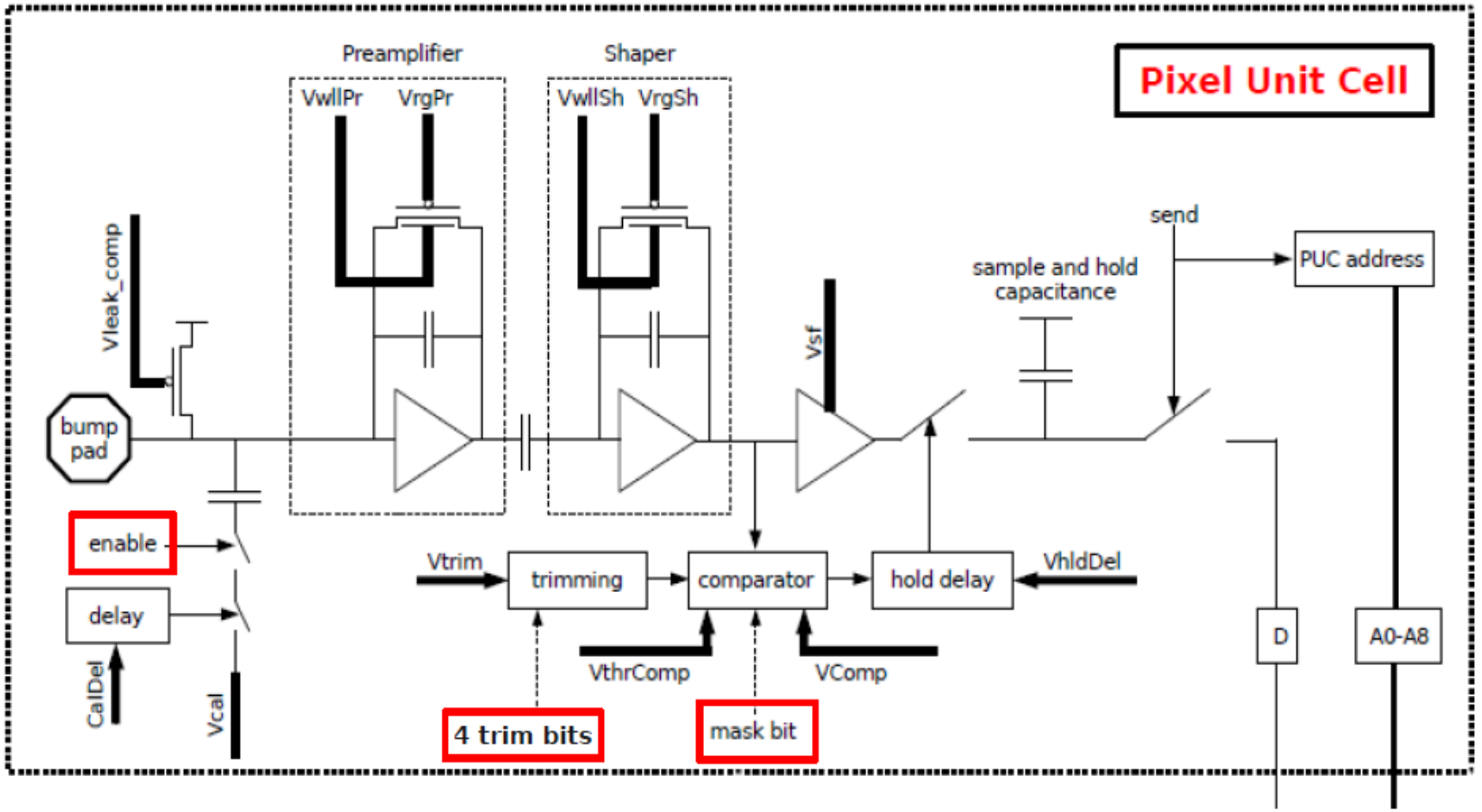




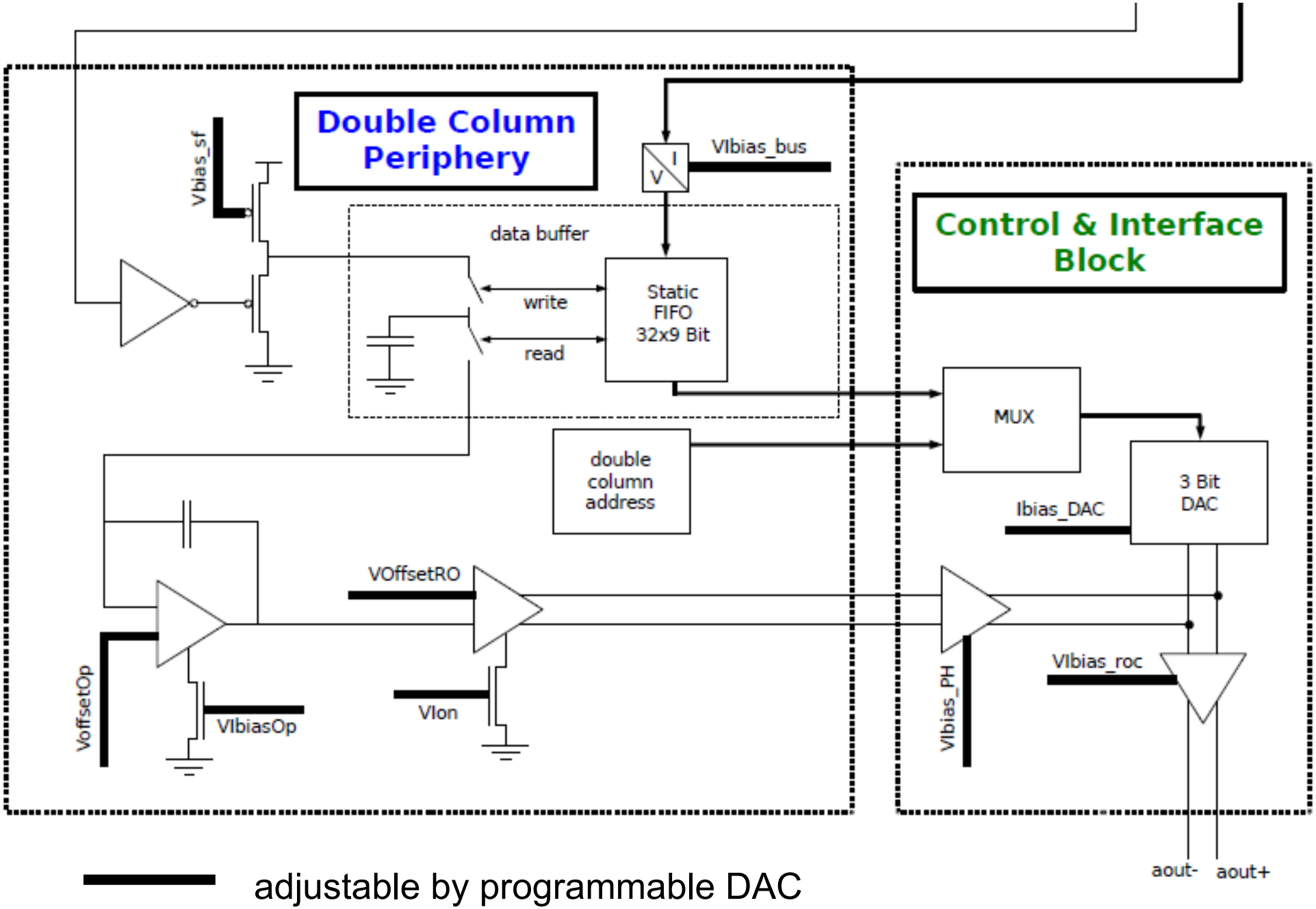
Summary

- CalDel and Thr efficiency tests are showing reasonable results
- Temperature and Temperature Calibration tests with JUMO seems to be understood. Possible to use at DESY ?
- Also presented: HldDel optimization procedure, Vcal linear range check, ID dependence on Vsf

Psi46 Pixel Readout Chip



psi46 pixel readout chip



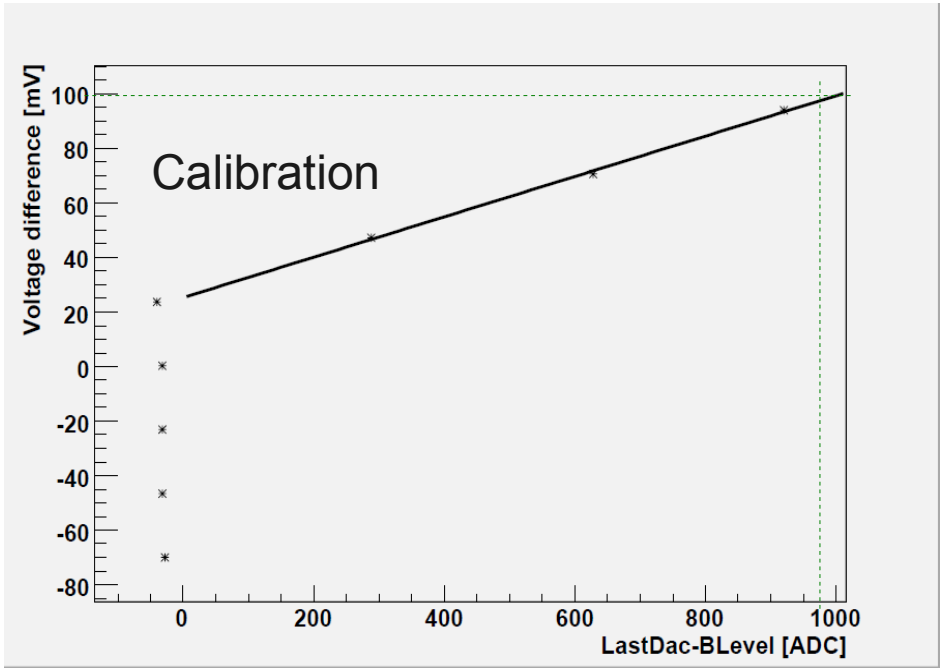
adjustable by programmable DAC

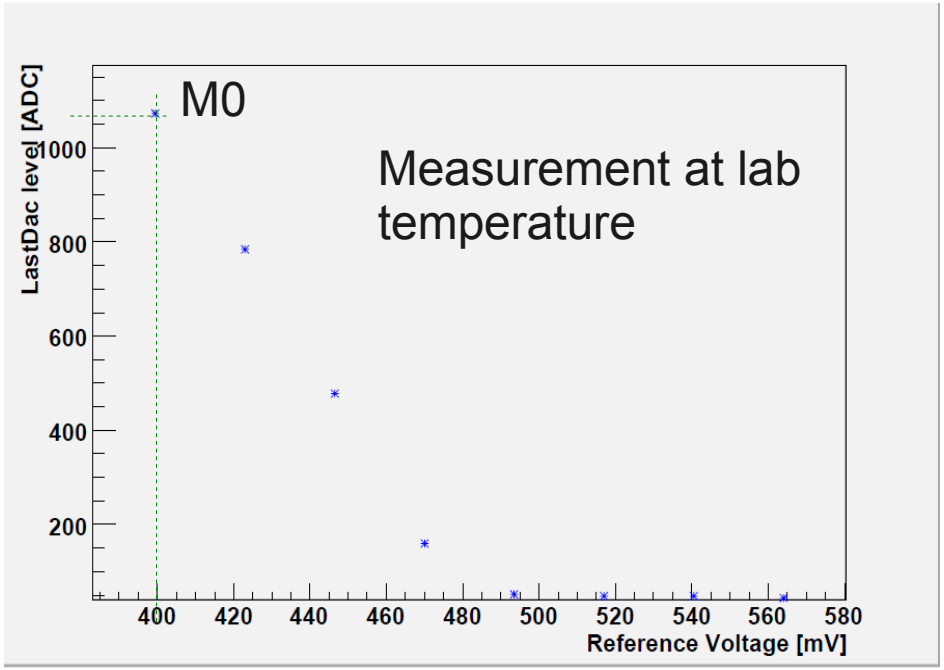
psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

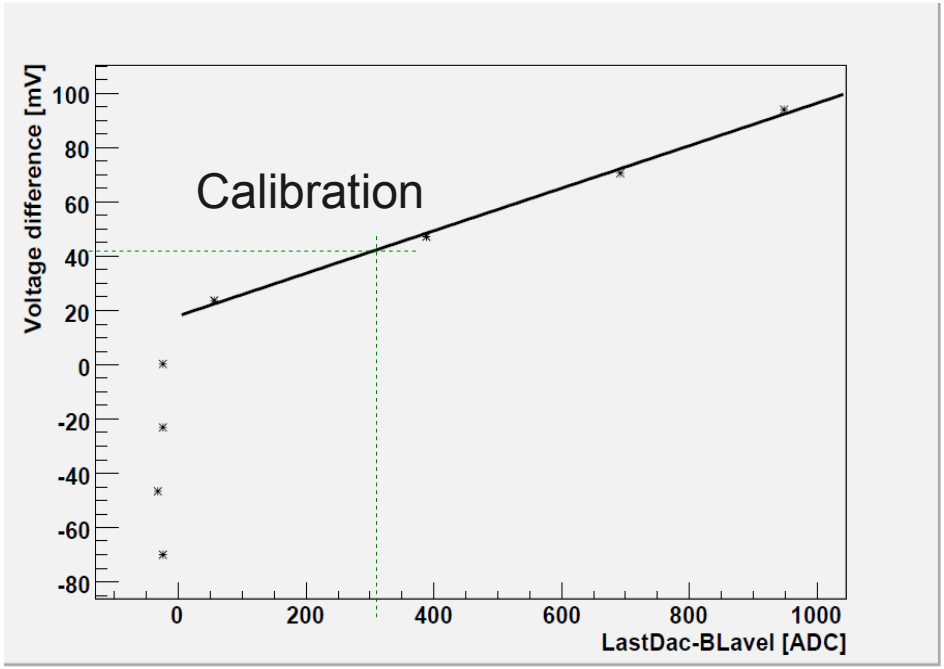
Temperature test results (Chip 2)

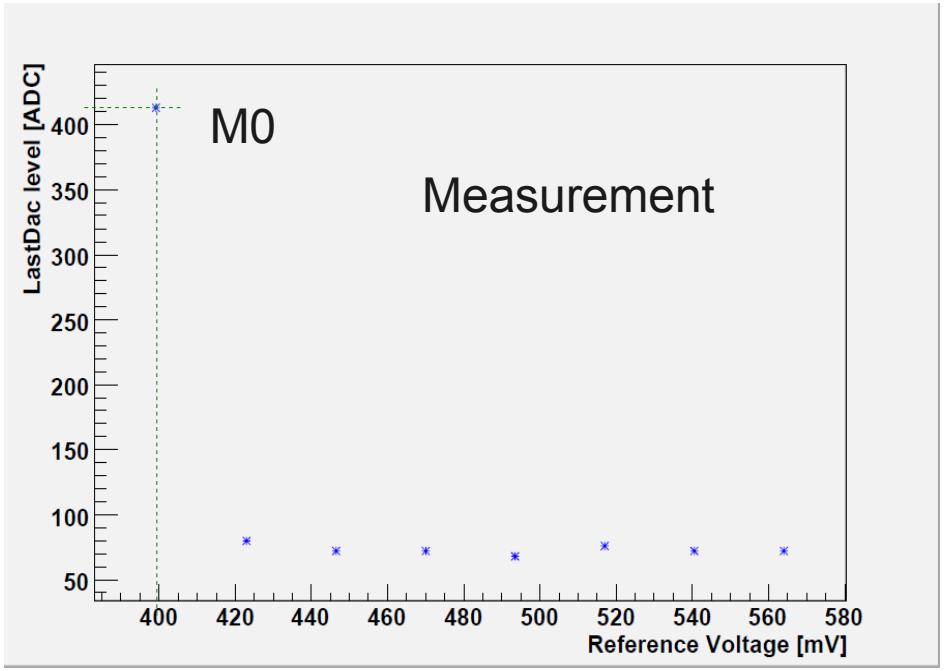




- Example, Chip 2:
  - Ref. V = 400, LastDac = 1068
  - V = 400 + fit->Eval(M0 – blackLevel) = 400 + fit->Eval(1068 – 76) = 499 mV
  - T = 0.625 · (V – 470) = 21°C

Temperature test results (Chip 6)





Only 1 measurement is possible. Measured LastDac value is ~3 times lower compare to Chip 2. Different T sensor is used ?

- Example, Chip 6:
  - V = 400 + fit->Eval(M0 – blackLevel) = 400 + fit->Eval(412 – 100) = 442 mV
  - T = 0.625 · (V – 410) = 20°C
  - Used for Chips 6, 7 – original parameterization from PSI