AGH University of Science and Technology

AIDA
Status of Readout Electronics and Future Plans

Marek Idzik AGH-UST

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

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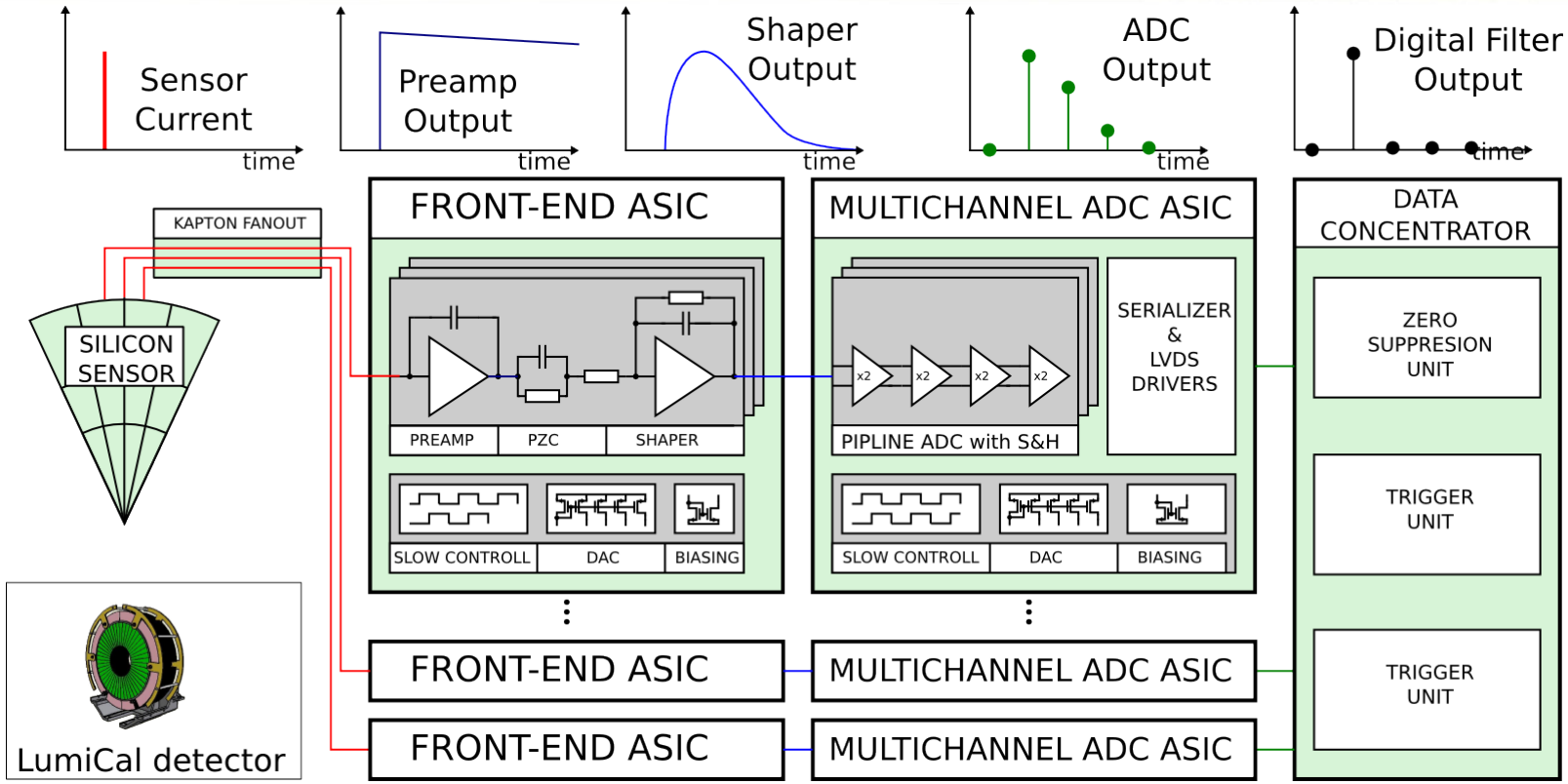
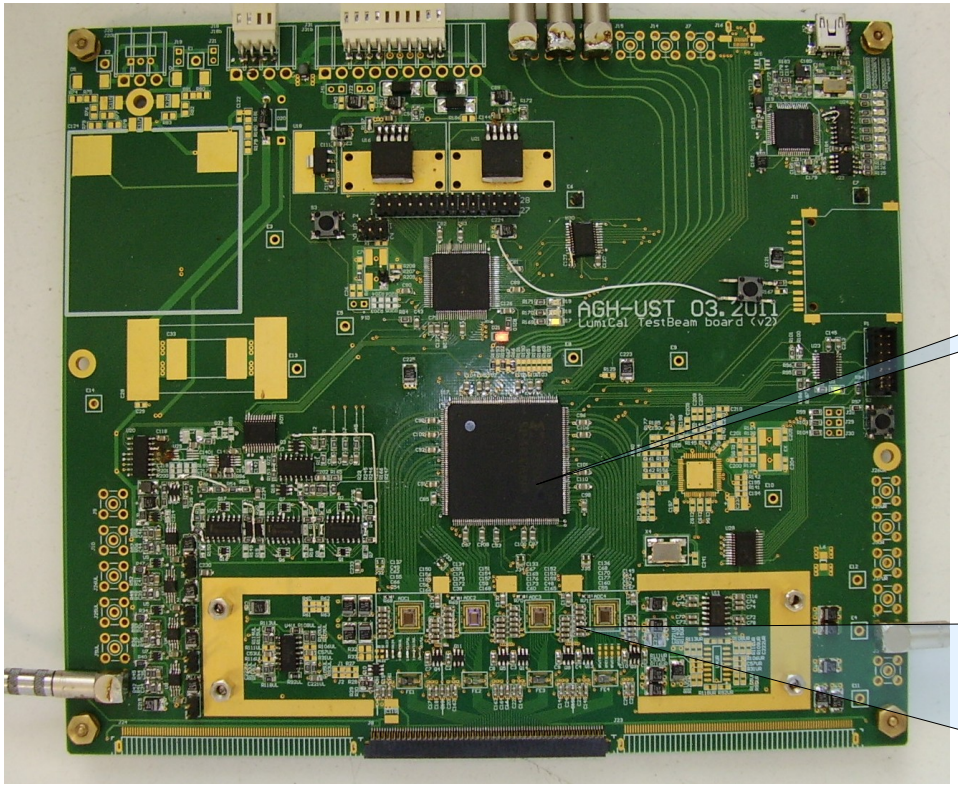
Present Readout of LumiCal detector



In last few years a multichannel readout comprising the front-end and ADC in each channel has been developed. Prototypes of 8 channel FE and ADC ASICs in AMS0.35um CMOS, plus FPGA based data concentrator, were integrated in the 32 channels system.

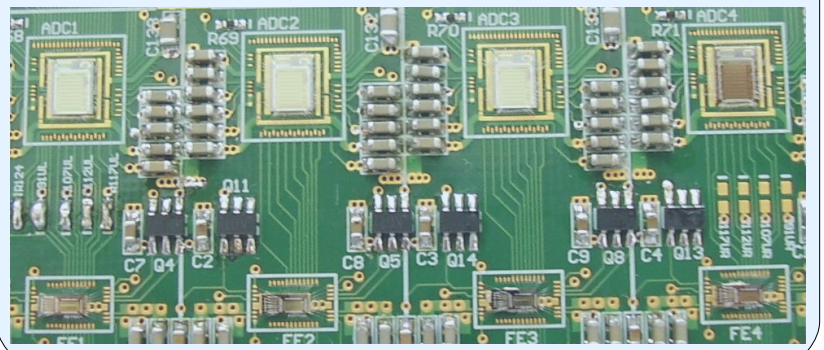
32 channels readout module

4 FE ASICs + 4 ADC ASICs + FPGA concentrator + Power pulsing



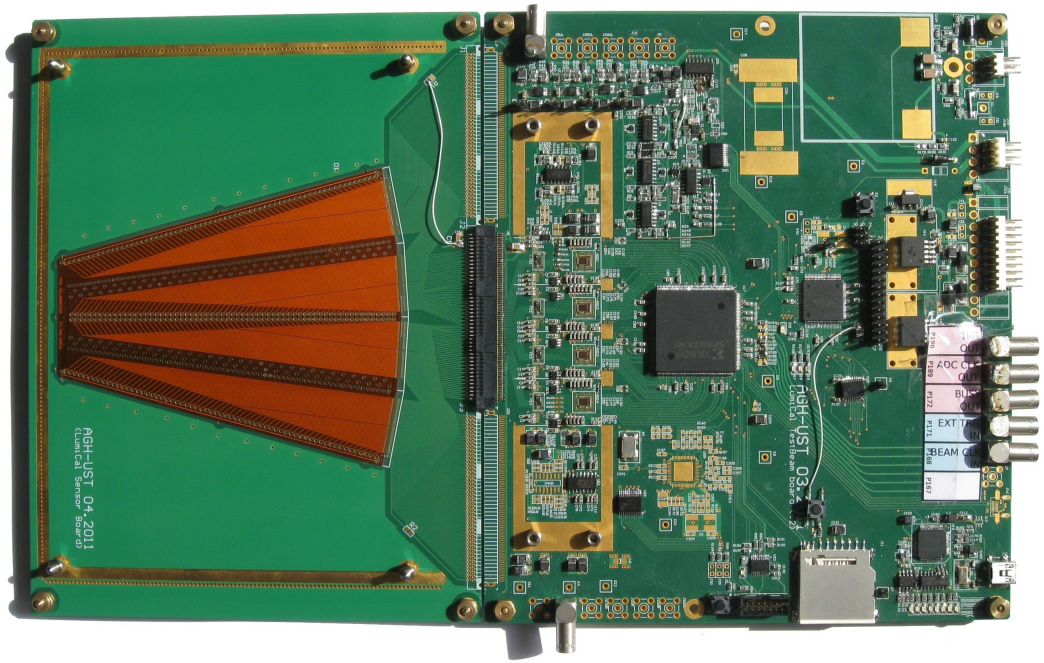
Data concentrator
Xilinx Spartan 3E

4 pairs of front-end + ADC



Paper on readout module accepted as Technical Note in JINST

LumiCal detector module



Good performance of detector module verified on 2 testbeams in 2011

Power pulsing (1ms_ON/199ms_OFF, ASICs Power_ON/OFF ~40)

Two modules available (Cracow, Zeuthen), with two sensor boards (BeamCal, LumiCal)

Using deconvolution, tests for CLIC are performed with asynchronous readout

This is THE detector prototype for 2012 or more...

Ongoing activities and future plans

- Analyses of testbem data in progress (Sz. Kulis in Cracow, other ??)
- Various ideas for improved readout, but first:
  - New ASICs needed
  - Sz. Kulis needs to write PhD thesis
- **Design of new, very low power, radiation hard, FE and ADC ASICs in IBM 130nm for ILC/CLIC**
  - Design of FE and ADC in progress
  - IBM 130nm VERY UNFRIENDLY technology, we are delayed...
  - In 2012 we would like to submitt both FE and ADC prototypes with few (~8) channels
  - In 2013 we would like to be ready for multichannel prototypes (there is no money for it...)
- Further plans after first IBM130nm submission...