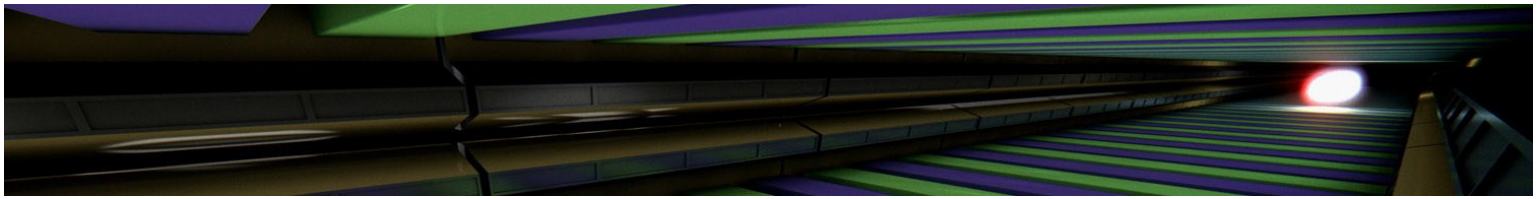


FPGA Experts Group, Framework developments and concepts

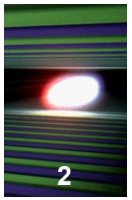
Patrick Gessler

European XFEL

WP75 and WP76

European XFEL

Agenda



- The FPGA Experts Group
- Repository and documentation platforms
- Framework developments
  - Start-up projects and software tools
  - Simulink based FPGA programming framework
- Difficulties and open issues

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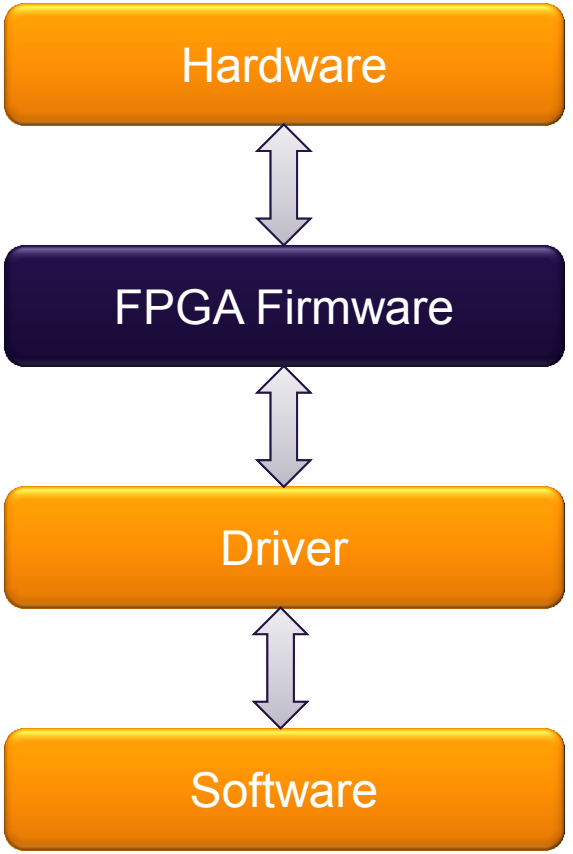
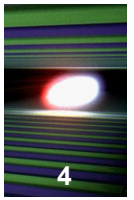
FPGA Experts Group - Goals

- Standardizing Interfaces
- Build up a framework
- Provide support
- Centralize
  - Documentation
  - Source code
- Exchange of knowledge
- Trainings
- Bi-weekly meetings
- Goals:
  - Reduce time and costs
  - Increase maintainability



FPGA Experts Group - Participants



- Currently ~40 persons on mailing list
- Around 20 participants on regular meetings from
  - XFEL
  - DESY Groups like MSK, MCS, NIM, MDI, FEA, …
  - UCL
  - STFC
  - Heidelberg University

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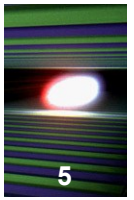
FPGA Experts Group - Activities



- Regular meetings
  - With talks and discussions
  - Every 2nd and 4th Friday in a month
  - Also available via EVO
- Organized Trainings and Tutorials
  - VHDL and Xilinx Virtex 5 technology (Q1 2011)
  - Plan Ahead, Partial Reconfiguration, Timing Constraints (Q4 2011)
  - Start-up Projects Tutorial (Q1 2012)
  - Planning of intensive VHDL course with HASYLAB (Q3 2012)
- Collaborative work on framework and tools

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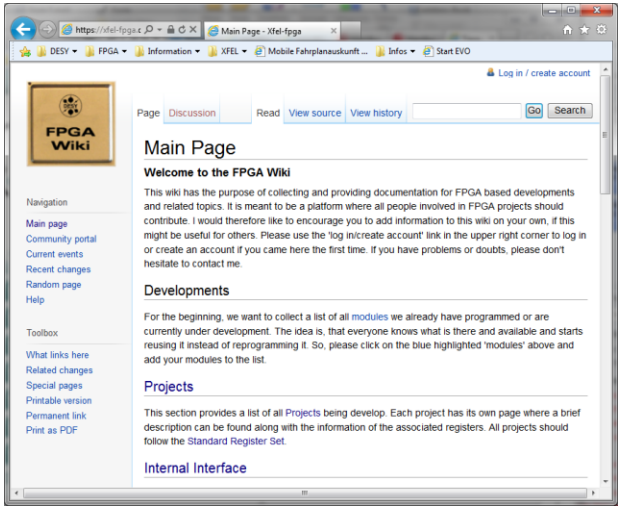
Repository and documentation platforms

- Source code repository for firmware
  - Subversion repository https://svnsrv.desy.de/desy/FPGA
  - Hosted by IT DESY Zeuten
  - Used to save and track all firmware projects

- Documentation and reference platform
  - FPGA Wiki http://xfel-fpga.desy.de
  - Hosted by IT DESY
  - Collect all information related to
    - Hardware
    - Interfaces
    - Projects
    - …



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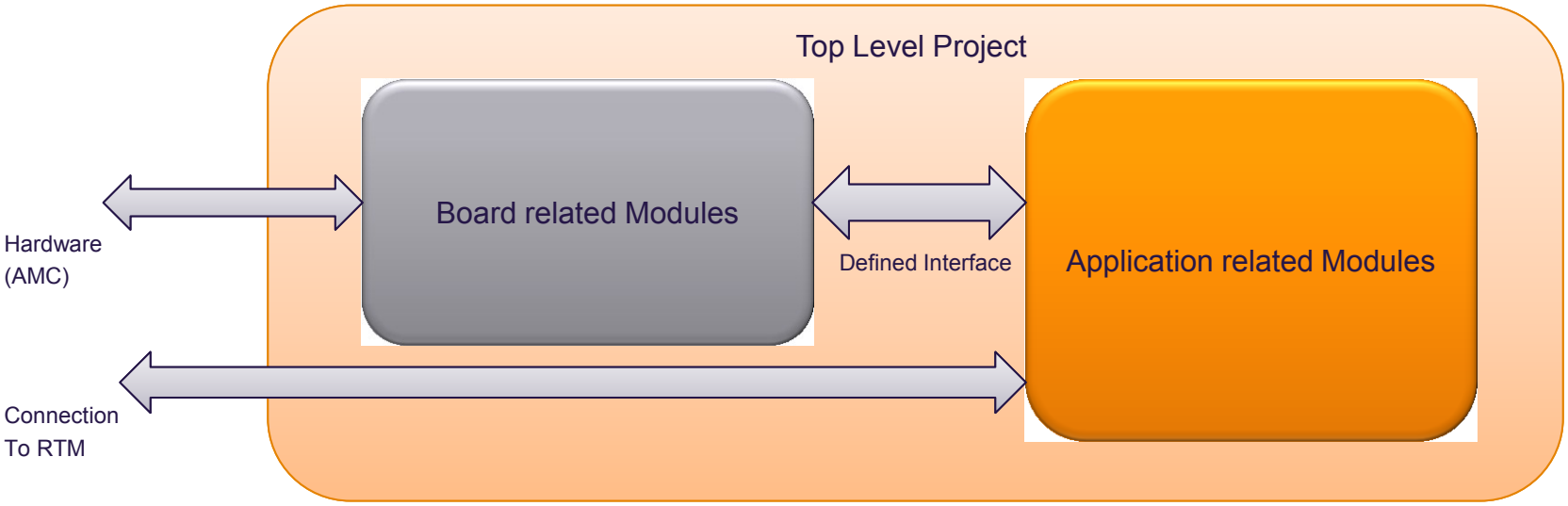
FPGA Framework – Start-up projects concept

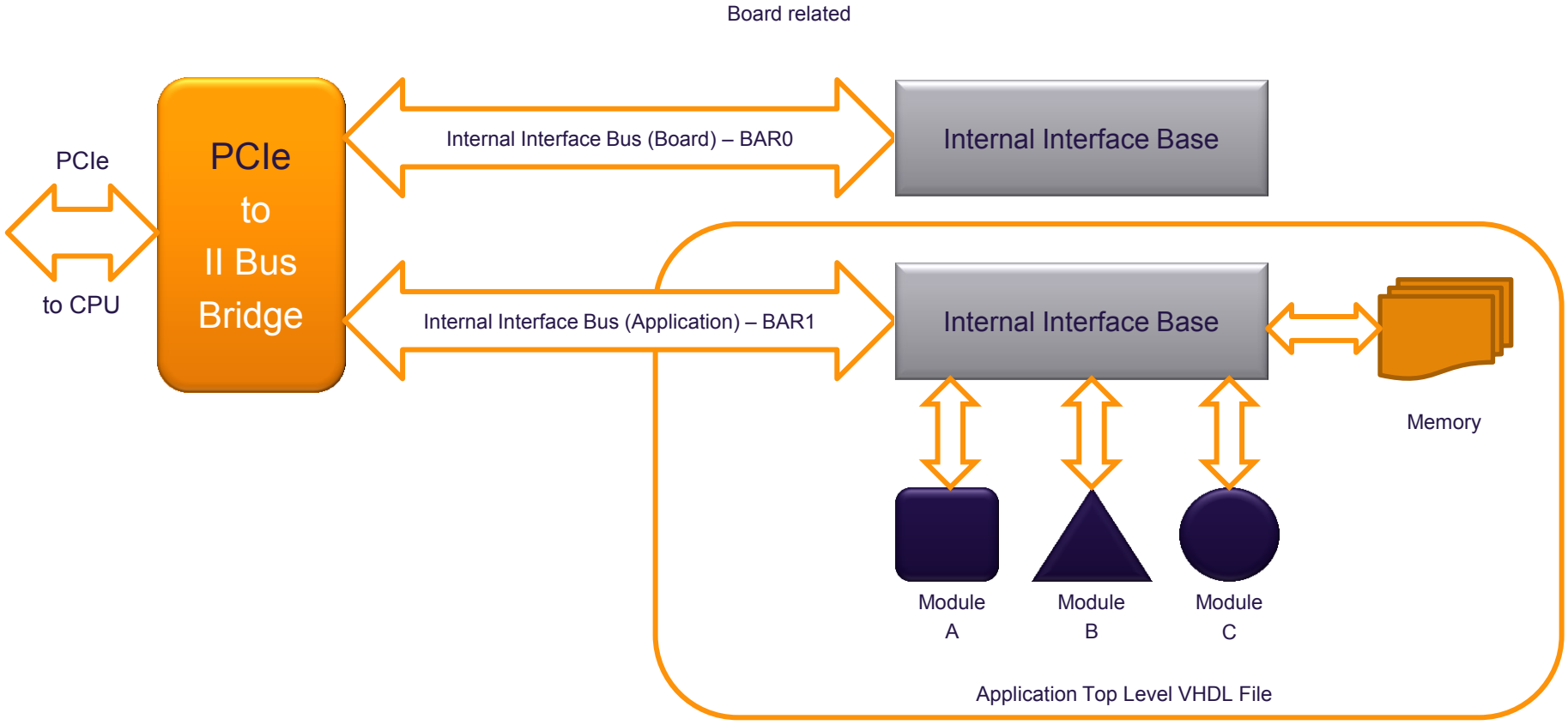


Original idea from Wojciech Jalmuzna (DESY)
(Board Support Package)

- First versions are available for
  - SIS8300 (→ https://svnsrv.desy.de/desy/FPGA/Projects/Boards/SIS8300/SIS8300_STARTUP)
  - DAMC2 (→ https://svnsrv.desy.de/desy/FPGA/Projects/Boards/DAMC2/DAMC2_STARTUP)

The core implementation is based on the intensive work done by W. Jalmuzna and colleagues

FPGA Framework – Internal Interface Bus



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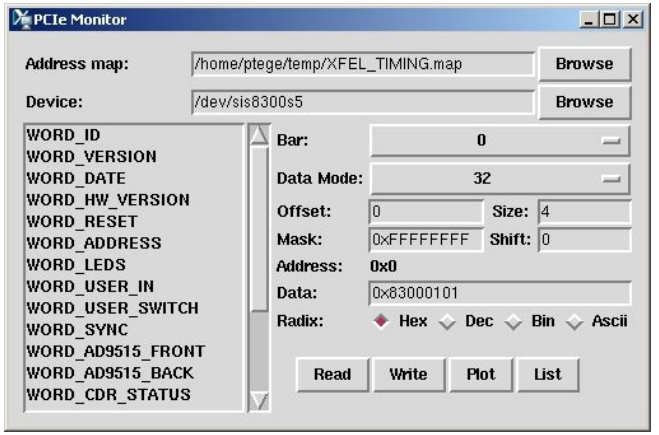
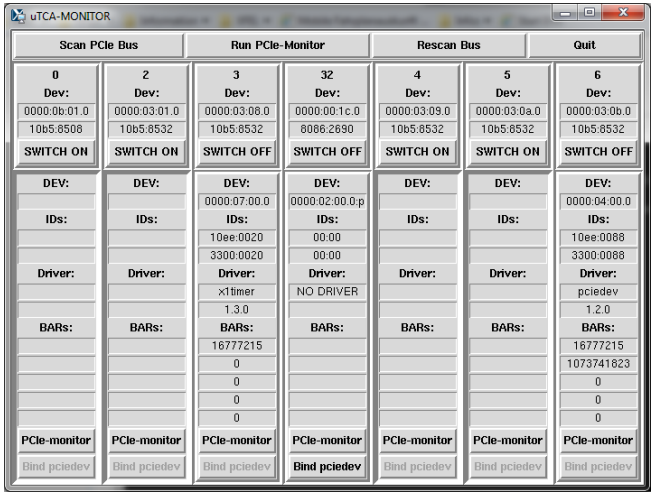
FPGA Framework – Simple software tools

- PCIe Monitor (Communication with Hardware)
  - Uses MAP file (generated from VHDL)
  - Register access
  - Plot of memory data
  - List of memory data



- UTCA Monitor (Communication with PCIe Hotplugging Driver)
  - (Dis-)connect PCIe endpoint in FPGA
  - Information about installed AMCs
  - Temporary development driver assignment



- Command line tools
  - pcie_rd, pcie_wr, firmware upload
  - Scripts for certain AMCs

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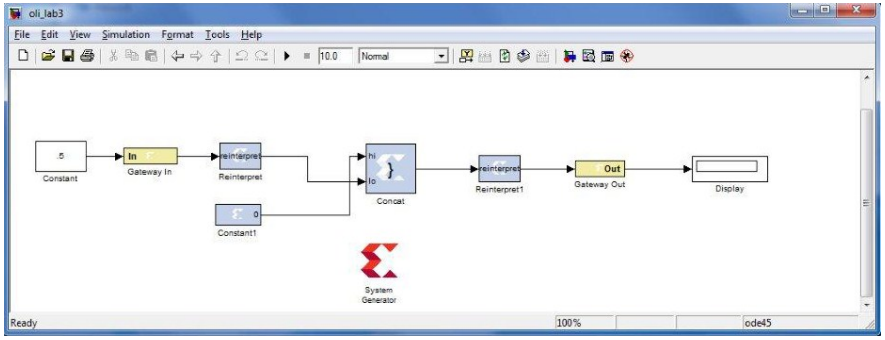
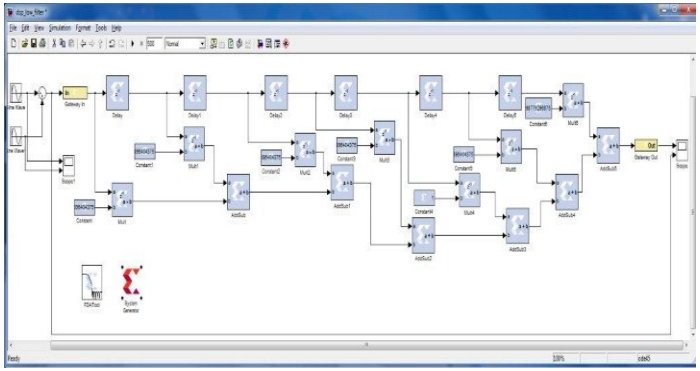
FPGA Framework – Simulink

- Using Simulink as programming environment for FPGA Algorithms
- Advantages
  - Easy to learn und use for non FPGA experts
    - ➔ **In most cases algorithm designers are not FPGA programmers**
  - Allows complete simulation
    - ➔ Input and output of Matlab data
    - ➔ Uses exactly the same quantization and resolution as the FPGA
    - ➔ Hardware co-simulation possible
  - Optimized modules available from FPGA vendor (~100 blocks)
  - Allows hierarchical designs and own modules





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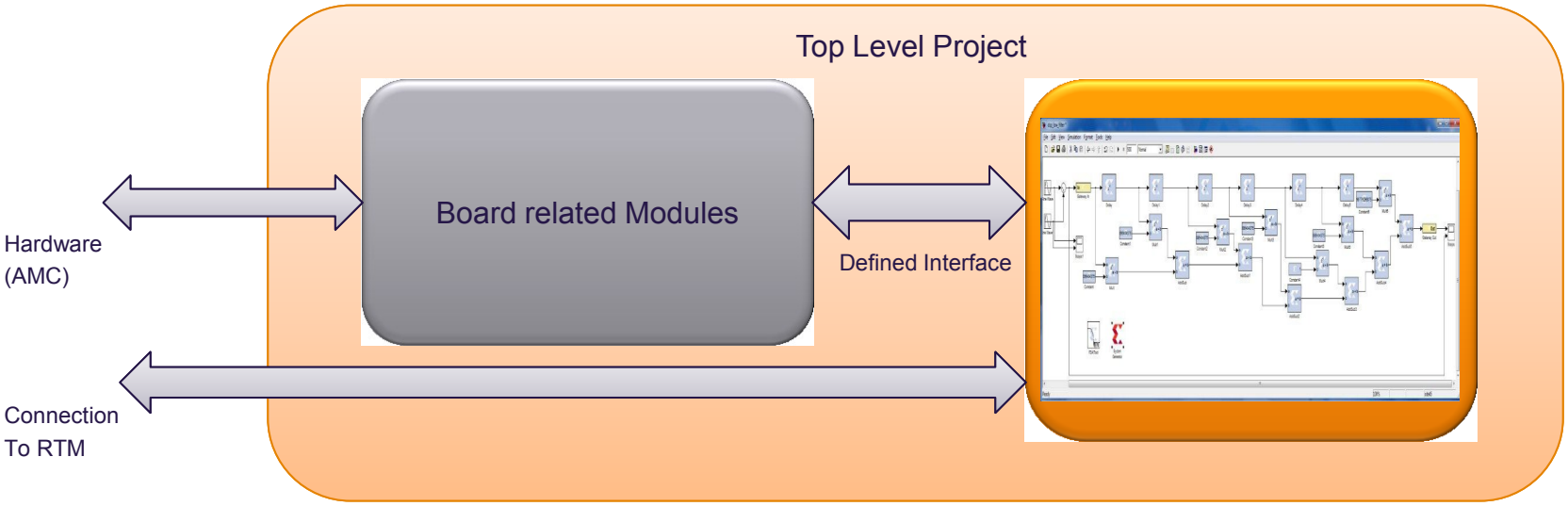
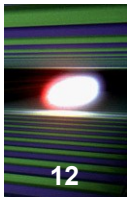
FPGA Framework – Simulink



- First test and implementations where done in Q4 2011
- Currently a full application is implemented (using SIS8300)
  - Including integration in Start-up project and II Bus

FPGA Framework – Simulink plans



- Integration with Start-up projects (special version)
- Development of optimized design flow and tools
  - Simplify bit file generation and deployment
  - Generation of MAP file information for Simulink part
- Build up a library of modules specialized to our applications
- Using partial reconfiguration for replacement of algorithms
- Include C to VHDL compiler into design flow

Difficulties and open issues

- Different source code repositories make life harder
  - MSK group and external collaborators have own repositories
  - At least regular copies to central repository are required

  → A structure change might be required

- Consistency of Start-up projects with W. Jalmuzna‘s work
  - There are currently slight changes in concepts (mostly file structure)
  - Current Start-up projects using version from end 2011

  →Harmonization is required

Time for questions…