Front-end Systems for XFEL

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DESY - MCS

- Outline
  - µTCA Hardware
  - DOOCS server organisation
  - Messaging and data handling
  - Status/Schedule

The XFEL will be based on µTCA

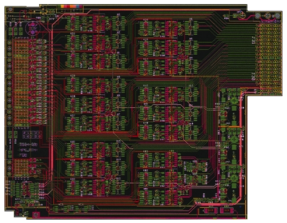


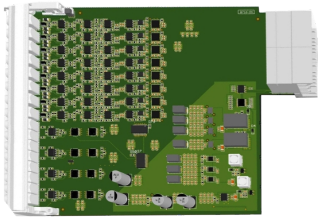
- Scalable modern architecture
  - From 5 slot single … 12 slot double size
- High availability
  - Redundant power and fan optional
  - Well defined management
- Differential links only: high analog signal processing quality

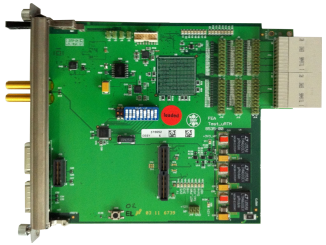
$$A = \frac{E[\text{Uptime}]}{E[\text{Uptime}] + E[\text{Downtime}]}$$

Several µTCA boards

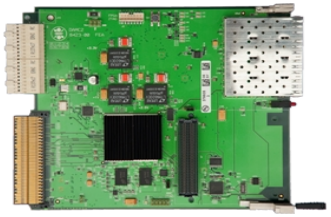
RTM

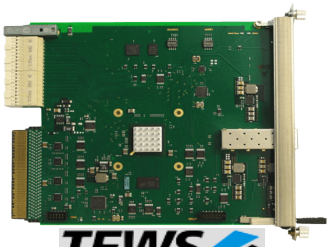






AMC

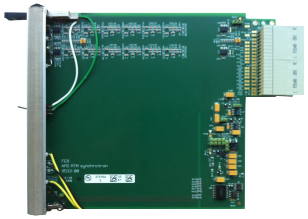


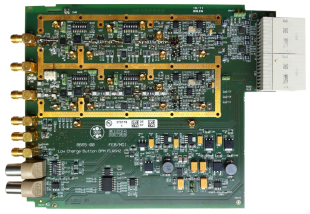


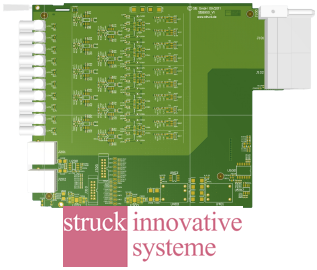
Digital Front

Analog Front

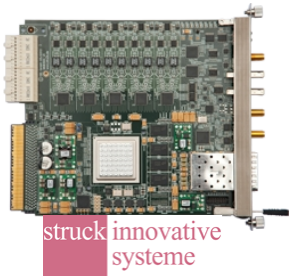
RTM





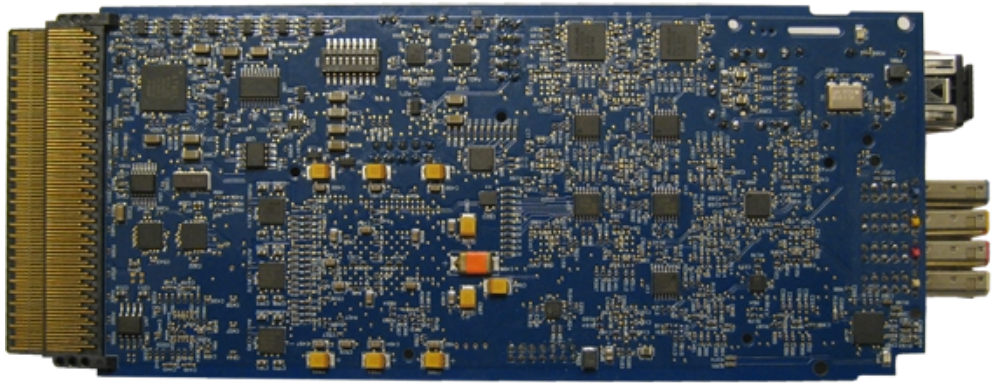


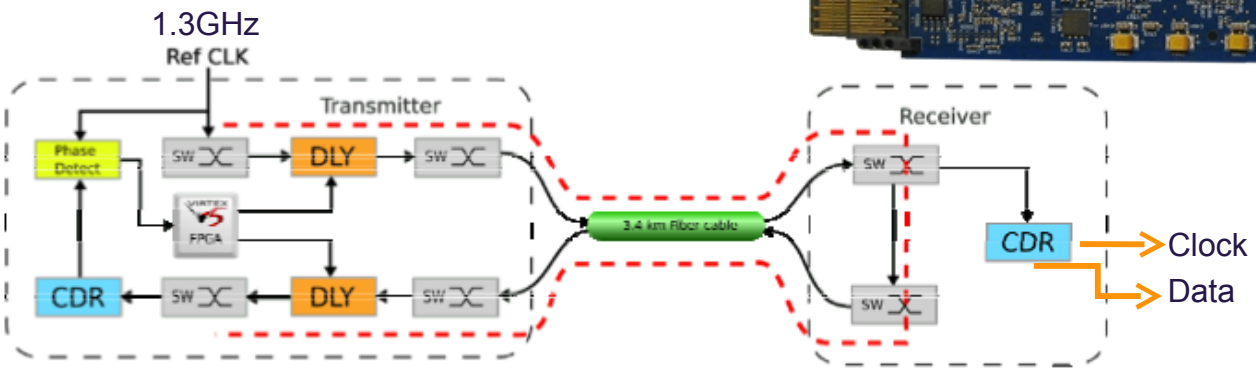
AMC



XFEL Timing System: 1. Prototype

- New timing system
  - Fiber optic links 1.3GHz
  - with drift compensation
  - AMC prototype is receiver and transmitter
  - ps stability (< 5ps RMS)
  - Clock, trigger and event distribution





Done by

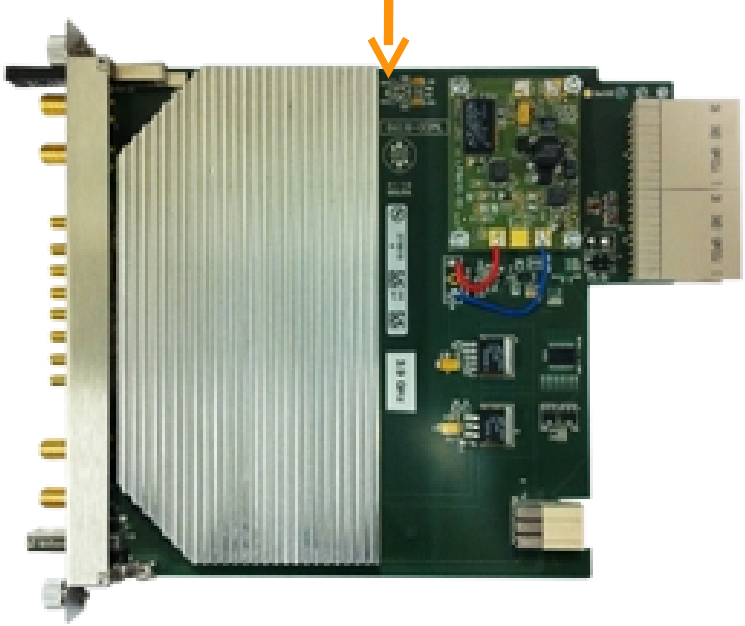
FYSIKUM

Hardware

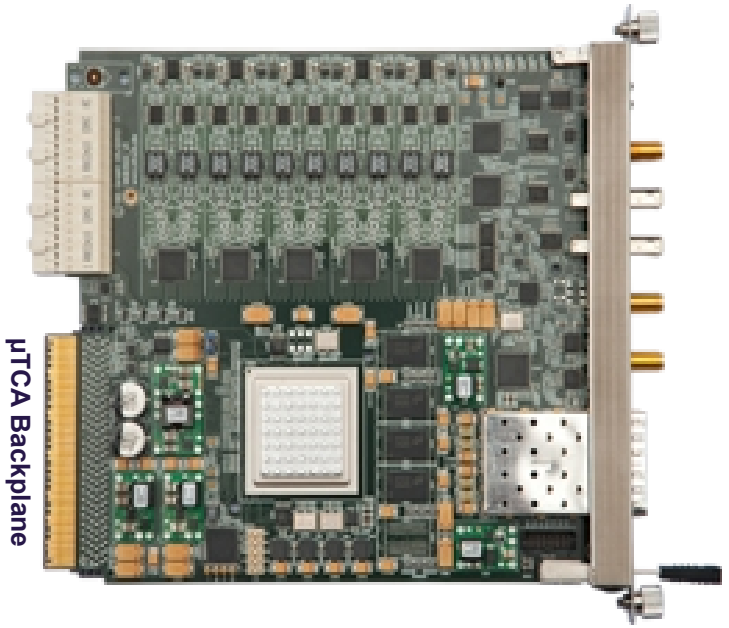
- XFEL will be based on the new MicroTCA.4 standard
  - Double size Advanced Mezzanine Card (AMC) modules with complex FPGA and PCIe link to CPU
  - Rear Transition Modules for signal conditioning

MTCA.4

PICMG

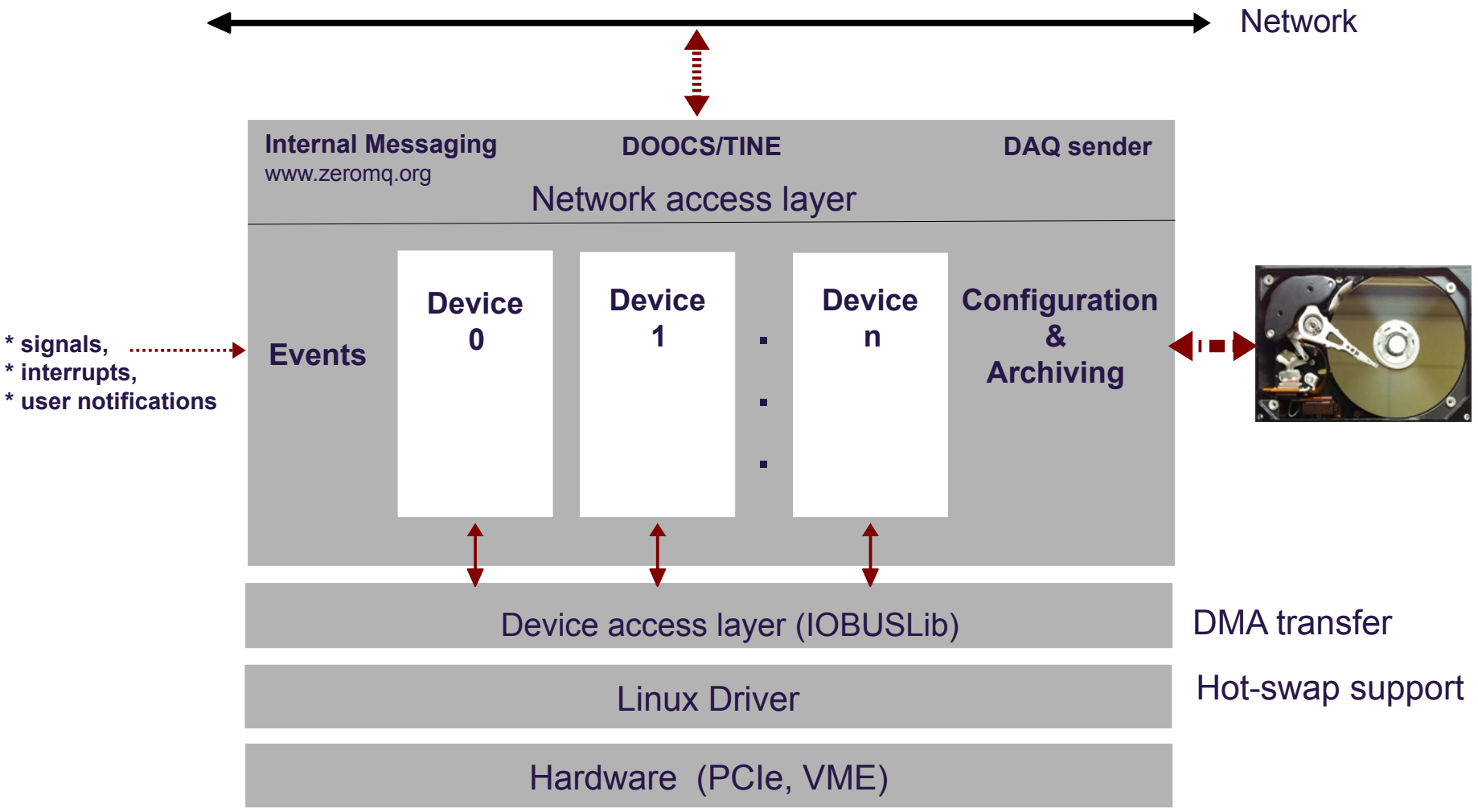


DWC8300 © DESY



SIS8300 © Struck Innovative Systems

DOOCS Server Organization



DOOCS Archiving System


```
TDS       tds;

tds.tm     = time;
tds.status = 0 // ok
tds.data   = data;

volt.hist.fill_hist (&tds);
```

History Property

D_hist volt.hist;
volt.filt

Archiver

Adaptive Filtering

Memory buffer

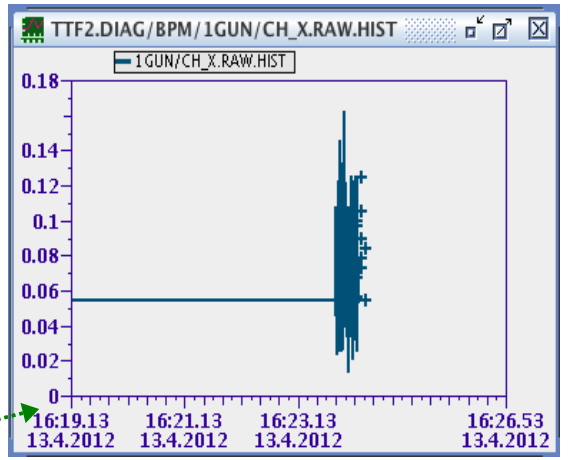
Archive File

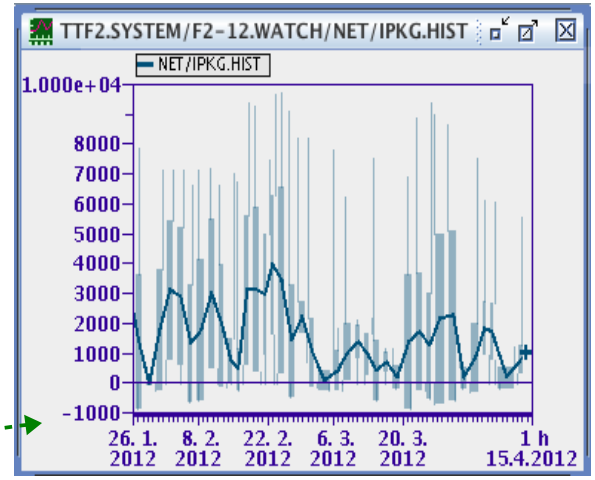
Adaptive Filtering

Ring buffer

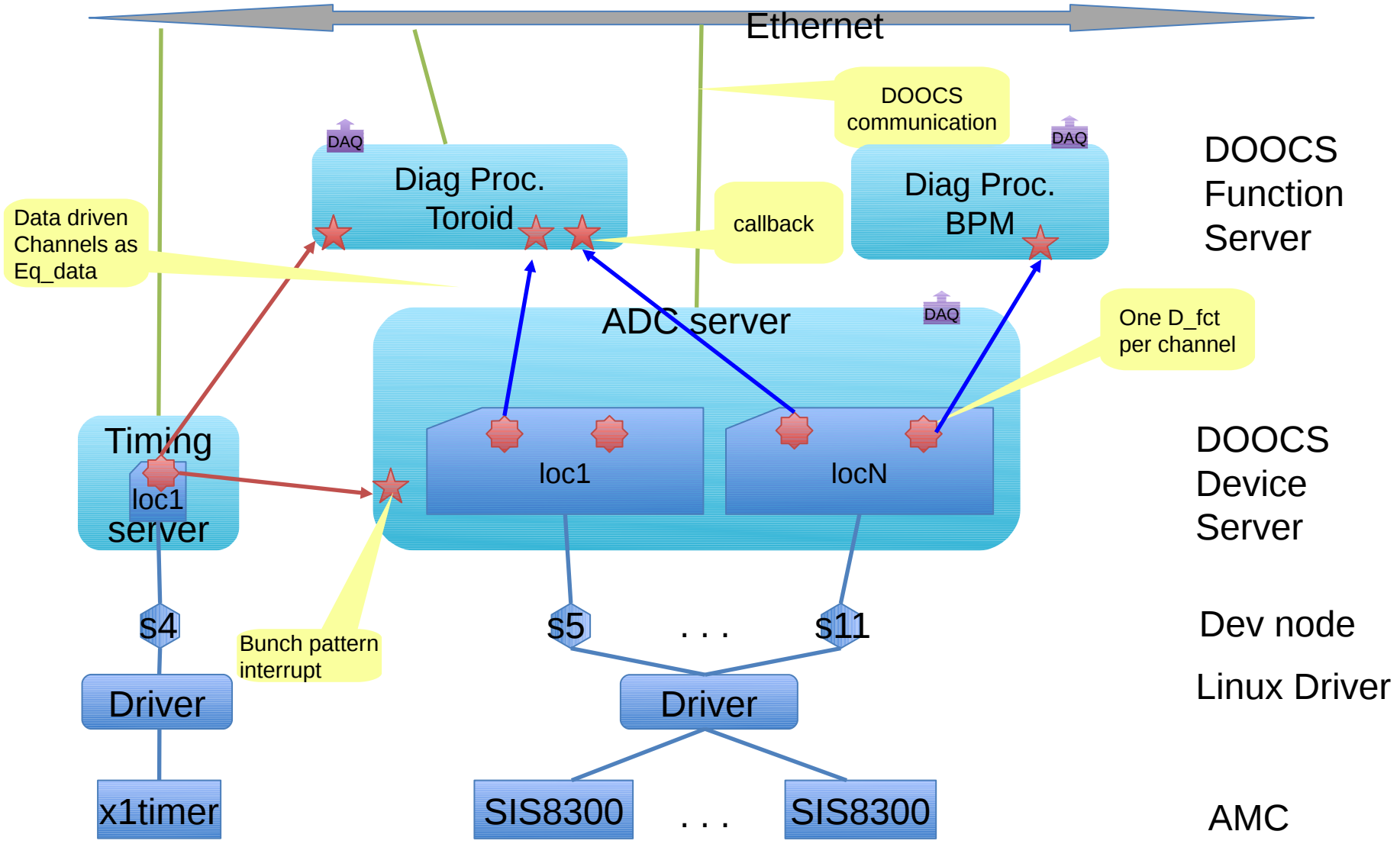
Long Time Archiver

Long time archive files

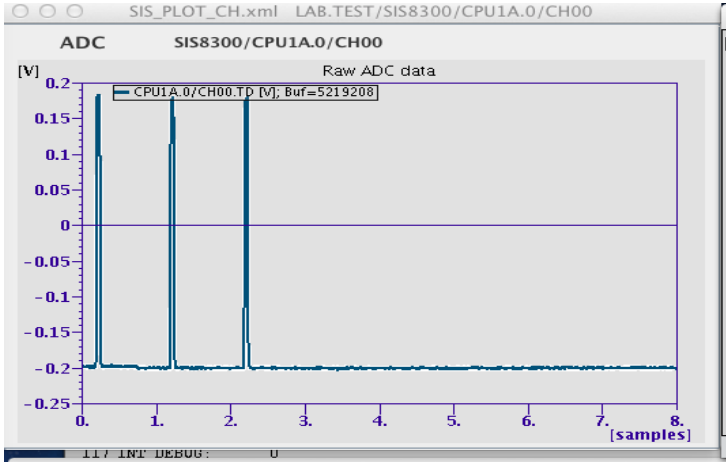


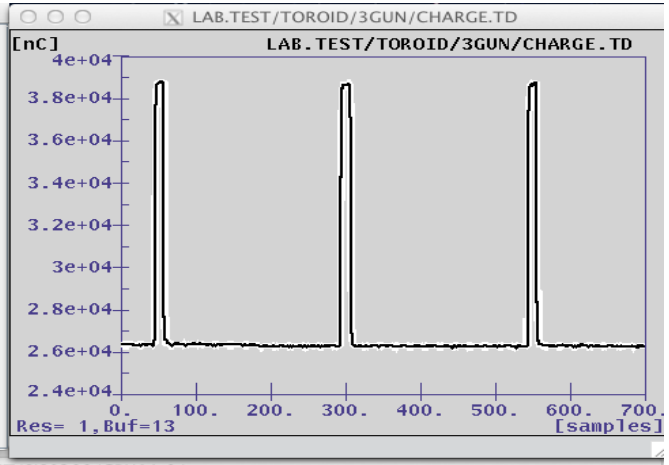


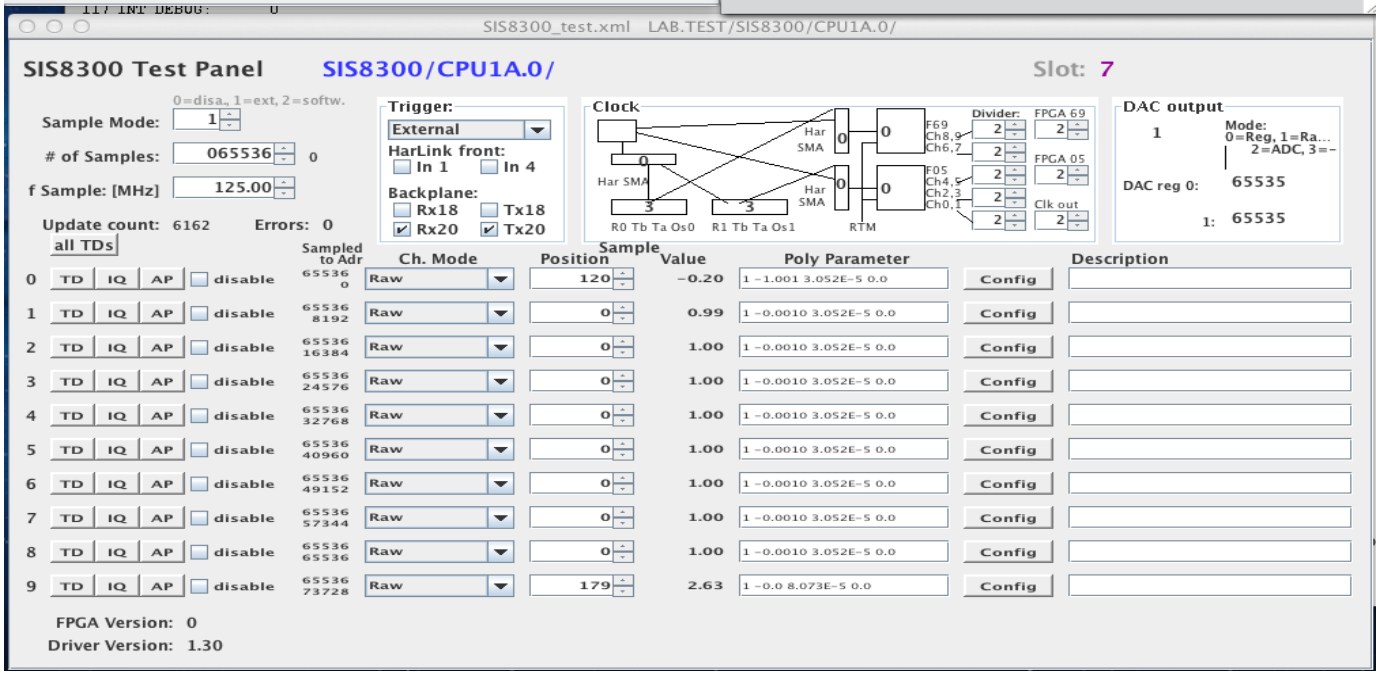
Front-end Architecture: example Toroid



Toroid server test set-up







Raw Signal from ADC

Charge reading from Toroid server

Configuration Panel for SIS8300

Some test results (very preliminary)

- On Core-Duo 1.5 GHz CPU (low end CPU)
- Source Code not yet optimized
  - Merging two 16bit word into one 32 bit integer
  - Additional buffer copy into Messaging system

- Test results (64 KB buffer, 125 MHz sampling, 10Hz operation)
  - SIS8300 DMA server with 80 ADC channels
    - ➔ ~60 % CPU usage, 5% Messaging system
  - Toroid Server with 80 locations
    - ➔ ~10 % CPU usage

- => only little overhead for the Messaging system

Status/Schedule

- µTCA Hardware available
- Messaging Software based on 0MQ include in DOOCS server library
  - First successful tests
  - Available May 2012
  - Need to implement a 16 bit array
- XFEL Timing system
  - First hardware available
  - DOOCS Server available in May 2012
  - Connection to FLASH timing in June 2012
- DMA Server for SIS8300 including Messaging Software under development
  - First test done
- Toroid Server including Messaging Software under development
- Complete installation planned for summer 2012 at FLASH