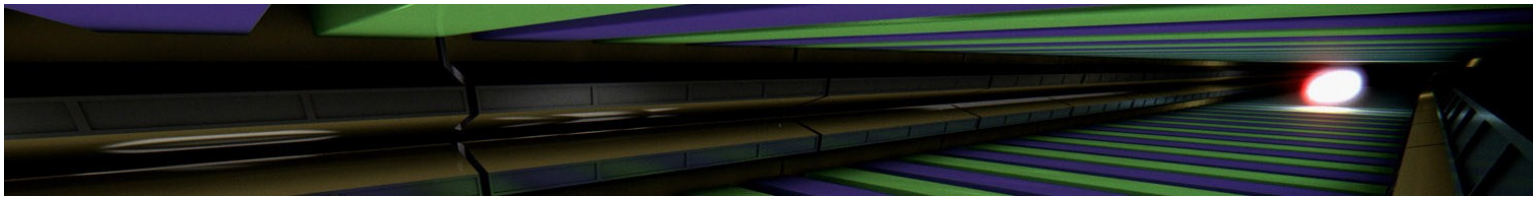


Electronic developments, concepts and applications for the Experiments and Photon Beam Line DAQ System

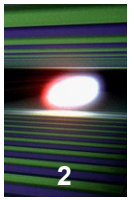
Patrick Gessler

European XFEL

WP75 and WP76

European XFEL

Agenda



- Instruments to be integrated in DAQ
- Requirements of the DAQ system
- Concepts, usage and developments
  - Beckhoff EtherCAT for slow control
  - MicroTCA.4 as main platform
  - ATCA for large scale systems (e.g. Train builder)
  - Special form factors for integrated systems (e.g. 2D detectors)
- Data processing and transmission concept
- VETO system for data reduction memory optimization

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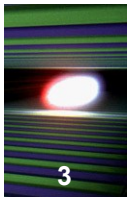
Instruments to be integrated in DAQ



- Optics (WP73)
  - KB mirrors for focusing
  - Refractive lens focusing
  - Monochromatic
  - Collimator
  - Slits
  - Attenuators
  - …
- Sample environment (WP79)
  - Particle injector
  - Cryostat
  - Precision stages
  - …
- Beam diagnostics (WP74)
  - Intensity monitors
  - Beam positioning monitor
  - Photon-electron spectrometers
  - K-monochromator
  - Screens and cameras
  - …
- Measurement instruments (WP8x)
  - e- and ion TOF
  - Point detectors
  - Spectrometers
  - …
- Laser systems (WP78)
  - Pump laser and diagnostics
  - …
- Vacuum systems (WP73)
  - Turbo pumps
  - Ion pumps
  - …
- Detectors (WP75)
  - AGIPD
  - LPD
  - DSSC
  - pnCCD
  - …

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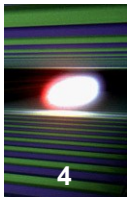
Requirements of the DAQ system



- High data volume to be processed and saved

Detector type	Sampling	Data/pulse	Data/train	XFEL/sec	LCLS/sec
1 Mpxl 2D camera	4.5 MHz	~2 MB	~1 GB	~10 GB	~300 MB
1 channel digitizer	5 GS/s	~2 kB	~6 MB	~60 MB	~0.2 MB

- Possibility to save all acquired data (but should be avoided)
- Scalability (combination and number of applications)
- Remote control and monitoring
- Extension and replacement during operation
- Early data processing and reduction
- Compatibility to machine hardware (e.g. Timing)

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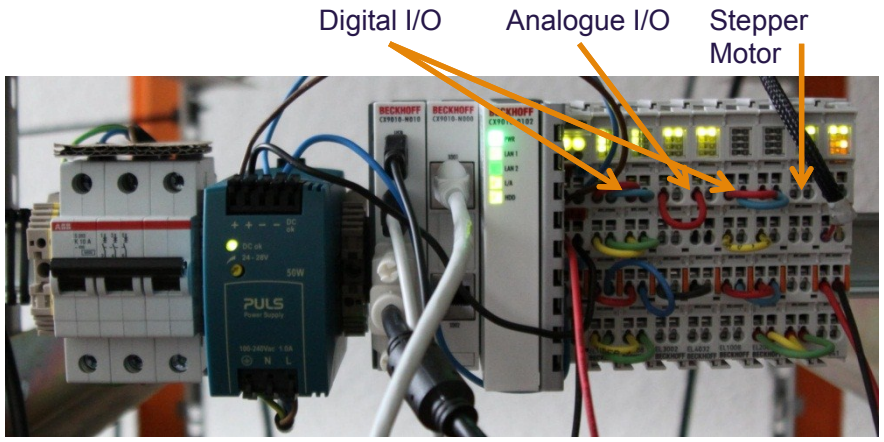
Beckhoff EtherCAT for slow control (N. Coppola)

- Integration of Beckhoff EtherCAT PLC rails in DAQ and control systems
- Allows complete software and hardware redundancy, steering and complete synchronization of slow varying quantities (~100 Hz)
- Real time Ethernet based control is widely used at light sources
- Usual systems to be controlled or values acquired
  - Digital I/O quantities
  - Analog I/O quantities
  - Environmental quantities
  - Synchronized and unsynchronized movements of motors for positioning at the highest resolution
  - Vacuum pumps
  - Vacuum gauges
  - Synchronized with Timing System
  - Interfacing with MPS



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MicroTCA.4 as main platform

- MicroTCA.4 allows
  - High-bandwidth communication between
    - → Boards and CPU via PCIe
    - → Boards via point-to-point connections
  - Synchronization via Timing Receiver
    - → Trigger
    - → Clocks
    - → Machine parameters
    - → Bunch structure
  - Remote control and monitoring
  - Module changes during operation (Hotplu
  - Functional extension via RTMs

Clock & Control RTM
(University Collage London)

DAMC2 – Universal digital AMC
(DESY)

Timing System
(Stockholm University / DESY)

SIS8300 – ADC AMC
(Struck Innovative Systems)

MicroTCA Carrier Hub
(N.A.T.)

High-performance DSP and FPGA board
(DMCS/DESY)

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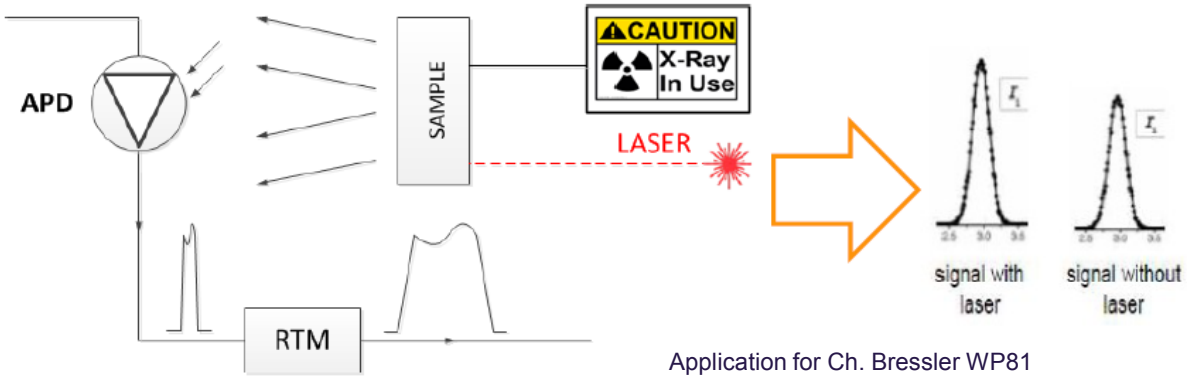
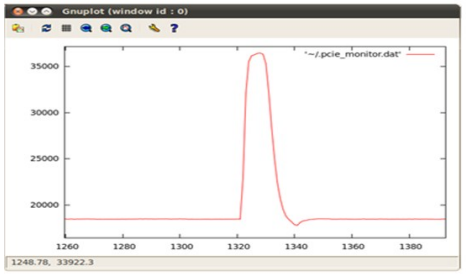
MTCA.4: Avalanche Photo Diode Project with SIS8300



Application for Ch. Bressler WP81

- Using a COTS ADC Module from Struck - widely used at XFEL (LLRF, BPM,…)
- A customized RTM had been developed in collaboration with Peter Goettlicher (DESY) for
  - Interfacing to the APD detector
  - Shaping the signal - increasing the pulse length and maintain the amplitude information
- Processing in FPGA or CPU and streaming of data
- System was tested with beam and APD module at Petra III (Good contact to P01 BL)
- Besides the foreseen use in WP81 it serves as an important test bed for
  - VETO source and related signal generation
  - Using Simulink for algorithm implementation
  - Device server implementation for MTCA.4



Curtsey: B. Fernandes (XFEL)

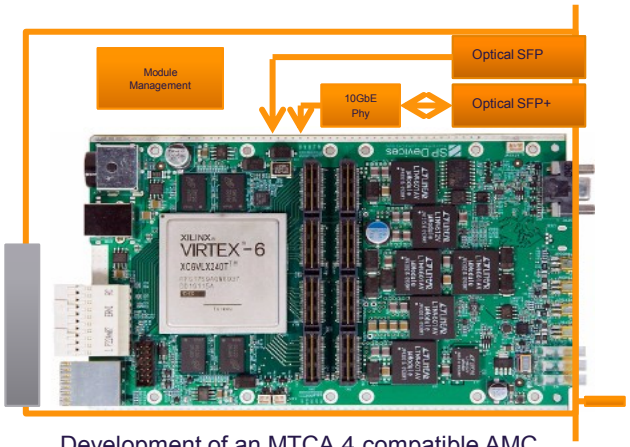
MTCA.4: High-Speed Digitizer developments

- A development with SP Devices Sweden AB just started

Product	Resolution	Maximum Sample Rate	Analog Bandwidth	Channels	On-Board Memory Size	Interface
SDR14	14bit in 14bit out	800 MSPS in 1600 MHz out	500 MHz	2 in 2 out	2 x 500 Mbyte	USB, cPCIe/PXIe, PCIe
ADQ108	8 bit	7 GSPS	2 GHz	1	1024 MS	USB, cPCIe/PXIe, PCIe
ADQ412	12 bit	1.8/3.6 GSPS	2/1.3 GHz	4/2	700 MS	USB, cPCIe/PXIe, PCIe
ADQ1600	14 bit	1.6 GSPS	800 MHz	1	500 MS	USB, cPCIe/PXIe, PCIe
ADQ DSP	-	-	-	-	1 GByte	USB, cPCIe/PXIe, PCIe

- They will design an AMC version of their digitizer family
  - Additional interfaces and MTCA.4 connectivity added
  - Final products expected end of Q4 2012

Existing Products
(PXIe/cPCIe, PCIe, USB)



Development of an MTCA.4 compatible AMC

Applications

- Photon Diagnostics
  - XGMD
  - XBPM
  - PES
- Detectors
  - 0D (e.g. APD)
  - 2D (e.g. pnCCD)
- Experiments
  - eTOF, iTOF

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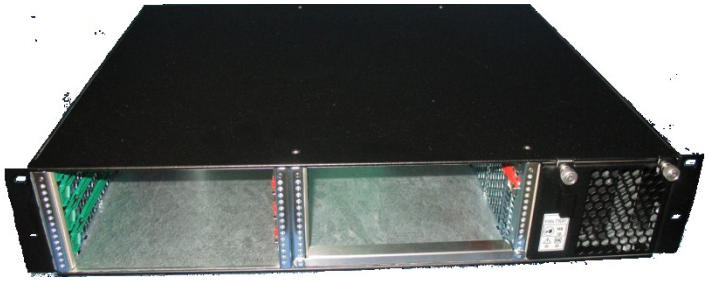
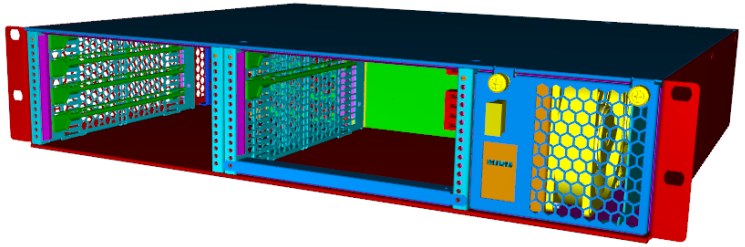
MTCA.4: 2U small crate with 6 slots

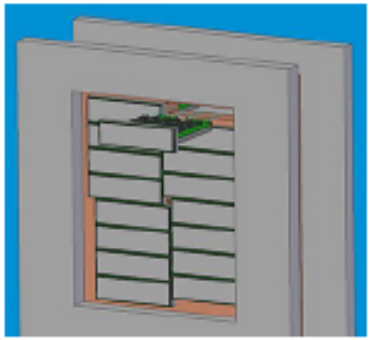
- Development with PowerBridge and Schroff
  - 2U high MTCA.4 crate with
    - 4 slots with double size AMC with RTM
    - 2 slots with double size AMC
    - 1 MCH
    - 1 Power Module
  - Prototype expected in May
  - When successfull, plan of
    - 4U high 12 slot version and
    - 6U high 12 slot version with full redundency





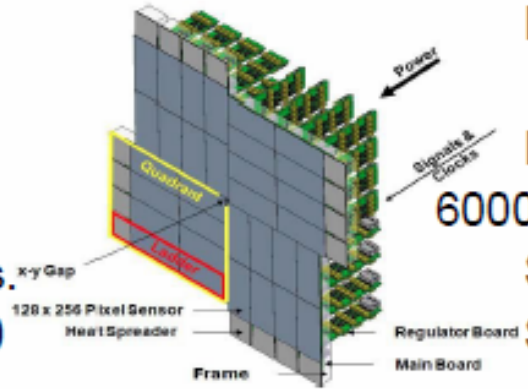
2D Detector developments

AGIPD Adaptive Gain Integrating Pixel Detector (AGIPD)



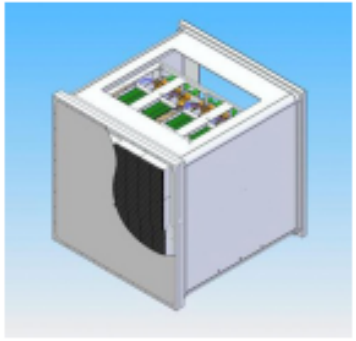
Energy range
3 - 13 keV
Dynamic range
10^4@12 keV
Single Photon Sens.
Storage Cells ≈ 300

DEPFET Sensor with Signal Compression (DSSC)



Energy range
0.5 - 6 keV (25 keV)
Dynamic range
6000 ph/pix/pulse@1 keV
Single Photon Sens.
Storage Cells ≈ 640

Large Pixel Detector (LPD)



Energy range
5 (1) - 20 keV (25 keV)
Dynamic range
10^5@12 keV
Single Photon Sens.
Storage Cells ≈ 512

Other Detectors

- 0D/1D detectors for high repetition rate applications (e.g. veto, dispersive spectrometers)
- Small areas, low rep. rate, low energy 2D imaging detectors
- Particle detectors (eTOF, iTOF)

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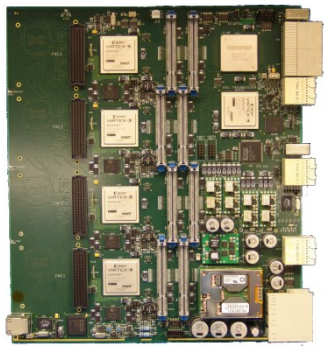
2D detector control and processing

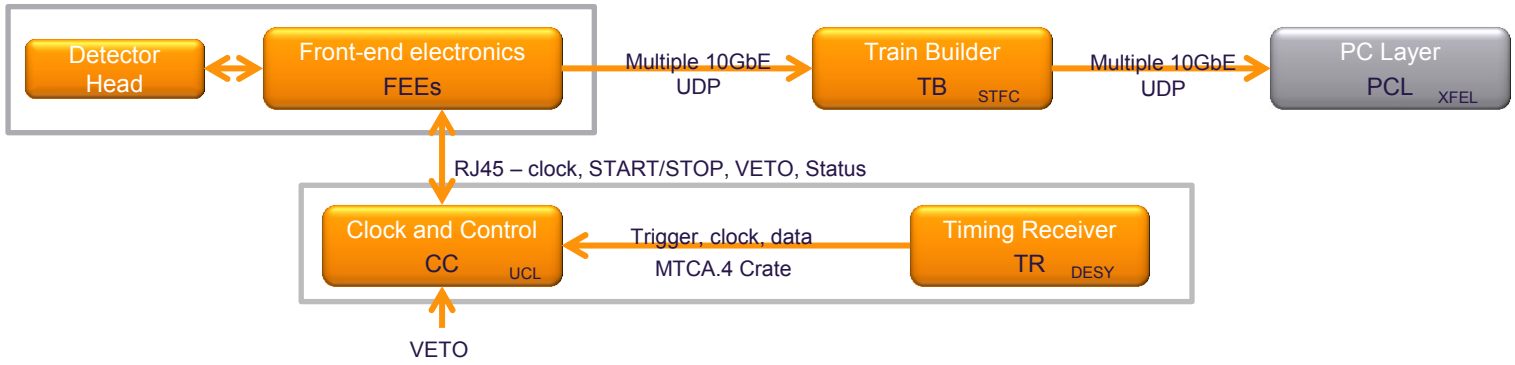
- Control and synchronization
  - Clock and Control RTM
  - Synchronized with Timing Receiver
  - One RTM controls a 1 Mpixel Detector
- Data reorganization and processing in Train Builder
  - Partial frames will be reassembled
  - A complete train put into memory
  - Transmitted via 10GbE to PC Layer
    - ➔ Dual 10GbE FMCs from DESY/FEA

Clock and Control RTM (UCL)

DAMC2 (DESY/FEA)



Train Builder ATCA Board (STFC)



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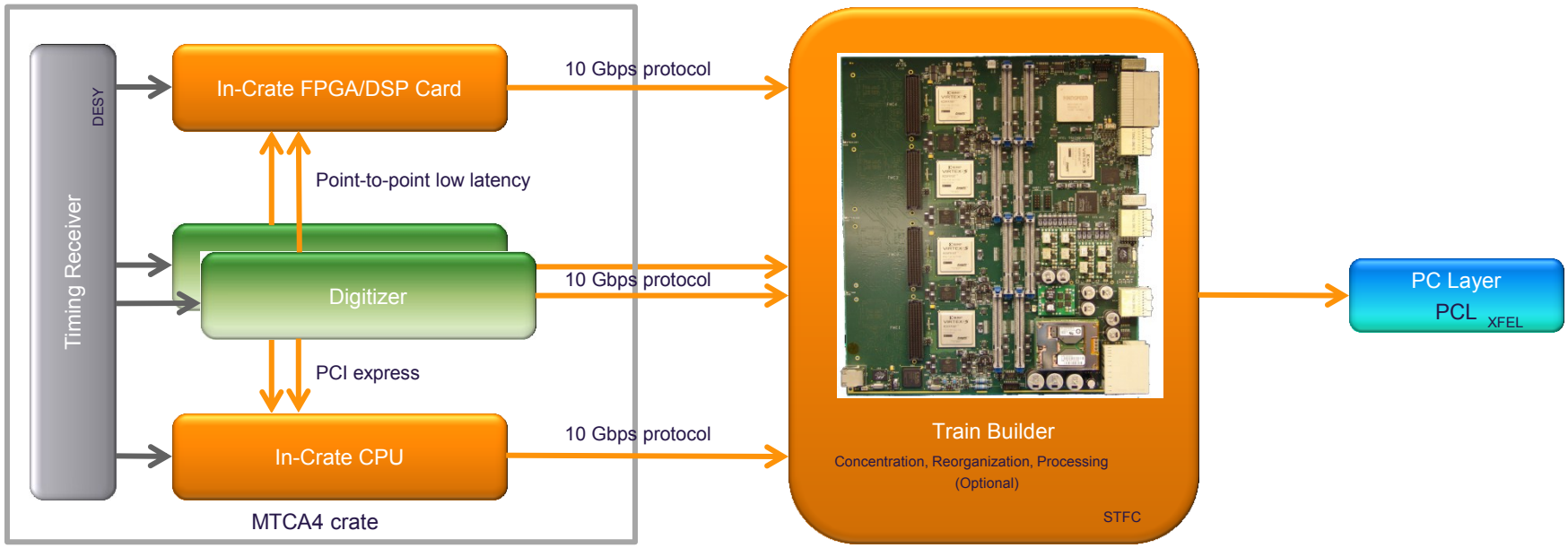
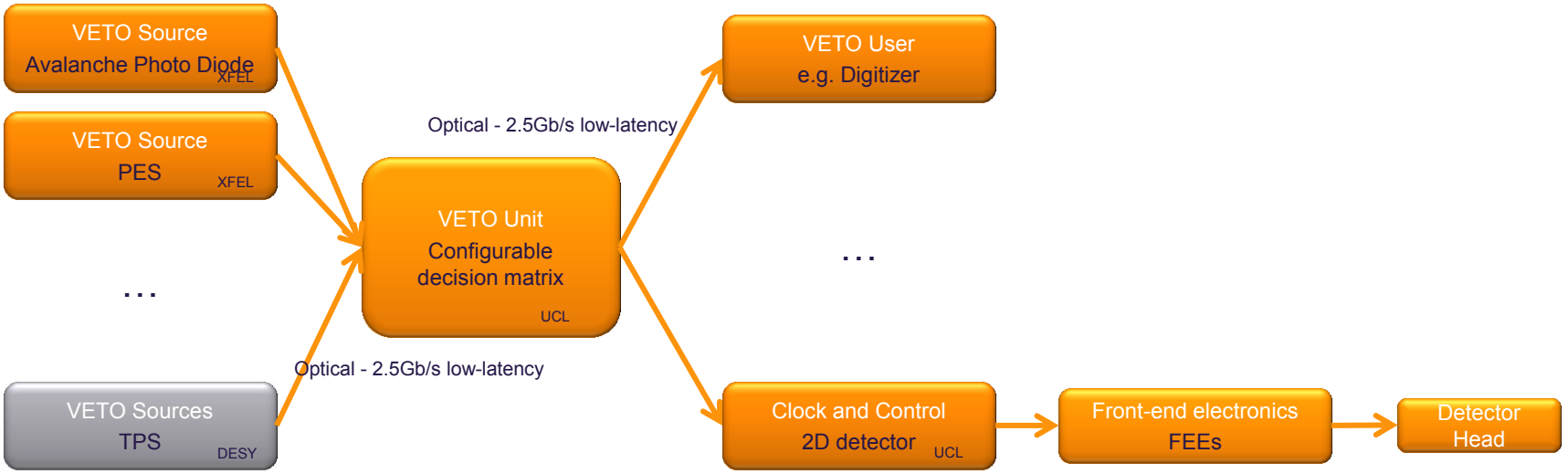
Data processing and transmission concept



- In-crate processing
  - In FPGAs of Digitizer
  - In local CPU
  - In a DSP/FPGA Bord
- Processing of multiple sources
  - Processing in FPGAs
  - Multiple Boards
  - Communication between all FPGAs
  - DDR and QDR Memory
- PC Layer
  - Software
  - CPUs
  - GPUs

VETO System for data reduction and memory optimization

- Optimize picture quality of 2D detectors
  - Limited frame capacity in ASICs (~300-700 frames)
  - Replace bad frames with new ones in ASIC before read out and transmission
- Data reduction
  - Discard useless data before transmission
- Implementation
  - FPGAs of diagnostics and detectors provide bunch information with low-latency
  - Configurable central VETO unit per experiment decides on bunch quality
  - FPGAs of detectors (maybe also diagnostics) receive the decision and react on it
  - Using a common protocol with beam based feedback system



Time for questions…