

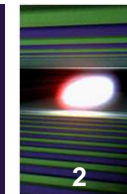


Integration of experiments and diagnostics

1st Meeting of the European XFEL Accelerator Consortium
17.4.2012

C.Youngman for WP76

List of PBS components to control



Optics (WP73)

- KB mirrors for focusing
- Refractive lens focusing
- Monochromator
- Collimator
- Slits
- Attenuators

Vacuum systems (WP73)

- Turbo pumps
- Ion pumps

Beam diagnostics (WP74)

- Intensity monitors
- Beam positioning monitor
- Photon-electron spectrometers
- K-monochromator and cameras
- Screens and camera

Tunnels contain components listed above

Laser systems (WP78)

- Pump laser and diagnostics

Sample environment (WP79)

- Particle injector
- Cryostat
- Precision stages

Experiment detectors (WP8x)

- e- and ion TOF
- Point detectors (diodes)
- Spectrometers

Experiment 2D detectors (WP75)

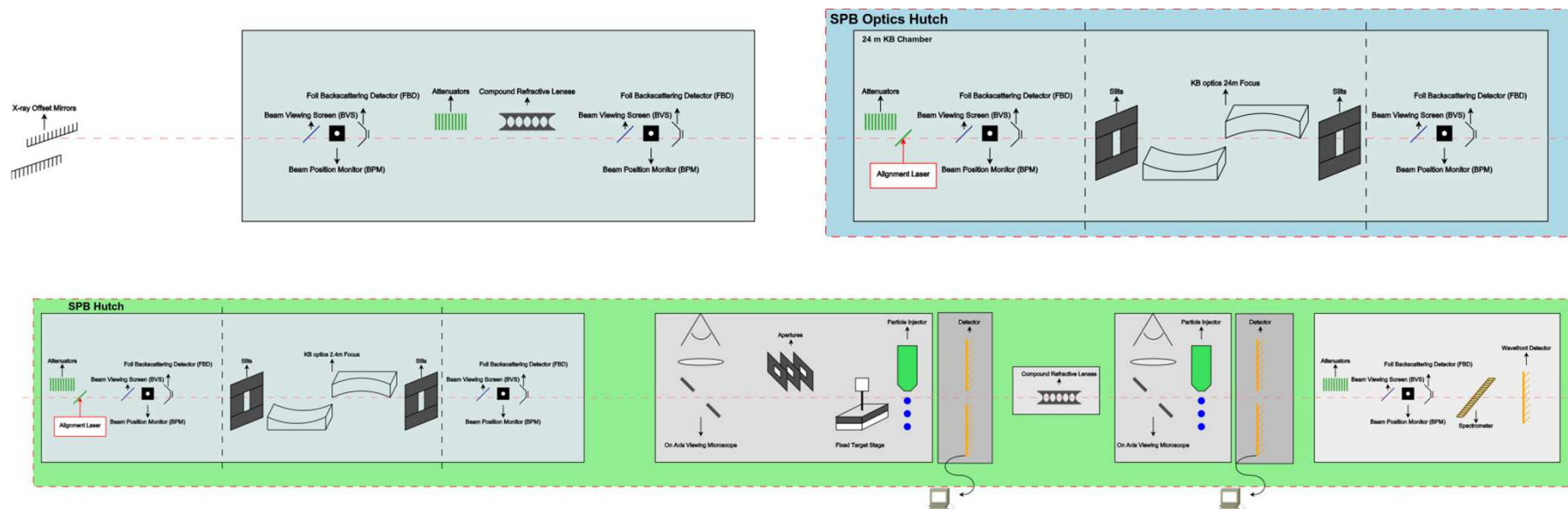
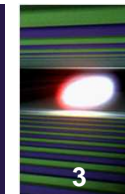
- AGIPD
- LPD
- DSSC
- pnCCD

DAQ
significant

Experiment hutches contain components above +
many of the tunnel instruments

To make a measurement it is necessary to control experiment, diagnostic and optics components

Draft layout of SPB experiment (~CXI at LCLS)



Components to control

- Diagnostics stations, cameras, screens
- Focusing CRL, KB... components
- Attenuators, apertures, slits
- Pumps, valves, gauges, motors
- Sample injection and laser systems
- eTOF, diodes, 2D cameras, spectrometer...

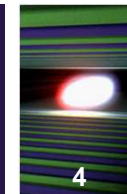
Component control channel count.

- | | |
|---------------------------|---------------------------|
| ■ Digital In/Out (412/52) | ■ Digitizers (1) |
| ■ Analog In/Out (168/9) | ■ Fast ADCs (28) |
| ■ Serial IO (39) | ■ Single shot cameras (9) |
| ■ Relays (48) | ■ Pixel cameras (2) |
| ■ Axis (241) | ■ ... |

The integration of large number of components is easier if a few solutions are reused often

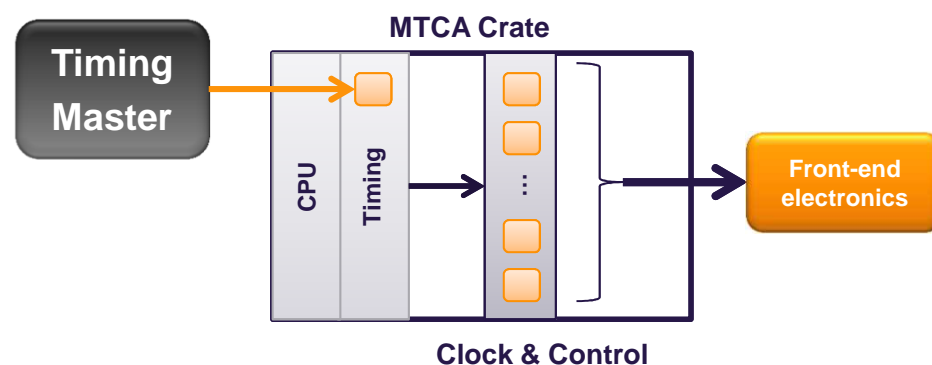
The EtherCAT distributed slow control system described by the previous speaker is a reusable solution.

Timing and Synchronization Systems for XFEL

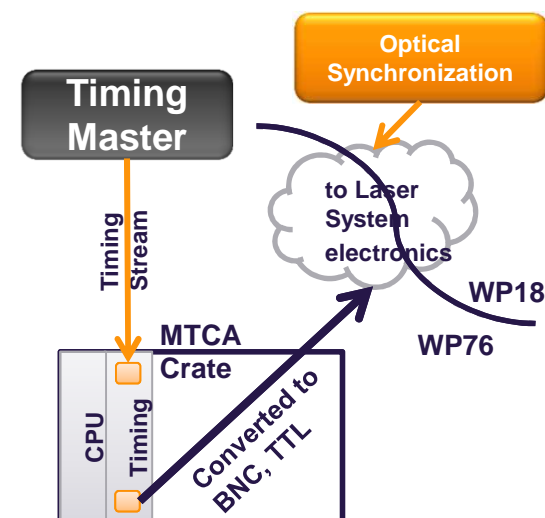


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	Timing System (WP28)	Optical Synchronization (WP18)
Provides	Clocks, Triggers and Data	Clocks
Stability	Less than 100ps	Less than 50fs
Applications	DAQ and Detector sequencing	Synchronize lasers to beam



- Timing master distributes reference clock with encoded data
- Drift is actively compensated
- Transmits events used for triggers (START) and bunch clocks
- Transmits bunch pattern and related information

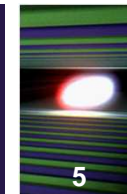


- Optical synchronization is required to be in phase with beam
- Timing is required to select the correct pulses

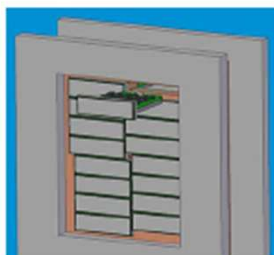
The e-machine Timing system (DAQ synch.) and optical synchronization (Laser synch.) interfaces are (re)used as is.

The e-machine MTCA.4 and ATCA crate and board standards are also (re)used.

XFEL detectors (source: WP75 – Oct 2011)

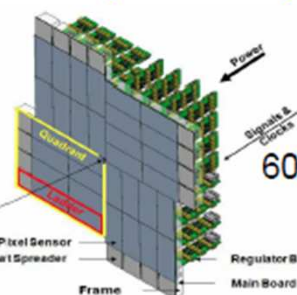


AGIPD Adaptive Gain Integrating Pixel Detector (AGIPD)



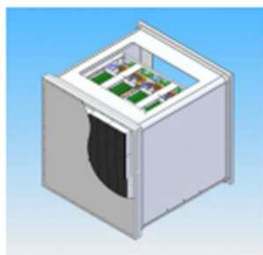
Energy range
3 - 13 keV
Dynamic range
 10^4 @12 keV
Single Photon Sens.
Storage Cells ≈ 300

DEPFET Sensor with Signal Compression (DSSC)



Energy range
0.5 - 6 keV (25 keV)
Dynamic range
6000 ph/pix/pulse@1 keV
Single Photon Sens.
Storage Cells ≈ 640

Large Pixel Detector (LPD)



Energy range
5 (1) - 20 keV (25 keV)
Dynamic range
 10^5 @12 keV
Single Photon Sens.
Storage Cells ≈ 512

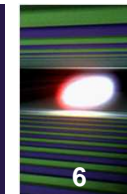
Other Detectors

- 0D/1D detectors for high repetition rate applications (e.g. veto, dispersive spectrometers)
- Small areas, low rep. rate, low energy 2D imaging detectors
- Particle detectors (eTOF, iTOF)

Control and DAQ features

- 2D: custom systems (ASICs, capacitive and digital pipelines), acquire limited number of pulses per train; modular design = 16 modules per Mpxl
- 1D: strip detectors
- 0D (diodes...) and Particle detectors: use Fast ADCs or Digitizers

Common backend 2D detector development



DAQ “clock and control” MTCA.4 sequencing board development

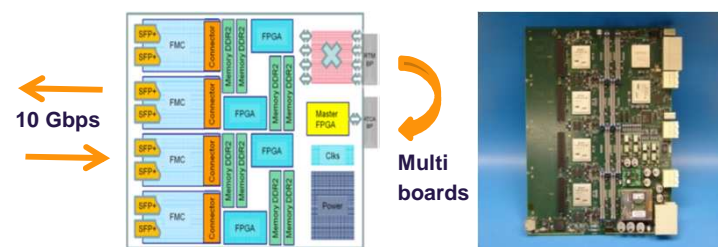
- 16 modules = 1 Mpxl
- One fast signal sequencing link / module (or quadrant)

DAQ “train builder” ATCA readout board development

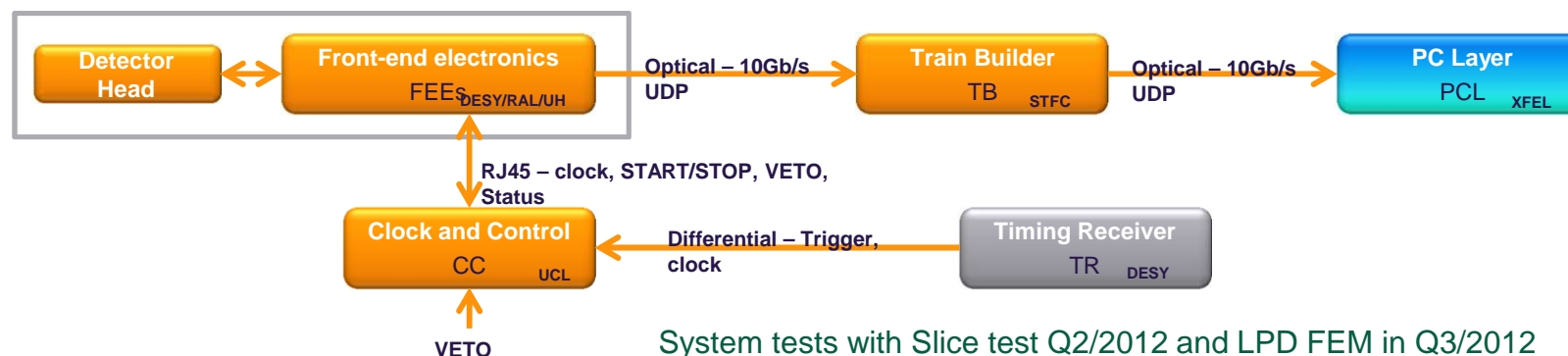
- collect image fragments from modules (10 Gbps links)
- reorganize into complete trains of pulse ordered images (cross-point)
- data processing in FPGA – remove empty, no ROI... frames
- send trains Round-Robin to PC layer (10 Gbps links)
- Multi board train builder installation should satisfy 4Mpxl camera demands in 2015



Prototype sequencer MTCA.4 RTM (UCL)



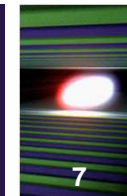
Prototype train builder ATCA board (STFC)



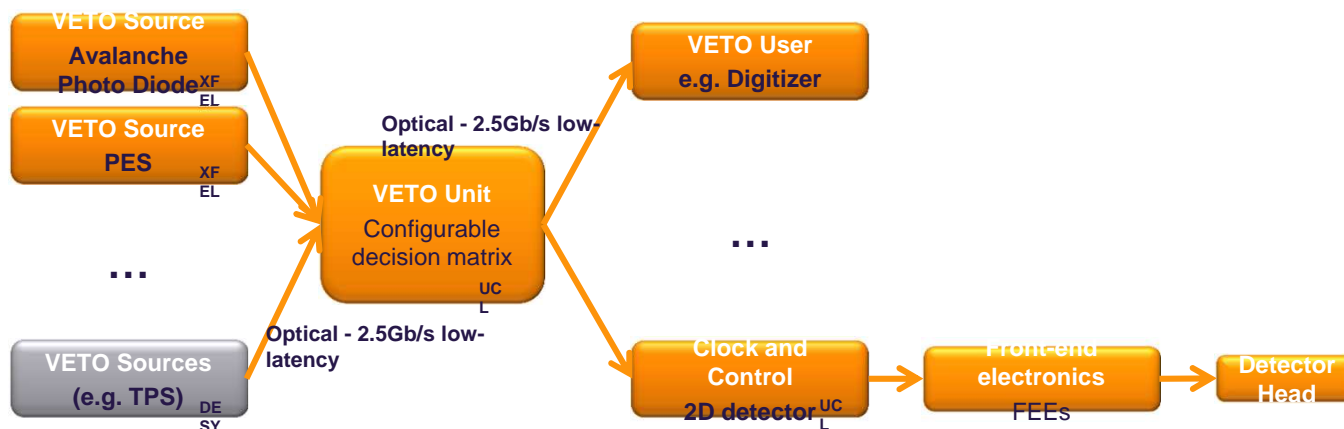
System tests with Slice test Q2/2012 and LPD FEM in Q3/2012

The train builder board can be reused to readout multiple digitizers, e.g. SQS's TOF and VMI systems, 1D detectors, etc.

Improving image quality – VETO system

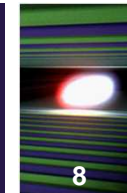


- **A VETO system is being implemented to**
 - Clear for reuse storage pipeline cells occupied by poor pulse data
 - Reduce amount of data to transfer or save
- **Centralized VETO unit per experiment**
 - Processes VETO pulse quality measurements from fast diagnostic and measurement devices
 - Trigger decision distributed to VETO users
- **All intelligent FEIs (detector and diagnostics) should participate in VETO – specification being consolidated**



The VETO is a trigger system – if the DataXpress collaboration is approved we will get feedback about veto, rejection and reduction data rates by end of 2012 based on analyzing data from LCLS.

Digitizer and Fast ADC integration into DAQ



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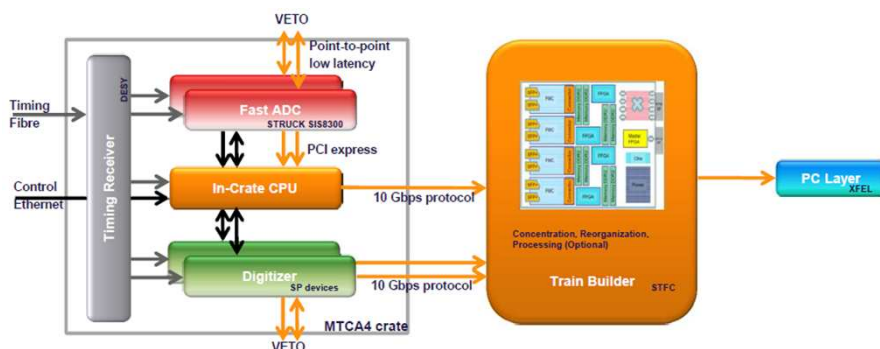
Standards chosen satisfy DAQ and control requirements

- MTCA.4 crate board: remote operation, RTM signal conditioning
- FPGA processing: data reduction/rejection and VETO generation/receiving (low latency SFP)
- 10Gbps data streaming

Device	Characteristics	Provider	Usage
Fast ADC	125 MHz, 16 bit	www.struck.de	4.5Mz shaped signals: APD, BSD...
Digitizer	1-7 GS/s, 14-8 bit	www.spdevices.com	eTOF, iTOF, VMI...

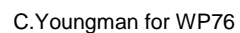
DAQ and control integration

- control = over ethernet to crate CPU and on to board via PCIe
- DAQ = to TB (or PCLayer) over board 10Gbps link or via PCIe to CPU 10 Gbps link (in 12 months)
- VETO = via board low latency link

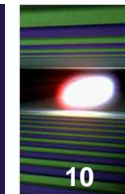


APD Fast ADC test system

- eTof
- spectrometer



The big picture – DAQ and control part 2



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Experiment diagnostics

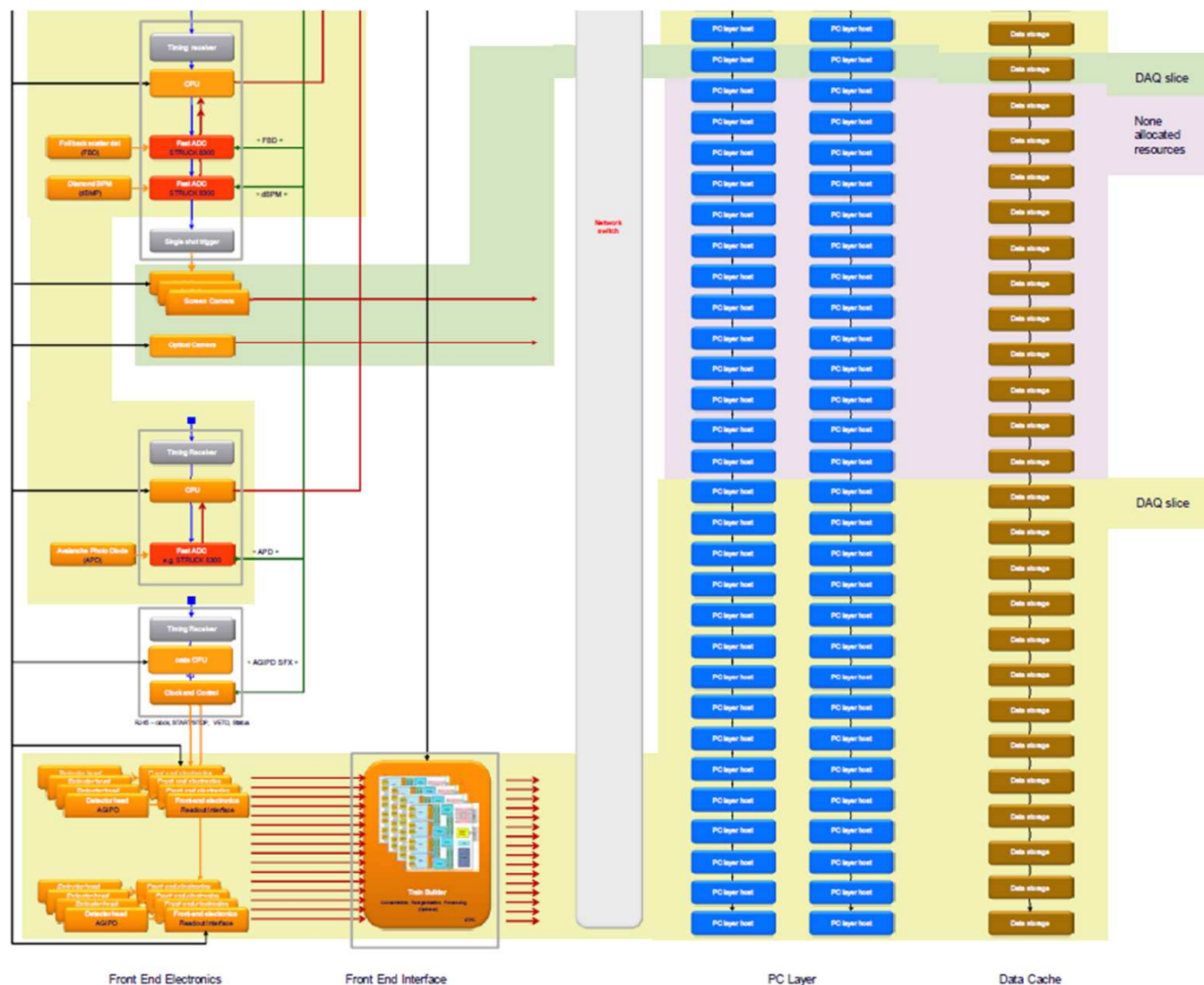
- BPM position monitors
- FBD foil back-scatter det.
- screen cameras
- optical microscope

Experiment VETO

- fluorescence monitor
- ...

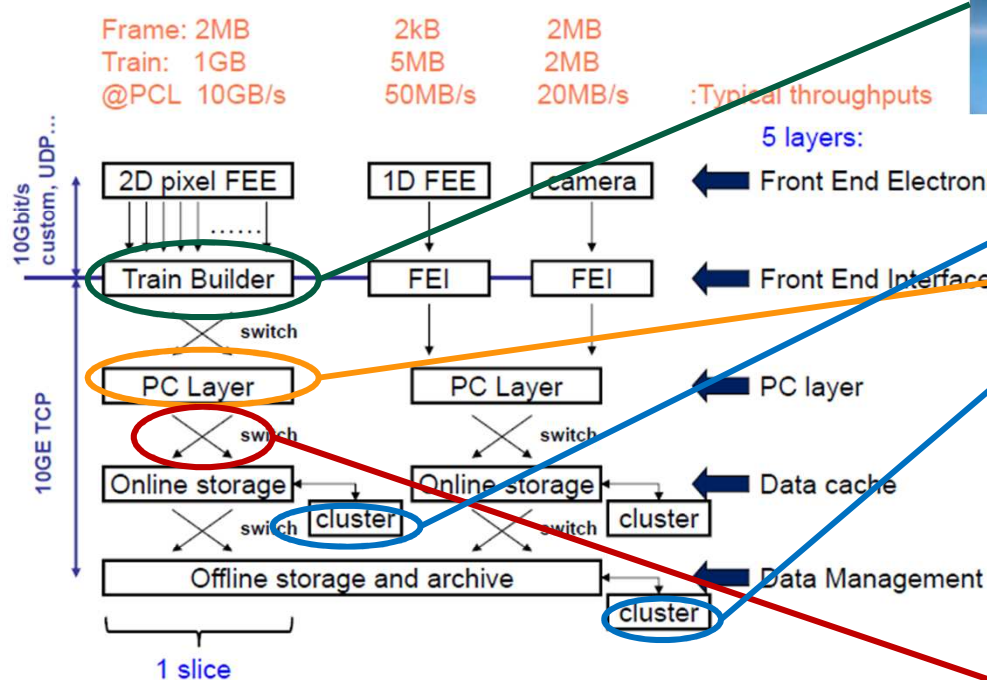
SFX large area camera

- AGIPD



DAQ layer:

TB prototype Q3/2012



Test of a vertical ½ to 1 Mpxl slice of architecture started



**Compute
+ GPUs
nodes**

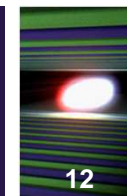
PC
nodes

DB+MDS
nodes



10 Gbps switch

Traffic management



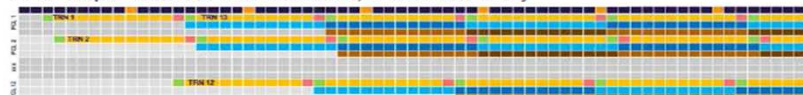
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Data traffic management concepts

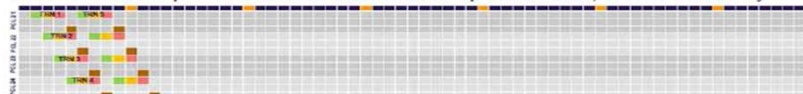
- Data traffic is DAQ slice specific and clocked by train delivery
- A DAQ slice could be limited to a single detector or many
- Transfers in and out are always full trains of frame ordered data
- A single “leading” bin is used to transfer “metadata” into the slice
- Multiple bins are used to insert large data volumes into the slice
- A single “trailing” bin catches any late data associated with the slice
- Leading and trailing bin traffic should be TCP protocol, other bins can be UDP, iWARP...

Simplified traffic schedule for SPB

SPB 1Mpxl camera: 1024MB/train, 4 time bin delay



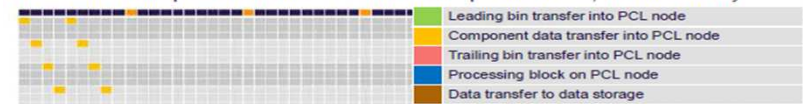
eToF 6MB/train plus 4 channel 4x5MB/train spectrometer; 2 time bin delay



SFX 1Mpxl camera: 1024MB/train, 3 time bin delay

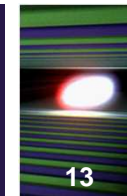


eToF 6MB/train plus 4 channel 4x5MB/train spectrometer; no time delay



- Leading bin transfer into PCL node
- Component data transfer into PCL node
- Trailing bin transfer into PCL node
- Processing block on PCL node
- Data transfer to data storage

Conclusions



- Considerable steps have been made towards integrating control and DAQ system for experiments, diagnostics and slow control
- Standard interfaces are defined and used to integrate to the machine and between control and DAQ sub-systems
- Prototype developments are reaching the test phase
- Integration within the homogeneous s/w framework is progressing

Thank you for listening !