LLRF ADC Firmware structure and high level software concepts

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1st Meeting of the European XFEL Accelerator Consortium
17.04.2012

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DESY

Outline

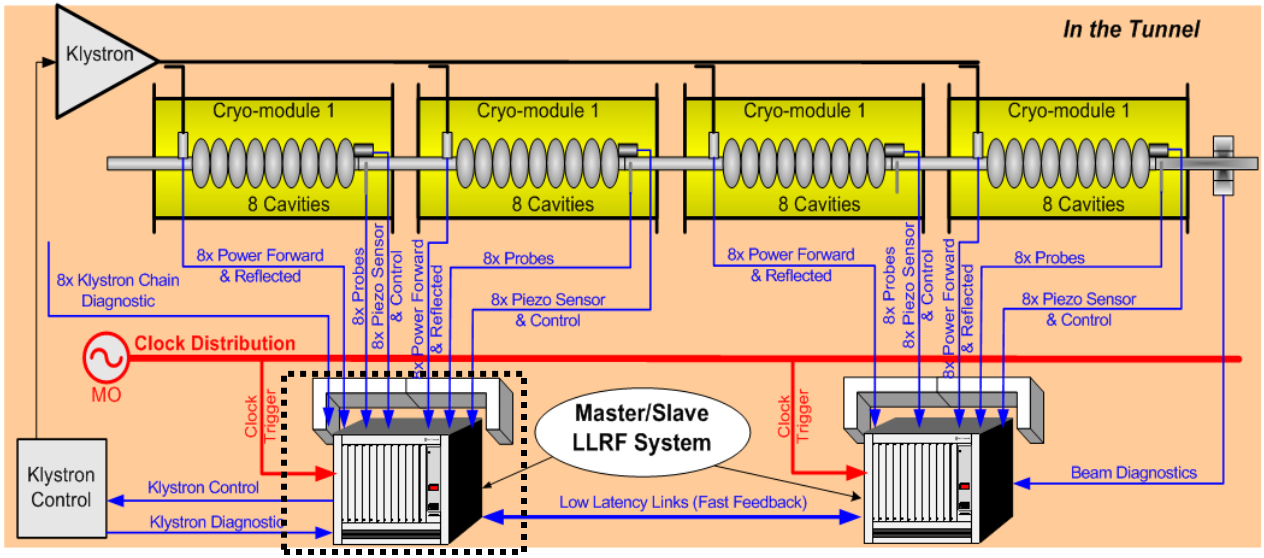
- Motivation and background
- Design example ADC board
  - Block diagram
  - Measurements
- Summary and outlook

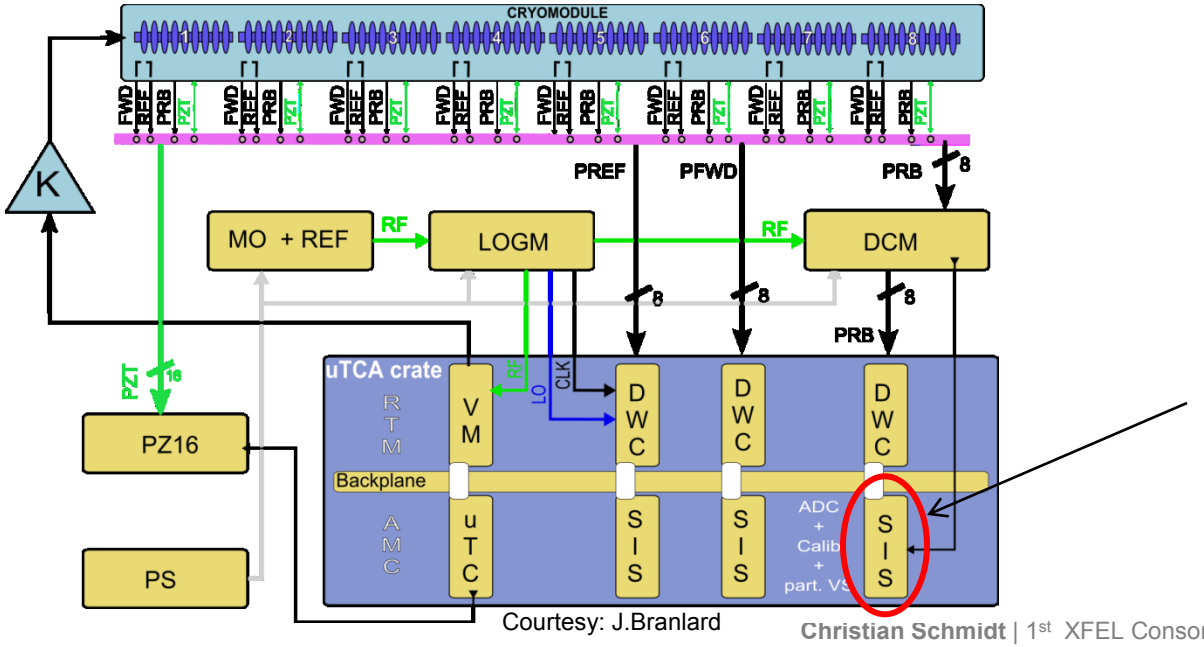
Motivation and general comments

- Reliable and easy maintainable, performance must be reached
- Generic to use at different systems with different properties
  - Individual Blocks can be modular plugged together depending on application needs
  - If possible use switches or dividers to adjust eg. for different frequencies
- Structuring must be extendable in future without major upgrade
  - Having margin in FPGA space, server CPU usage, communication bandwidth
- Transition stage in a new project
  - Iterations needed / adaptation to new requirements
- Functionality tests, benchmarks, setup procedures
- Design concept essential
  - Interface definition and communication bandwidth estimation
  - Estimation of FPGA space, server layout and subsystem integration

LLRF signal topology for XFEL main linac

Subversions for:
- Injector
- Third harmonic
- NC structures

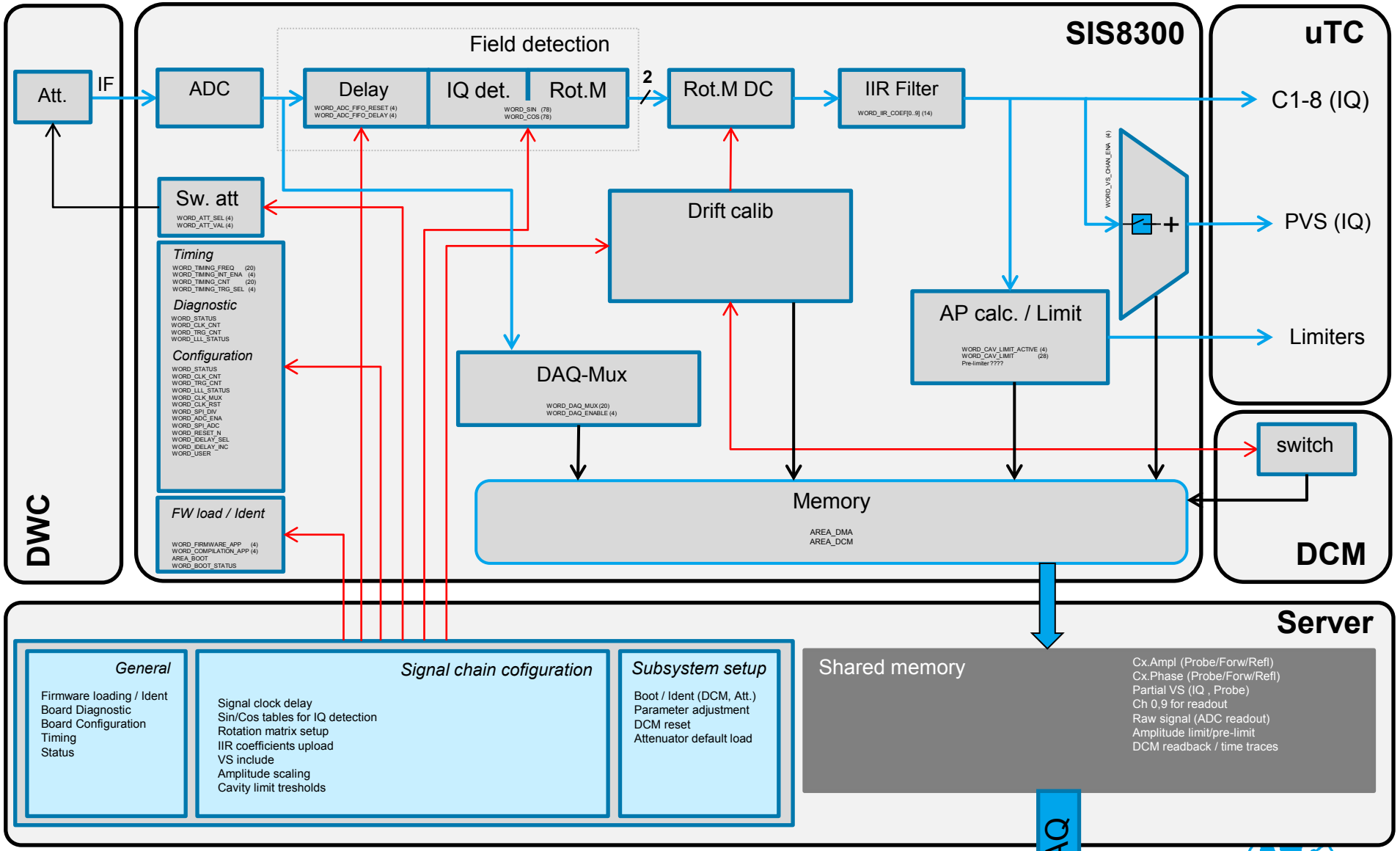




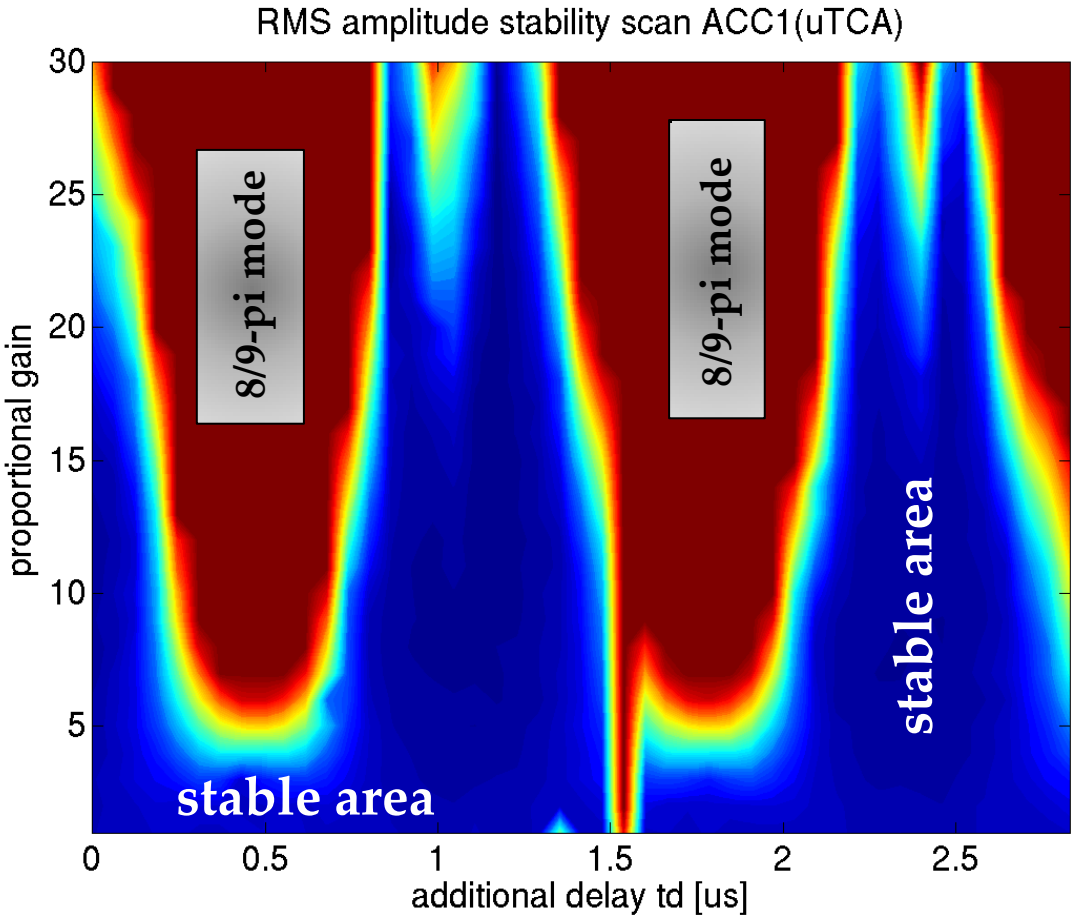
Courtesy: J.Branlard

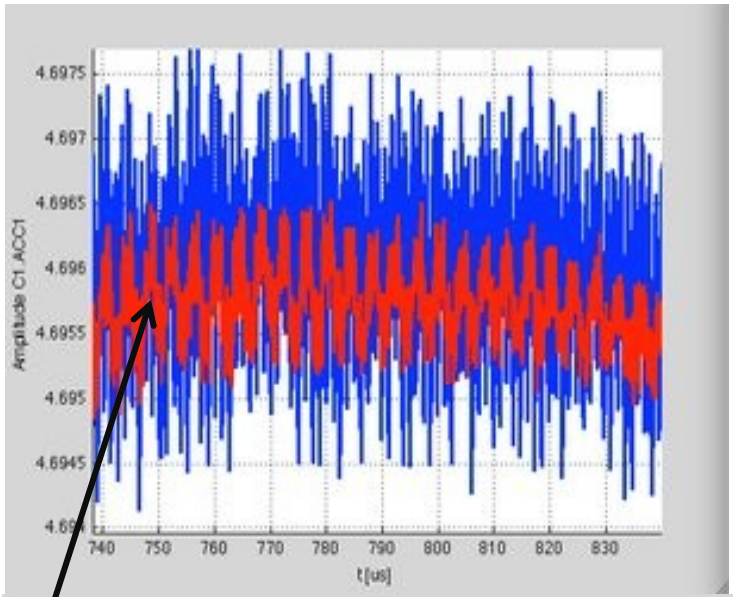
ADC board for readout of:
- Probe
- Forward
- Reflected
- ….
- Control DCM / DWC

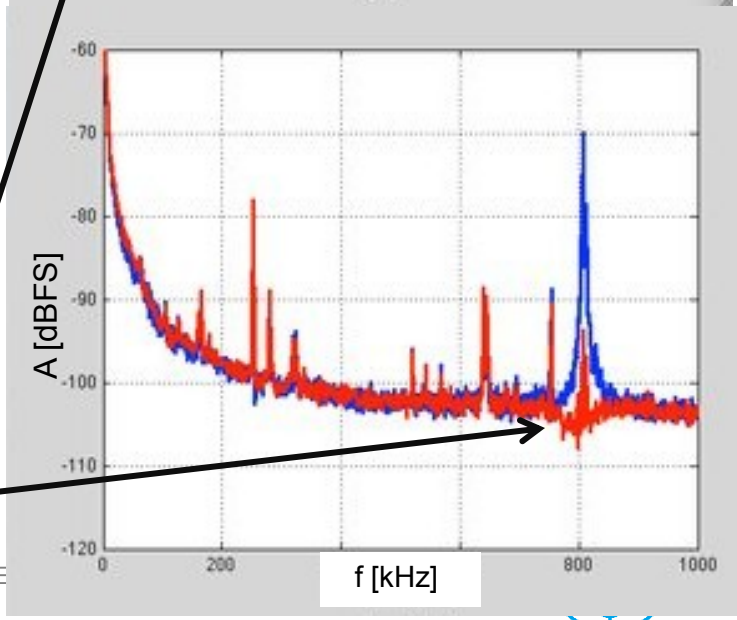
ADC board functional block diagram



Filtering unwanted signal contributions



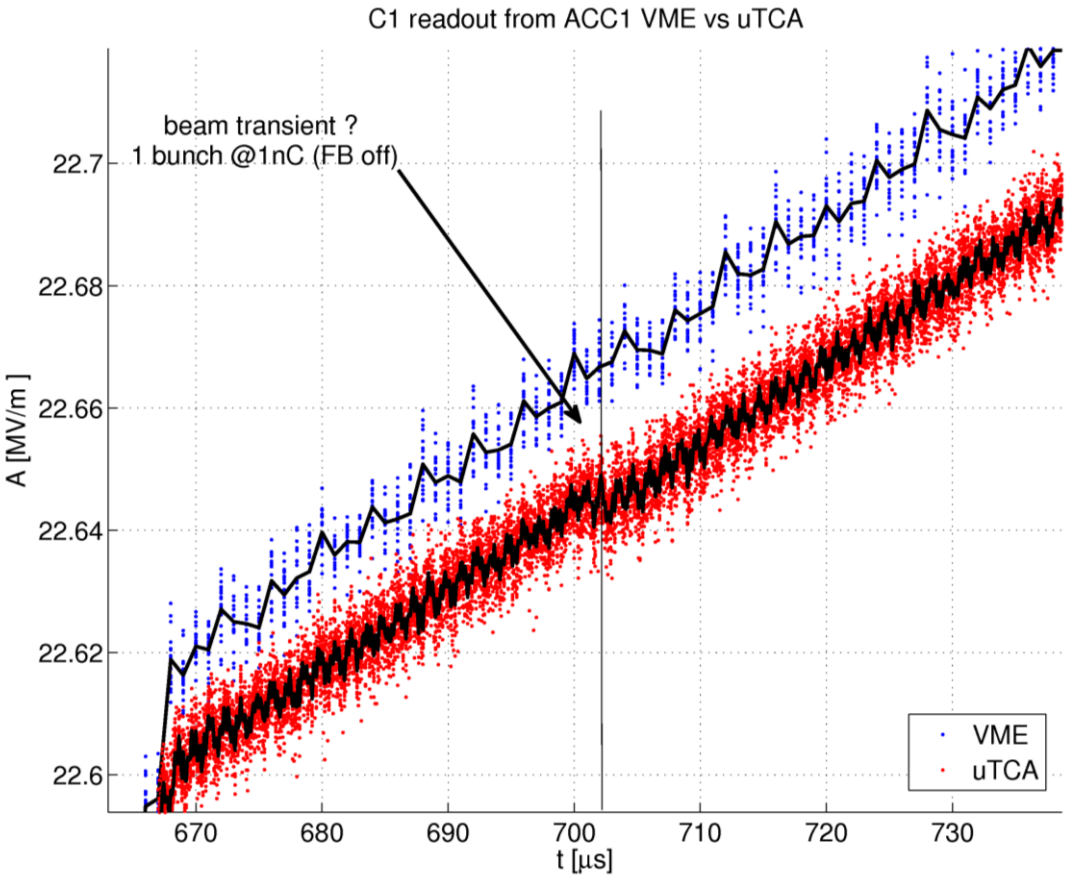


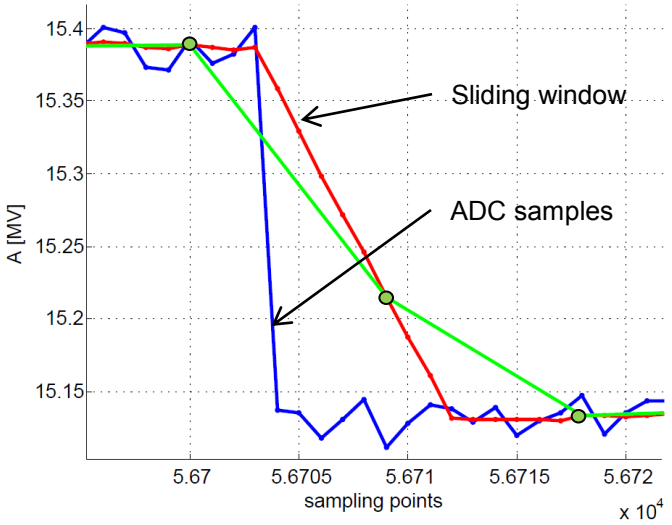


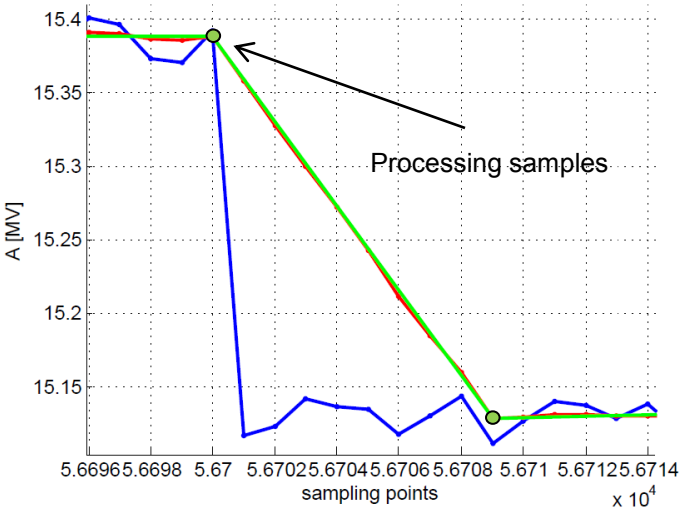
- Low-pass / band-stop filters are implemented
- Reduction of unwanted modes
- General signal filtering (LP)

Filtered signal

Measurements of beam induced transients

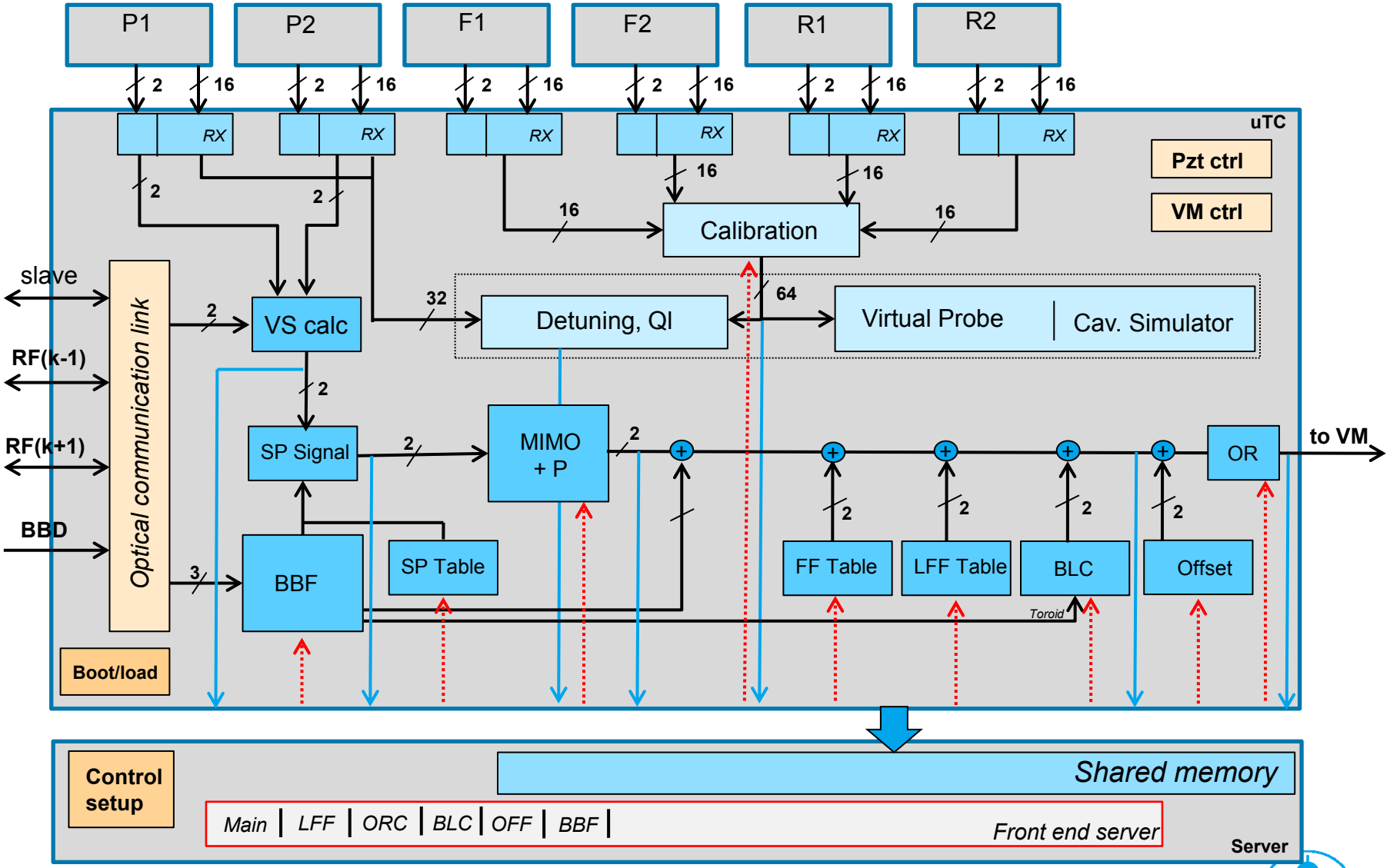






- Use delay for alignment of individual cavity transient readouts for e.g. VS calibration, beam loading compensation

Controller (Master) functional block diagram

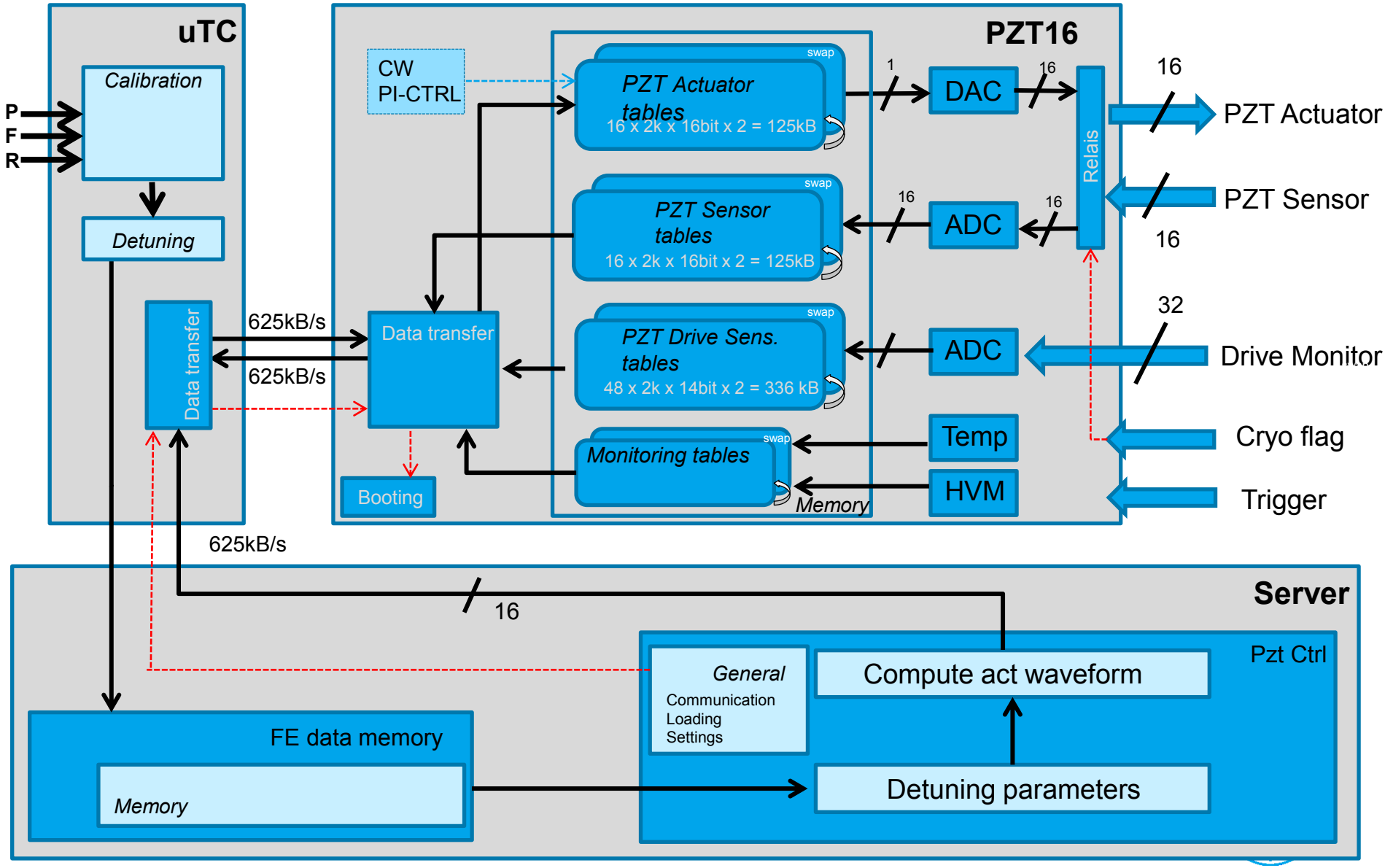


Summary

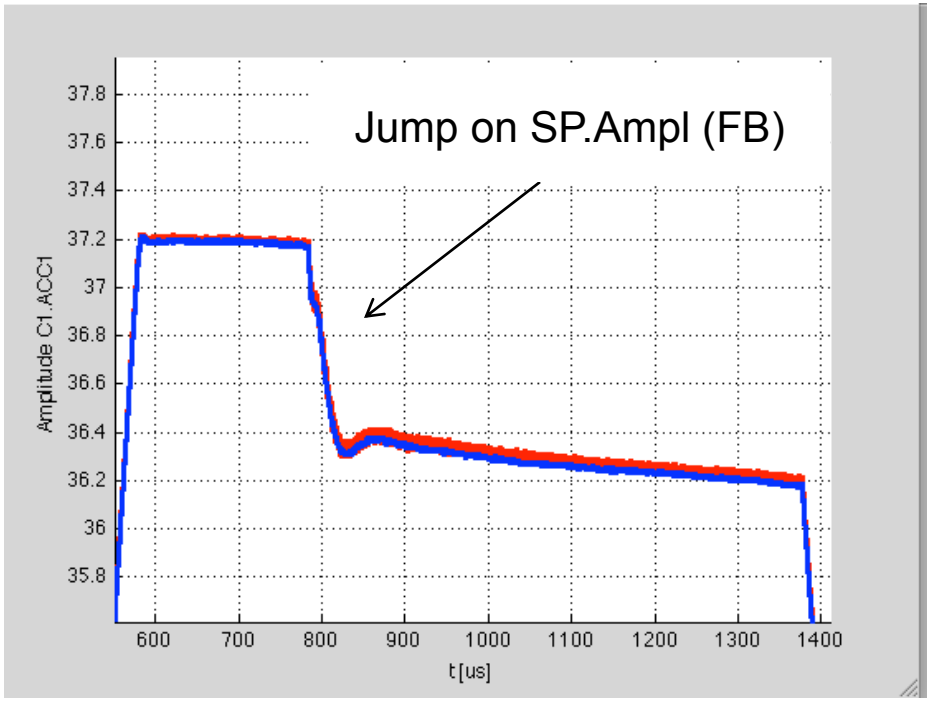
- Generic software structure for multi-purpose application
  - Maintainability
  - Programming effort
- ADC firmware layout for LLRF
  - Modularity and preprocessing
  - Communication / control of further sub devices
- Currently transition of controller firmware to uTC
- Setup / Test / commissioning of a full LLRF station

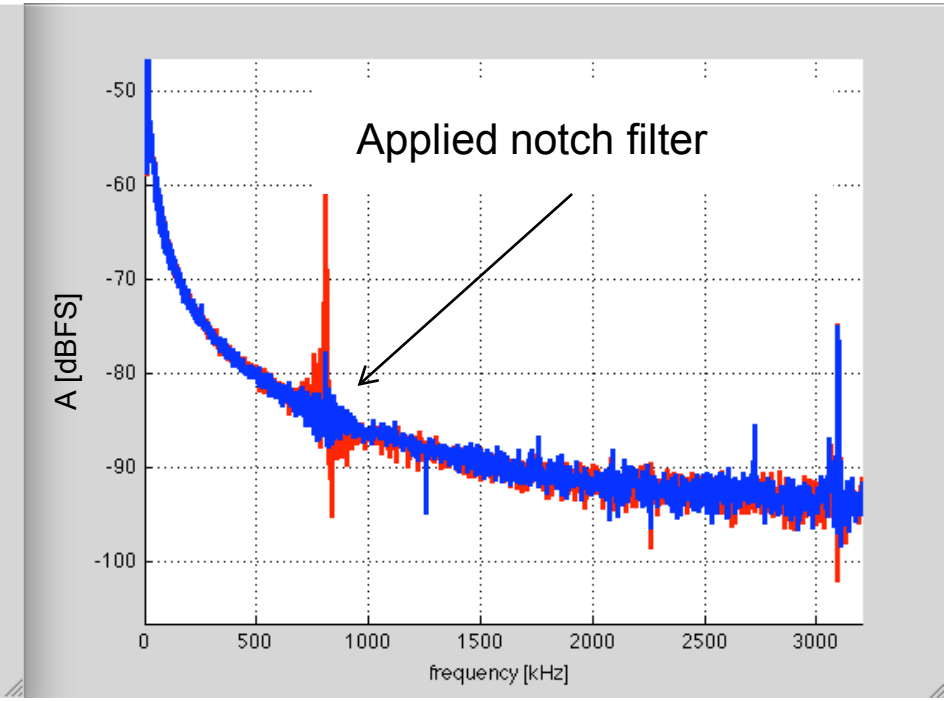
Thanks for you attention

Pzt function block diagram



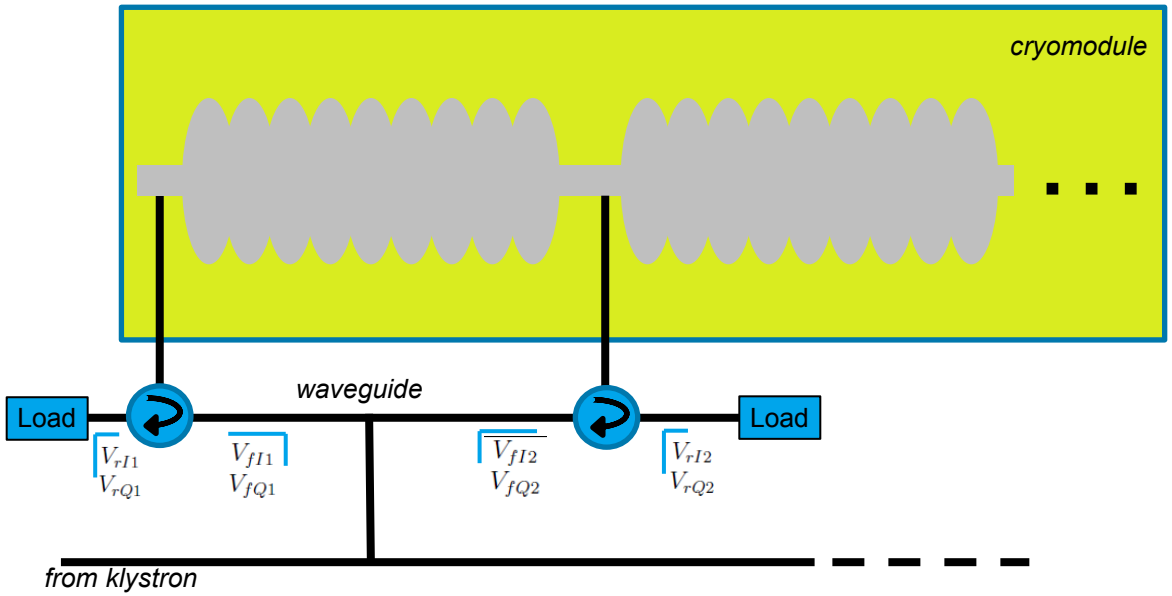
Filtered cavity transient response





- Typial step down in amplitude done for FLASH2 operation
- Broadband excitation leads to oscillation in particular of of the 8/9-pi mode
- Impacts from beam loading / pre-limiter setpoint reduction

Calibrated waveguide signals (online)



- Coupling of cavity pairs on a waveguide branch
- Directivity of the couplers
- Required for virtual probe and detuning computation
- Should be implemented on uTC signal entry level

- 8x8 Matrix for 2 cavity channels
- 16 cavities for 1 uTC board, 9MHz
- Estimation: 256 DSP slices
  - One matrix for 4 channels
  - Optimization might further reduce size
  - 40% of FPGA size !!

$$\begin{pmatrix} V_{fI1c} \\ V_{fQ1c} \\ V_{rI1c} \\ V_{rQ1c} \\ \hline V_{fI2c} \\ V_{fQ2c} \\ V_{rI2c} \\ V_{rQ2c} \end{pmatrix} = \left(\begin{array}{cccccccc} 1 & 0 & c_{13} & c_{14} & c_{15} & c_{16} & c_{17} & c_{18} \\ 0 & 1 & c_{23} & c_{24} & c_{25} & c_{26} & c_{27} & c_{28} \\ c_{31} & c_{32} & 1 & 0 & c_{35} & c_{36} & c_{37} & c_{38} \\ c_{41} & c_{42} & 0 & 1 & c_{35} & c_{46} & c_{47} & c_{48} \\ \hline c_{51} & c_{52} & c_{53} & c_{54} & 1 & 0 & c_{57} & c_{58} \\ c_{61} & c_{62} & c_{63} & c_{64} & 0 & 1 & c_{67} & c_{68} \\ c_{71} & c_{72} & c_{73} & c_{74} & c_{75} & c_{76} & 1 & 0 \\ c_{81} & c_{82} & c_{83} & c_{84} & c_{85} & c_{86} & 0 & 1 \end{array}\right) \begin{pmatrix} V_{fI1} \\ V_{fQ1} \\ V_{rI1} \\ V_{rQ1} \\ \hline V_{fI2} \\ V_{fQ2} \\ V_{rI2} \\ V_{rQ2} \end{pmatrix}$$