European XFEL Timing System

1st Meeting of the European XFEL Accelerator Consortium

by
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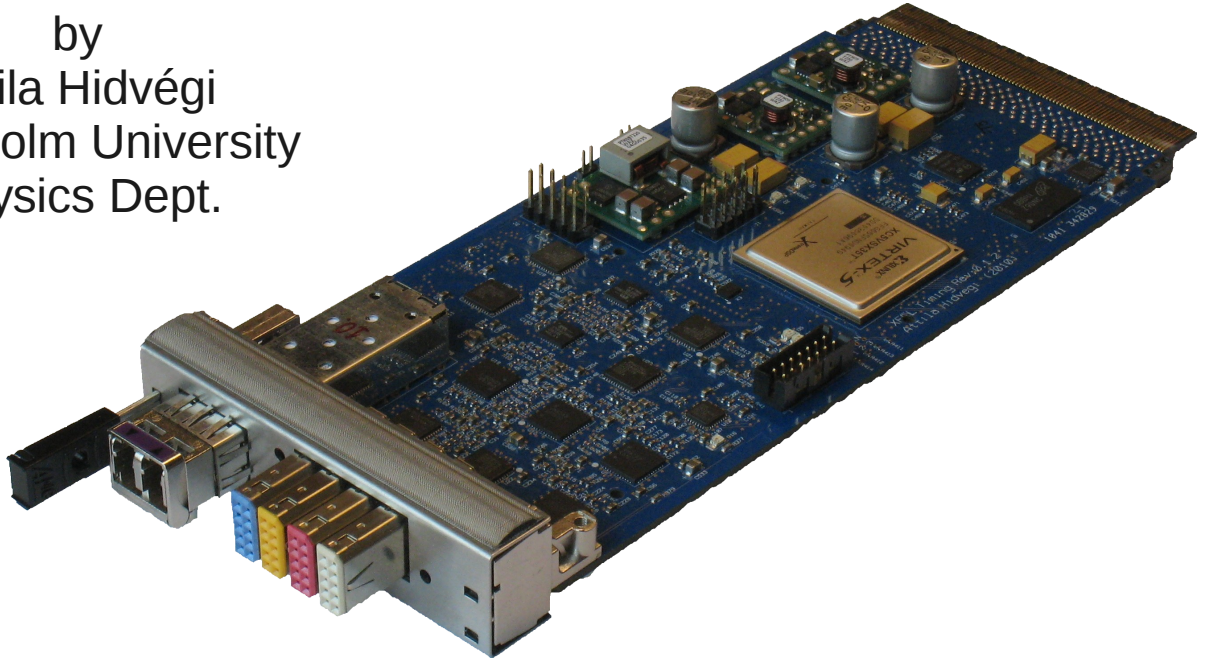


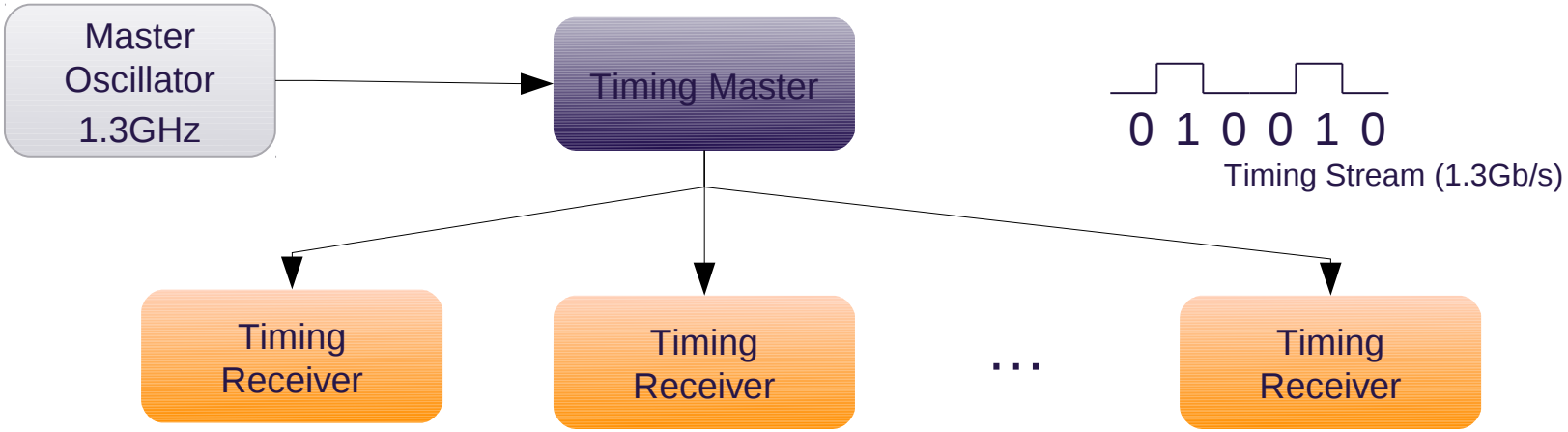
Overview

- Purpose and requirements overview
- Overview of the timing system
- Basic principle of the drift-compensation
- Current AMC timing-system
  - The hardware
  - Results
- FPGA Firmware development
- Next AMC timing-system
- Conclusions and Outlook

Purpose and requirements

- Distribute clocks and trigger information to the whole accelerator system and experiments.
- Deliver the 1.3 GHz main RF-frequency and other derived frequencies.
- Synchronize the clock-phases and keep them drift free, with a total jitter: <5 ps (RMS).
- Deliver clocks and triggers through the backplane and through the front panel.
- Cost efficiency

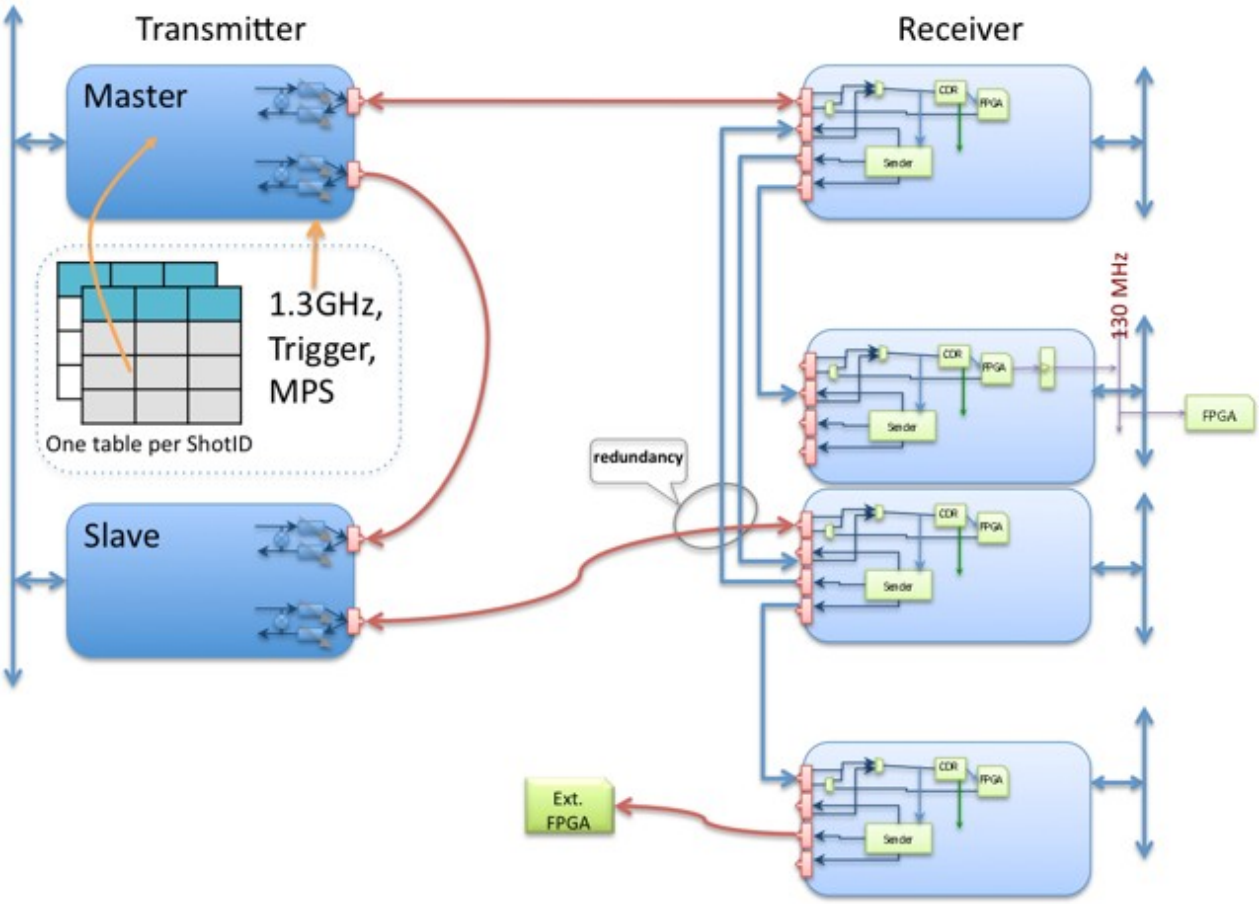
Overview of the timing system



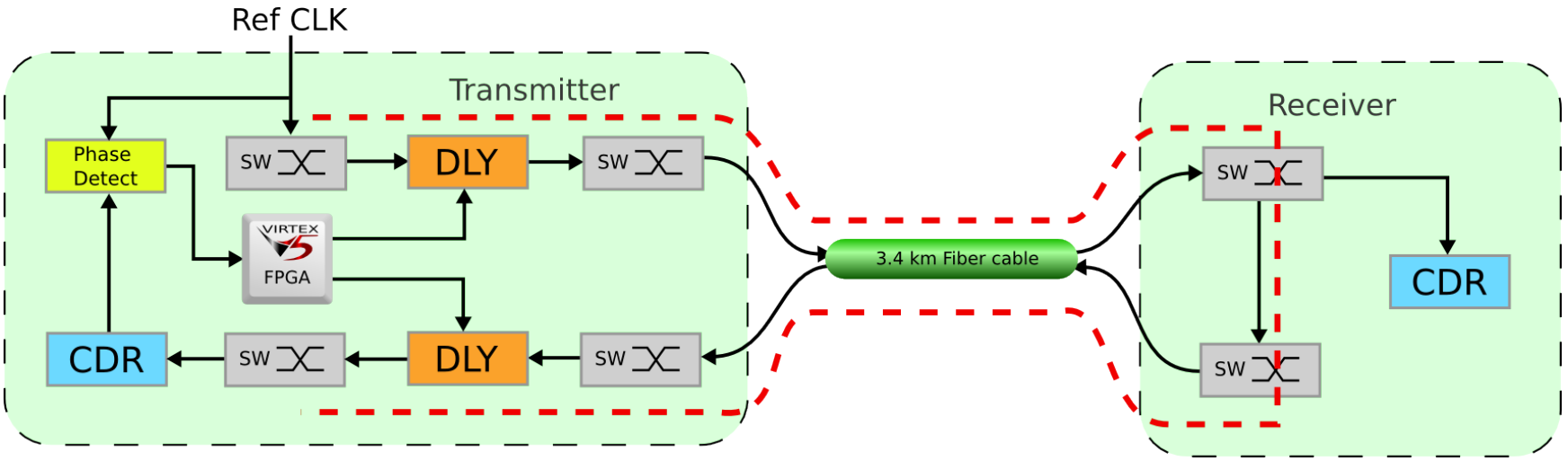
- Timing master distributes reference clock with encoded data
- Drift is actively compensated
- Transmits events used for triggers and bunch clocks
- Transmits bunch patterns and related information
- Allows recovery of 1.3 GHz reference clock
- Provides configurable divided clocks
- Sub-distribution is possible

Overview of the timing system

- Redundant fiber cable for long distance communication
- Local re-distribution of timing information
- Clocks and triggers delivered over the backplane



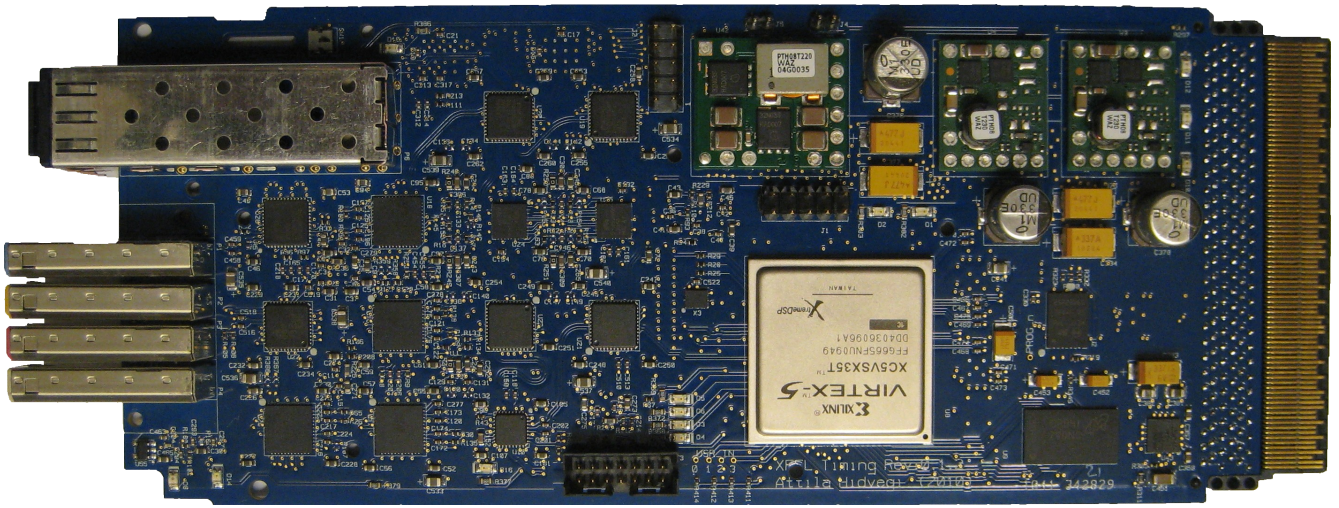
Basic principle of the drift-compensation



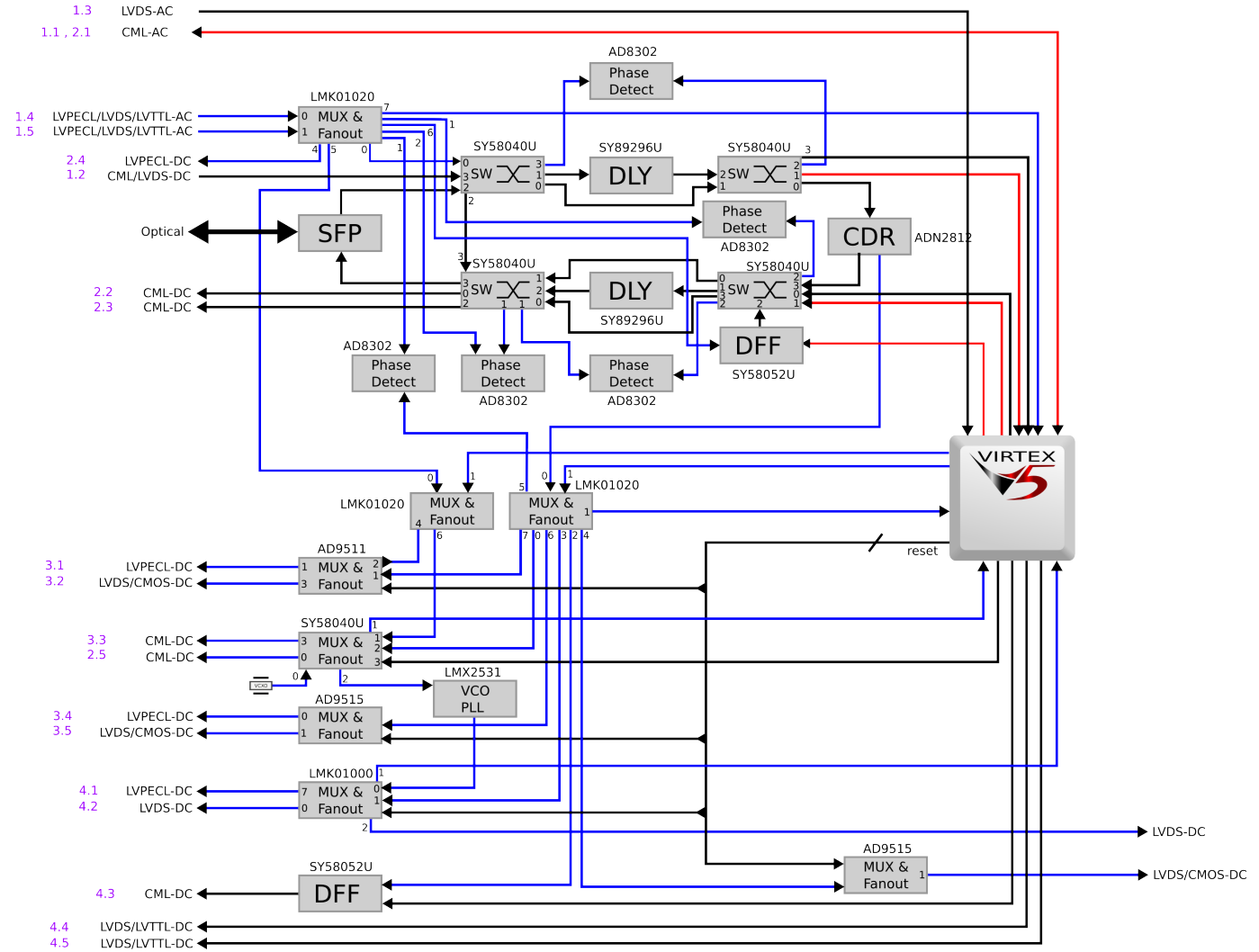
- Total delay is 2x (fiber delay + PCB track)
- Tx and Rx path is kept equal and constant
- Clock phases and temperatures are measured at key locations
- Drifts are detected by phase-detectors.
- Total loop is adjusted by delay components.
- Drifts are assumed to be relatively slow
- Loop-control implemented in an FPGA

Prototype AMC timing board

- Both transmitter and receiver functionality
- Delivers clocks and triggers through front panel and backplane.
- 8 M-LVDS signals to the backplane
- Main frequency is 1.3 GHz
- Derived frequencies are divided from the main frequency, and synchronized in phase
- Clock outputs are adjustable in steps of 100 ps
- Single SFP for optical communication
- ~25 W power consumption

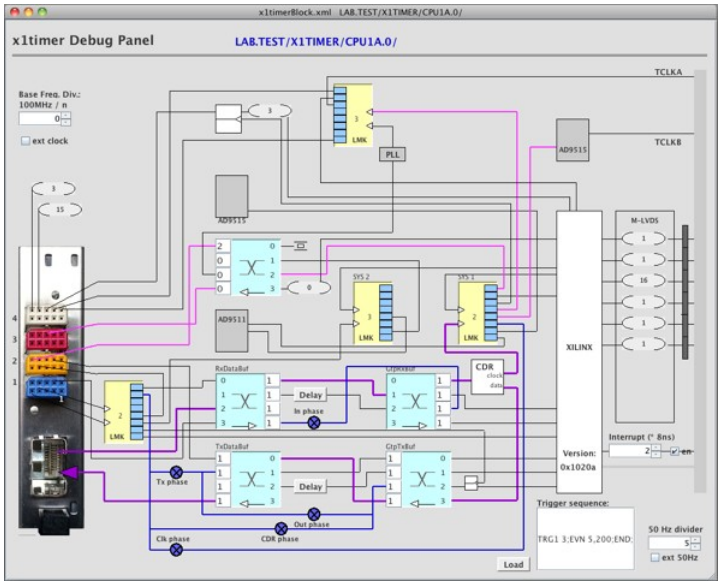


Prototype AMC timing board



AMC prototype results

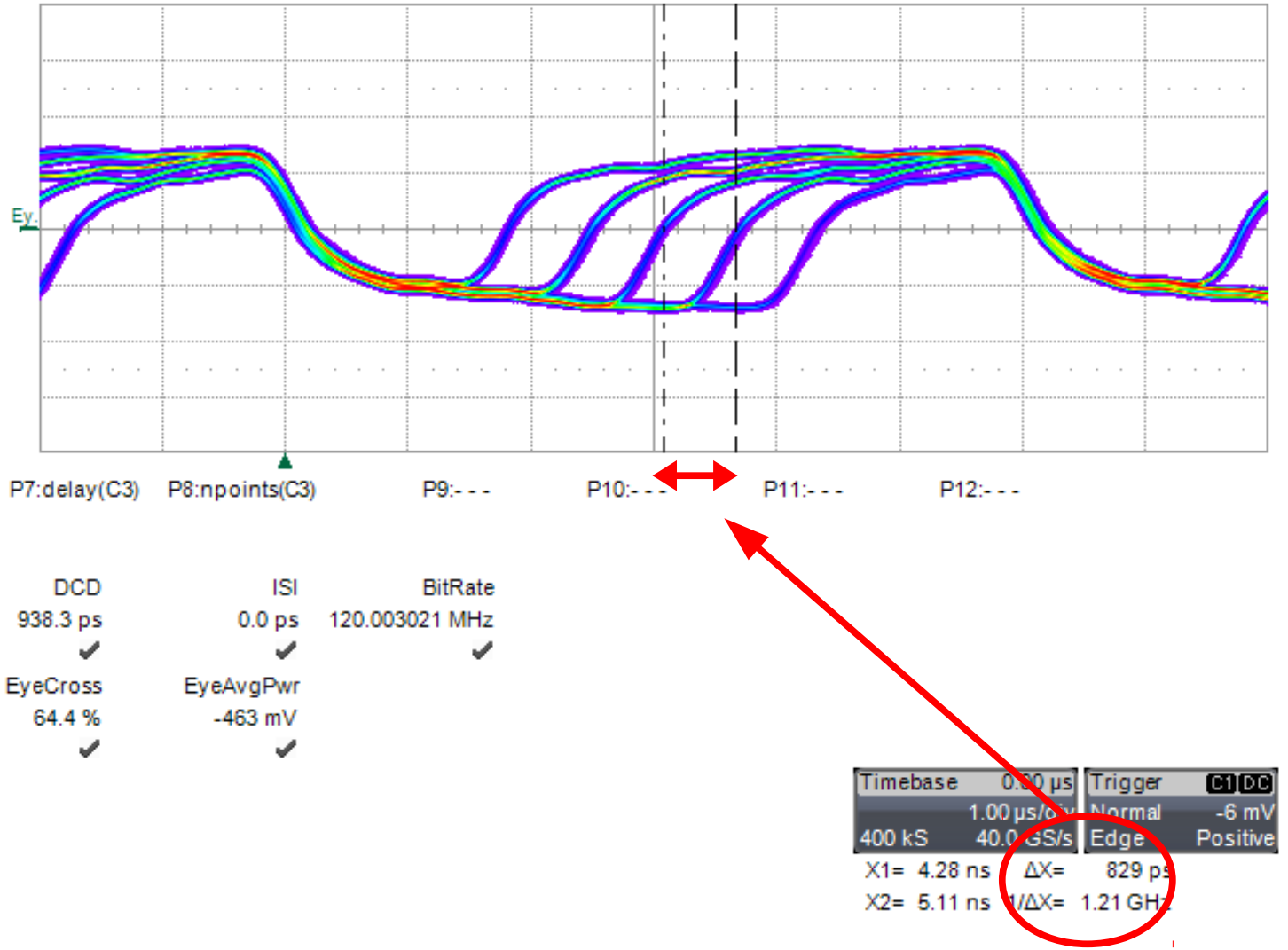
- <1.5 ps (RMS) random jitter on some of its outputs
- <120 fs (RMS) loop-time stability, <600 fs (p-p)
- Trigger delivered with 1.3 GHz phase resolution
- Test and support software has been developed for the board



FPGA firmware development

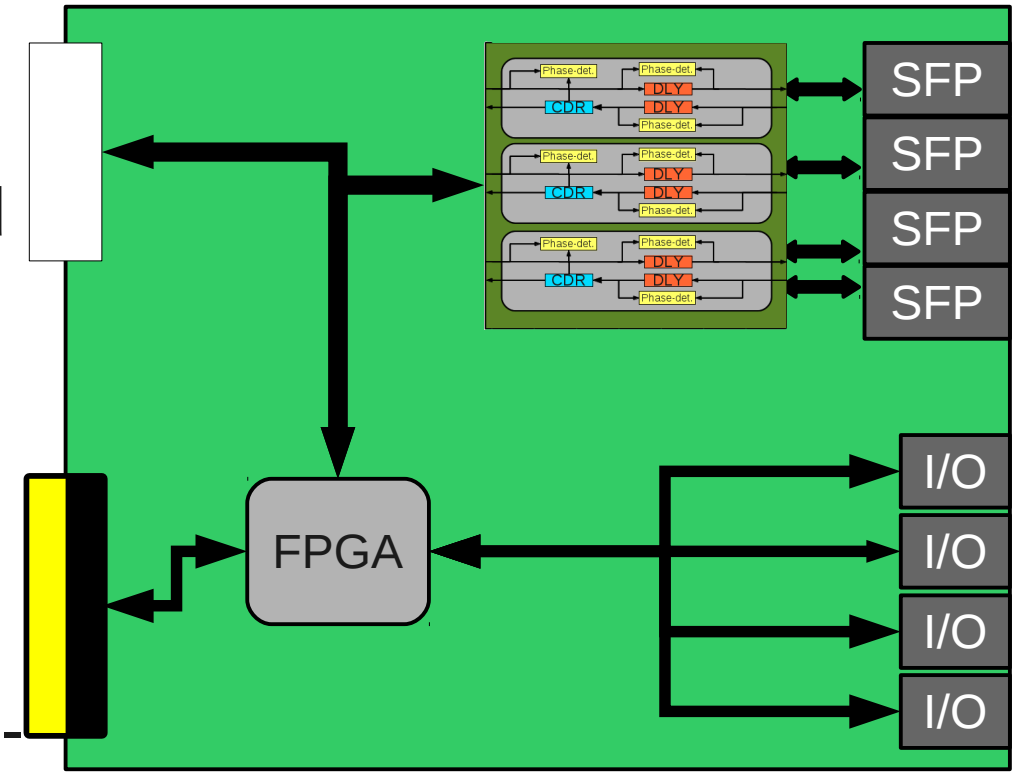
- SoC with MicroBlaze running the loop-contro (only prototype AMC)
  - Emulates fast drifts for debug purpose
- Fixed latency GTP transceiver
  - Important for total loop measurement and proper trigger generation
- Custom SerDes for trigger generation
- Timing protocol mostly implemented

Custom SerDes for 1.3 GHz phase resolution (Virtex-5)



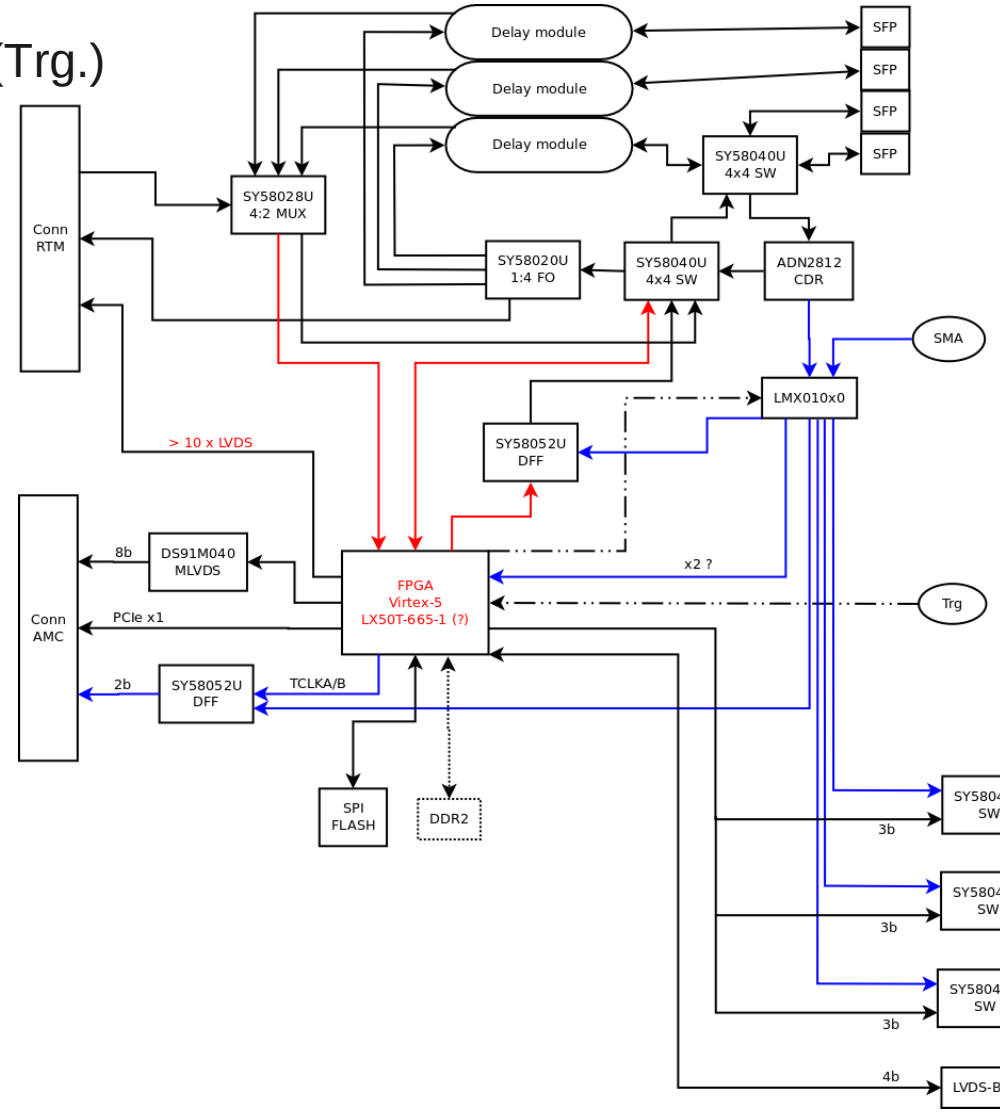
Final timing board design

- Double size AMC
- Both transmitter and receiver functionality
- Delay control implemented on daughter-board, and used by transmitters
- Support for RTM for more I/O customization
- Provide triggers with 1.3 GHz or 1.0 GHz phase-resolution.



Final timing board I/Os

LVDS (2.5V DC) (Trg.)
CML (*AC*) (Data)
I2C, PDI
MP_PWR



4 x SFP+

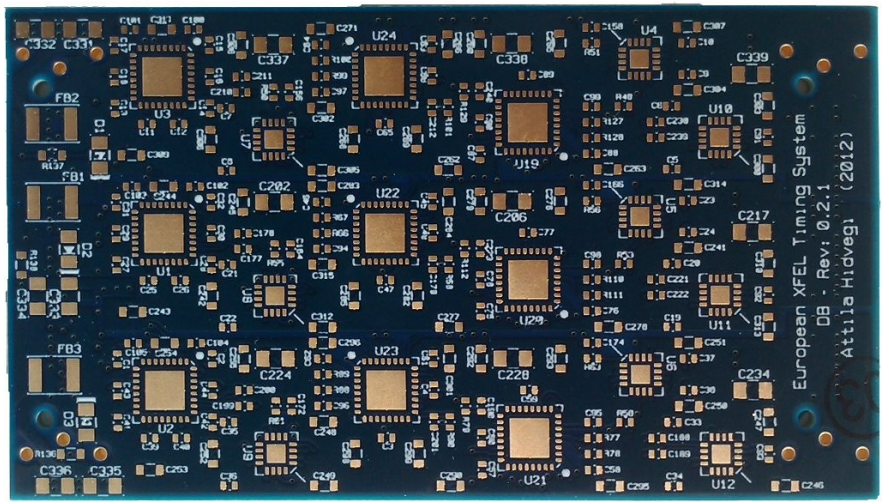
Ref CLK (AC)
Single-ended

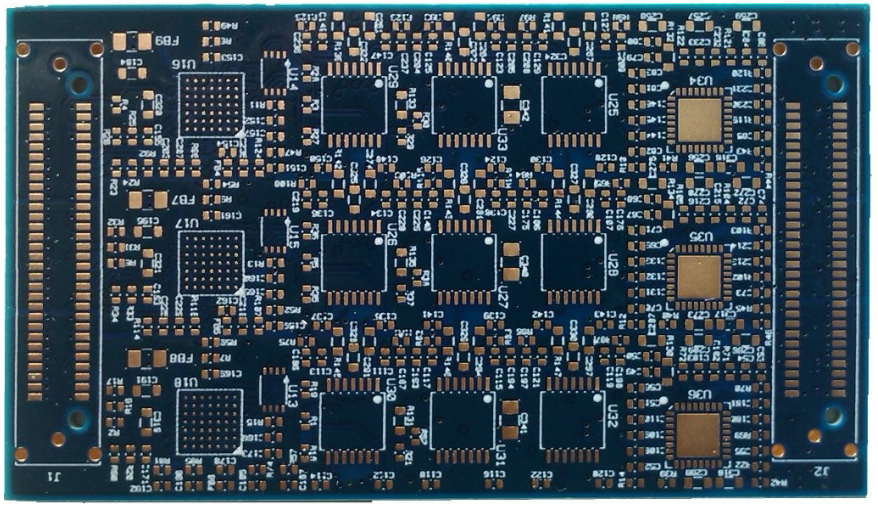
TCKA, TCKB
8 x M-LVDS

+5V/GND
3 x 2.5V
DC - CML

Daughter-board

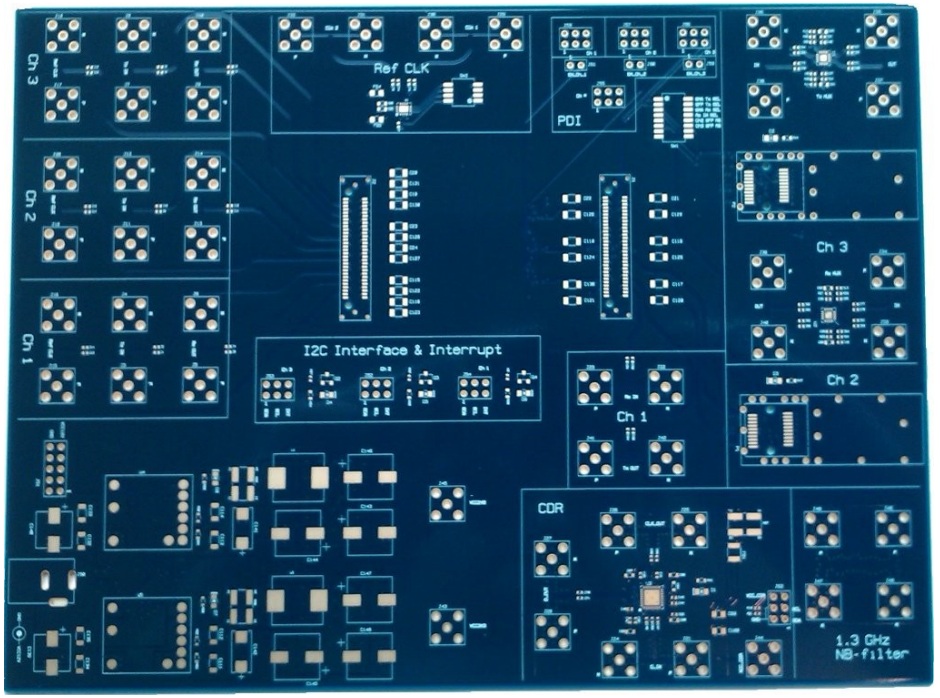
- 3 independent channels
- Delay components for drift compensation
- All phase detectors located on the daughter-board
- ADC/DAC/GPIOs also on the daughter-board
- One µC per channel to run the loop-control
- Component cost ~$420
- Reduce cost and overall complexity of AMC





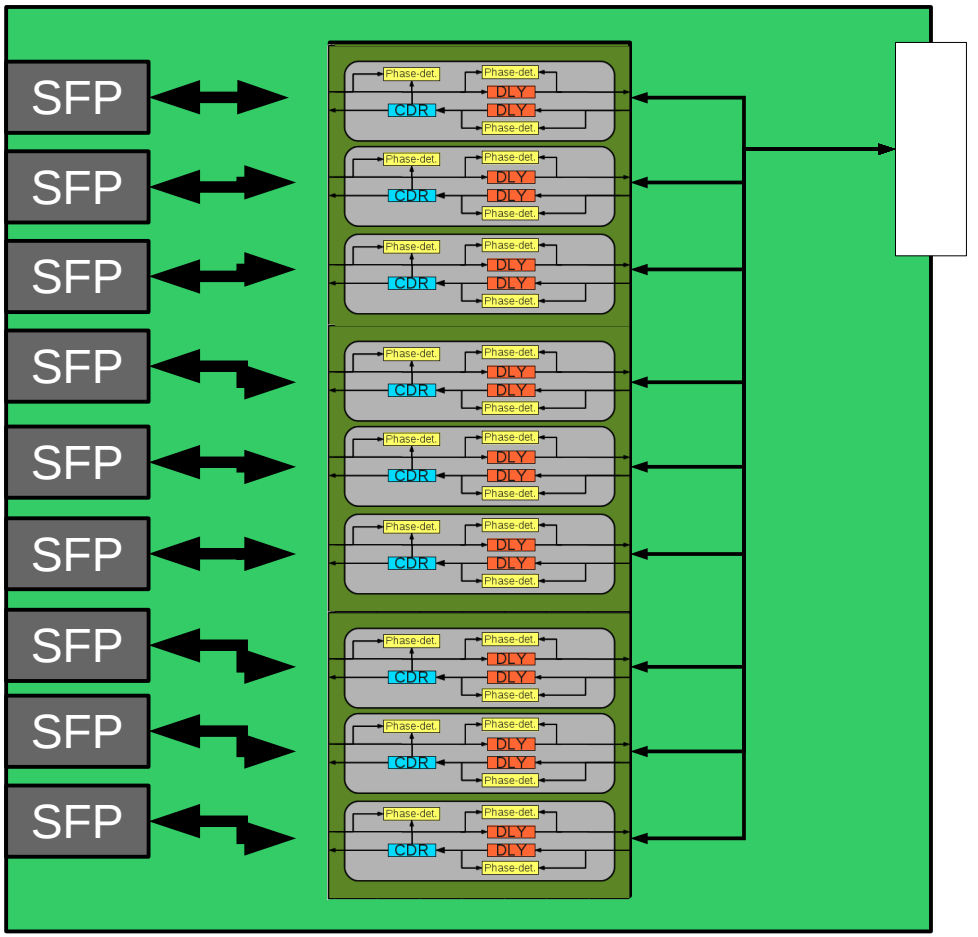
Daughter-board test system

- Software development in parallel to hardware development
- Daughter-board qualification and characterization
- Independent measurements and debug from AMC



Rear Transition Module

- RTM for transmitter fanout
- 9 SFP modules
- 3 daughter boards
- All channels are transmitting the same data
- Receiving input can be selected by a multiplexer



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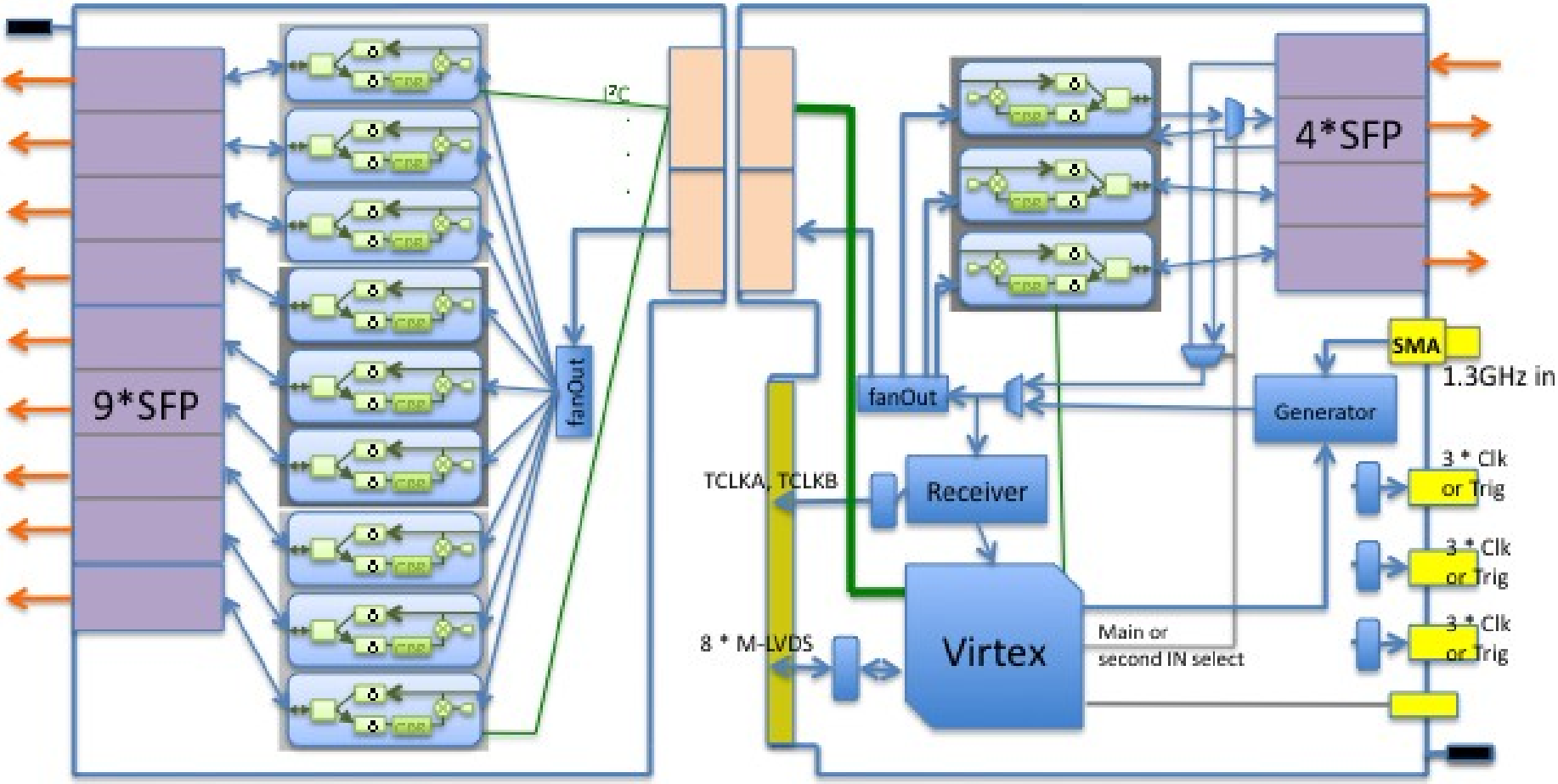

Conclusions and outlook

- Prototype AMC:
  - The board has performed well. Low jitter and good drift-compensation was achieved.
  - Gave us important experience
  - Major firmware development was made, both at SU and DESY
  - Is used by some DESY groups now
- Final AMC:
  - Double size board
  - More cost-efficient
  - Will be sent for manufacturing ASAP !!
  - Need to get it ready for production after the summer !
- Daughter-boards:
  - First boards have been manufactured
  - Needs to be tested and qualified
  - Evaluation board has been designed and manufactured