AGH University of Science and Technology

Status of Readout Electronics for LumiCal detector and Future Plans

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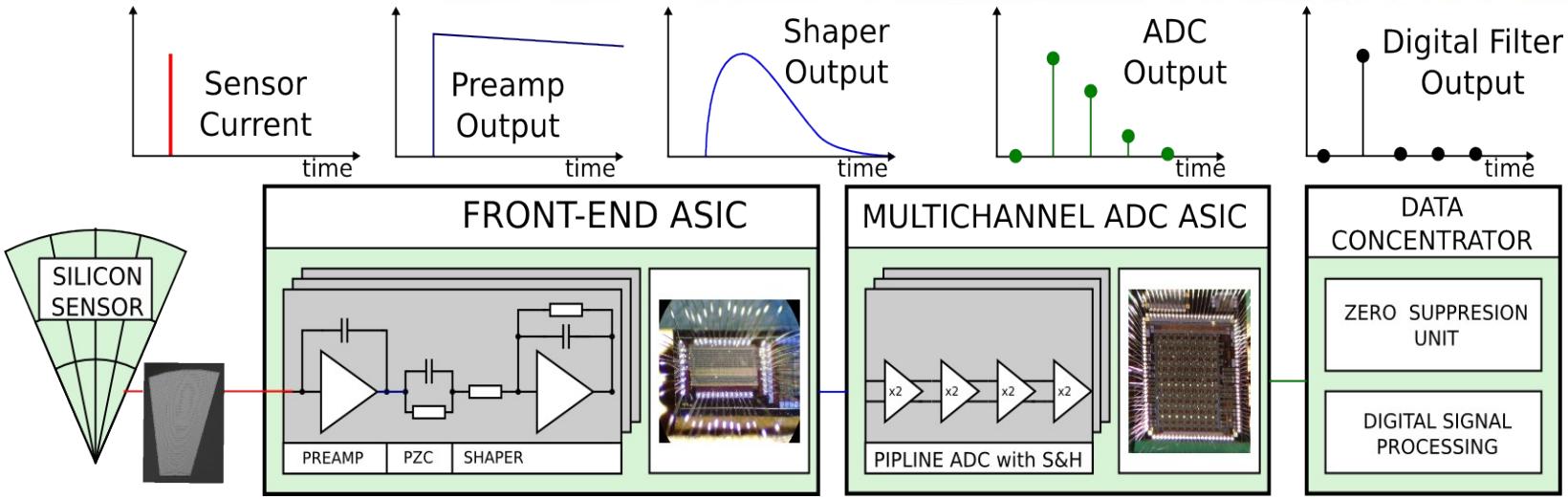
Outline

- Status and ongoing works with readout electronics developed in AMS 0.35um
- Development of new readout for LumiCal detector in IBM 130nm

LumiCal detector readout chain



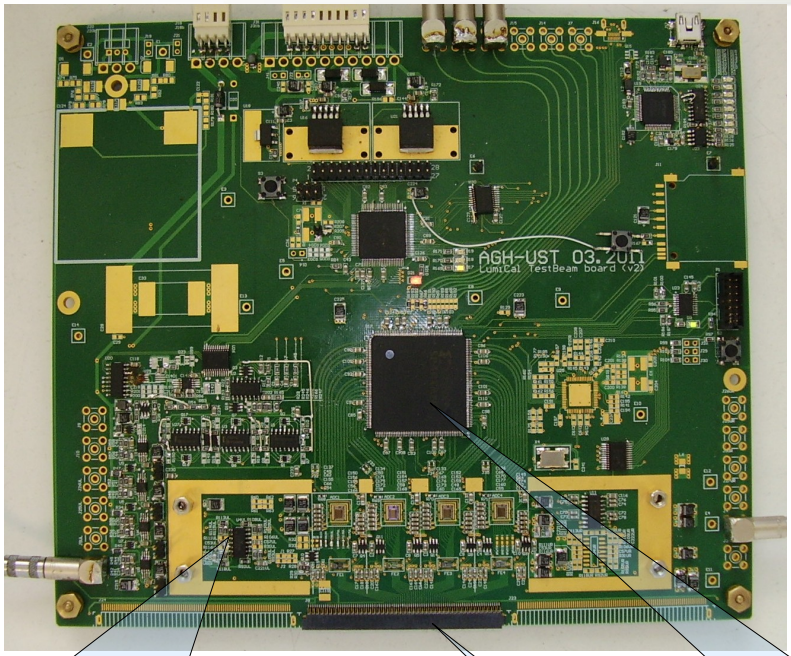
Main components of LumiCal detector readout:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (AMS 0.35um)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (AMS 0.35um)
- FPGA based data concentrator and further readout

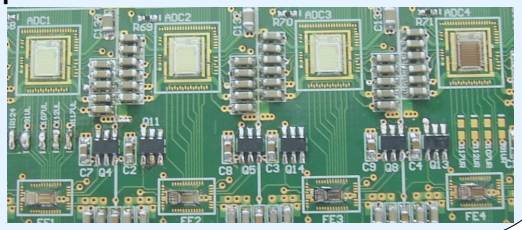
Front-end - M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminosity detector at ILC", NIM A 608 p.169-174, 2009

Multichannel ADC - M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012

32 channels readout module
Final readout based on AMS 0.35um ASICs



4 pairs of front-end+ADC ASICs



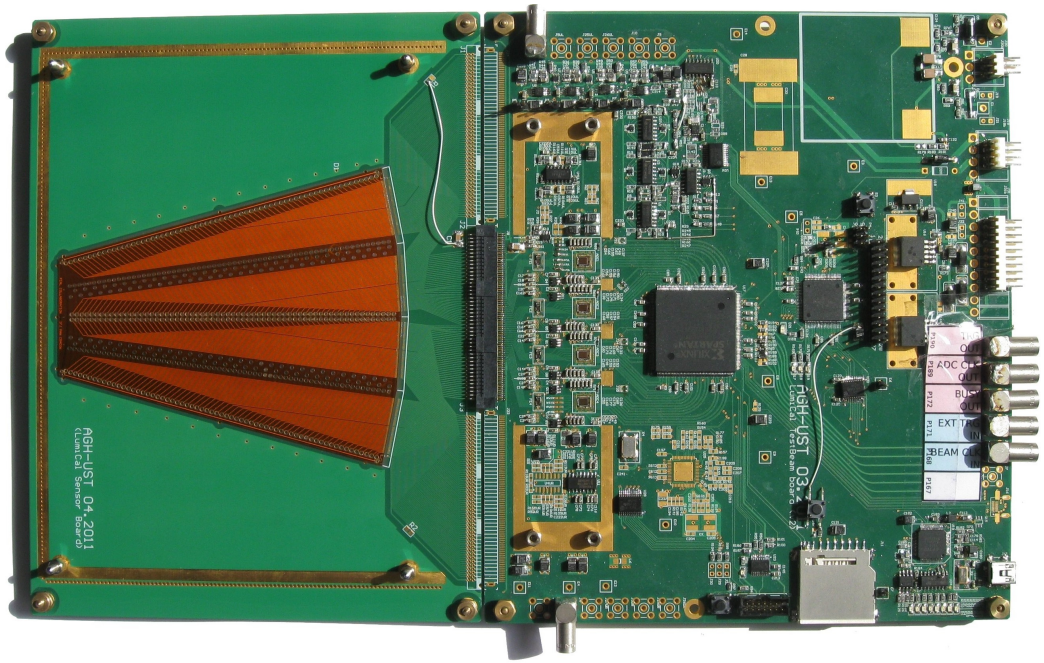
Data concentrator
Xilinx Spartan 3E

sensor
connector

- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock usec for synchronization) ILC mode

Sz. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", Journal of Instrumentation JINST 7 T01004 2012

LumiCal detector module



Good performance of detector module verified on 2 testbeams in 2011

Power pulsing (1ms_ON/199ms_OFF, ASICs Power_ON/OFF >30)

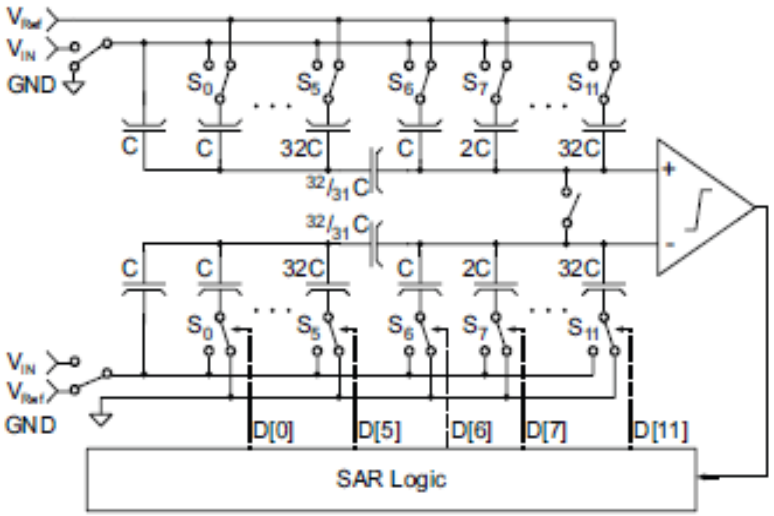
Two modules available (Cracow, Zeuthen), with two sensor boards (BeamCal, LumiCal)

Using deconvolution, tests for CLIC are performed with asynchronous readout

New developments in IBM 130nm

- Readout system developed in AMS 0.35um works very well, but in view of final readout of LumiCal at ILC/CLIC, some parameters (power consumption, speed, radiation hardness) would need to be improved...
- The design of readout with the same architecture (FE+ADC in each channel) has been started in IBM 130nm
  - Prototypes submitted in February 2012
    - 10-bit SAR ADC, PLL, SLVS I/O
  - Prototypes submitted yesterday...
    - Improved 10-bit SAR ADC&PLL&SLVS, 6-bit SAR ADC
  - Due to"last minute" problems front-end postponed...

Design of SAR ADC in IBM 130nm



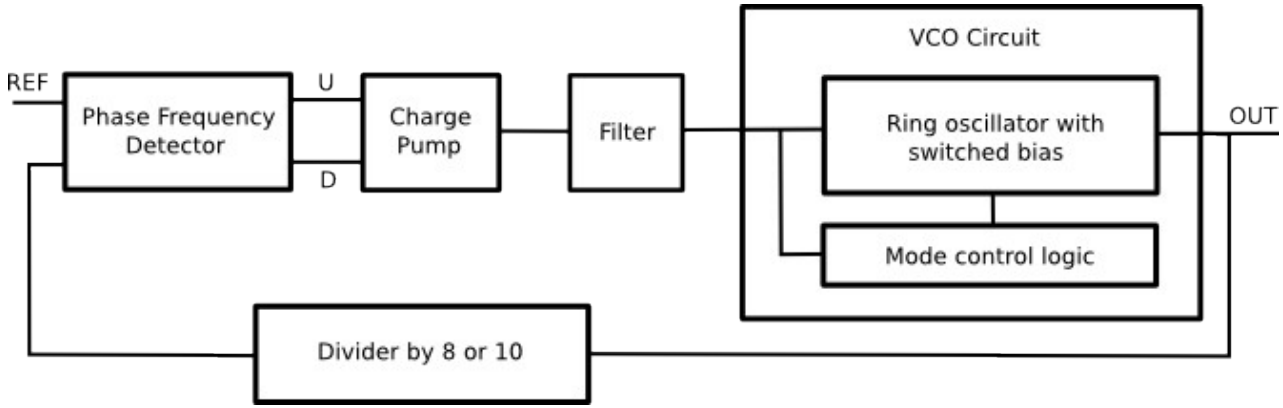
Submitted designs of 10-bit ADC

- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – No-bit clk
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch

Submitted design of 6-bit ADC

- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – No-bit clk
- Scalable frequency (up to ~100 MS/s) and power consumption
- <0.5 mW at 40MS/s
- ~40um pitch

Design of PLL for data serialization in IBM 130nm



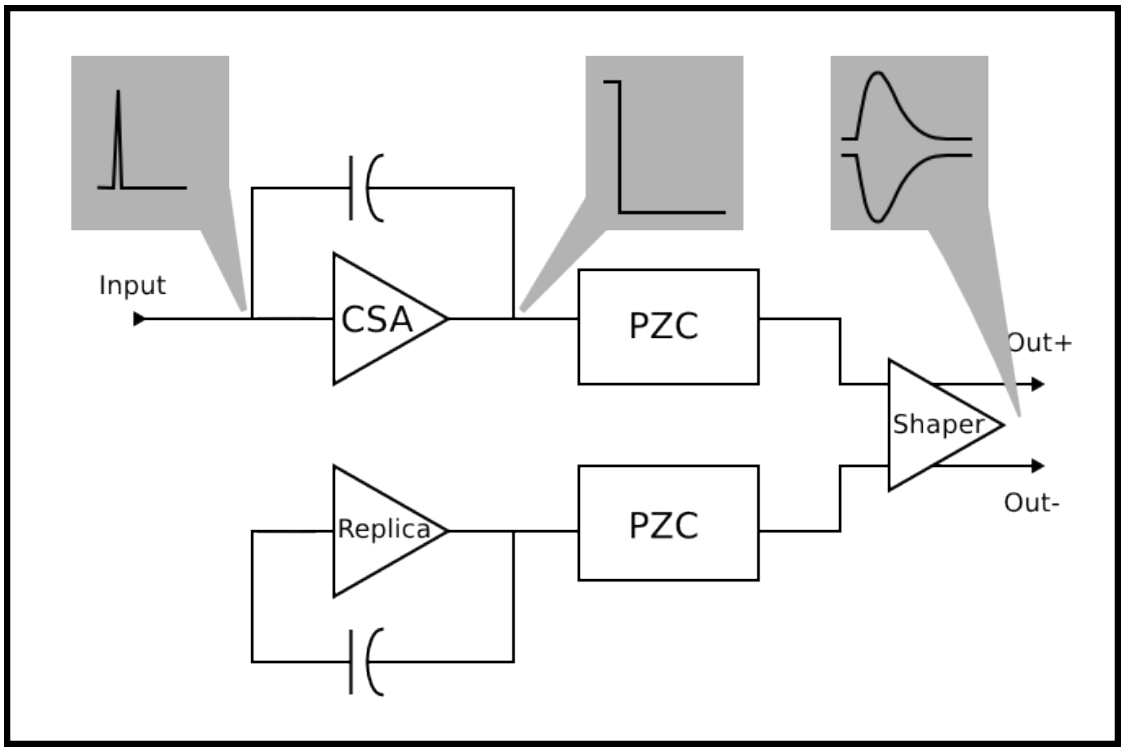
Prototype submitted in February 2012

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 60MHz – 520MHz,
- VCO frequency division by 8 or 10
- Power consumption <0.5mW at 500MHz
- Area 200um x 160um
- Simulated jitter RMS<5ps

PLL submitted in yesterday…

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- Jitter RMS<5ps

Front-end design in IBM 130nm, in progress...



Specifications, still under discussions:

- Charge Sensitive Preamplifier with PZC
- Fully differential CR-RC Shaper
- Variable gain: 0.15 $^{mV}/_{fC}$ – 15 $^{mV}/_{fC}$

(Two modes: calibration – high gain and physics – low gain**)**

- Variable peaking time: 25 – 100 ns
- Cdet ~ 5 - 30 pF
- Noise < 0.4 fC (SNR ~ 10 for MIP)
- Power cons. ~2mW/channel

R&D on microelectronics within AIDA

- Within AIDA WP3 task a network activity is set up to assess advanced CMOS technologies, the best candidates for use in future HEP experiments
- Design of microelectronics libraries and blocks to be made available to the community of users in HEP is foreseen
- The 65nm CMOS has been chosen as the baseline technology
- AGH-UST considers to try some of the blocks: ADC, PLL, SLVS
- Is there any interest in FCAL for such advanced (and expensive) technology ???

Summary and future plans

- The development in AMS 0.35um completed with well performing and already extensively used 32 channel readout module. ADC chips still available and maybe some front-end...
- First prototypes of main LumiCal readout blocks designed in IBM 130nm, ADC and PLL already submitted, front-end will be submitted in 2012
- We are eagerly waiting to test the first ASICs in 130nm...
- In optimistic scenario the projects of multichannel versions may be designed and submitted in 2013. Since there are very limited AIDA resources at AGH-UST, for this aim more resources will need to be found.

Thank you for your attention

Design of calorimeter prototype - AIDA
Tentative sched./Who what ?/what is forgotten?

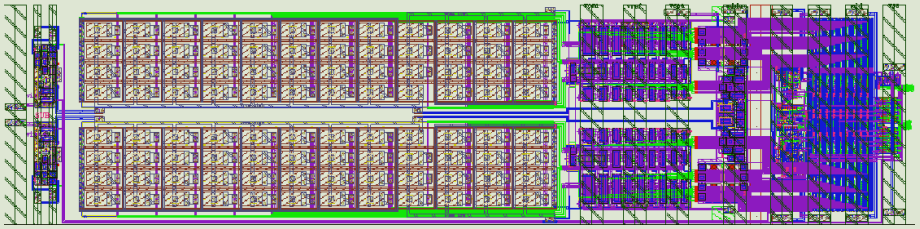
- Mechanical structure - ready ~ July 2012
- Tungsten structure
  - First 5 plates ~June 2012, next part 2013 ?
- Sensors – ready
- ASICs – key factor for the timeline
  - ADC – we will test first prototype soon, FE submission august/november 2012, second FE submission ~mid 2013
  - FE&ADC ASICs ready end of 2013 (optimistically), funds for 2013 needs to be found
- Readout electronics – development should start begin. 2013
- DAQ ?
- Position control ?
- Construction and tests – should start in 2014

Calorimeter prototype – AIDA whats is done ?

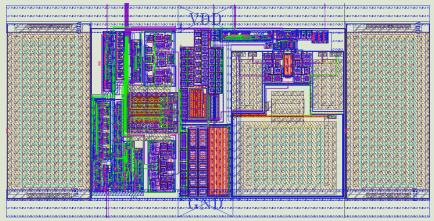
Mechanical structure

CERN

Layouts of ASICs prototypes in IBM 130nm CMOS



10-bit ADC
600um x 145um



PLL
310um x 150um

AGH-UST (submitted in Feb. 2012)

I'd be willing to add photos of other pieces done ???
Tungsten plates are on the way...(AGH-UST, CERN, IFJ-PAN)