# Analysis of the Beam Test data for the Beam Calorimeter Prototype

Olga Novgorodova DESY, BTU Cottbus FCAL Workshop 7-9 May, 2012 Zeuthen







#### Outline



- **> Forward Calorimeters**
- > Test Beam Measurements
- > CAEN ADC Analysis
- > Common Mode Noise
- > Deconvolution Method
- > Deposition Simulation
- > Conclusions







**Precise luminosity measurement**,

Hermeticity (electron detection at low polar angles), Assisting beam tuning (fast feedback of BeamCal data to machine)

Challenges: radiation hardness (BeamCal), high precision (LumiCal) and fast readout (both), ygorodova | FCAL Meeting, Zeuthen | 7-9 May 2012 | Page 3



#### **Beam Cal Prototype**











- > GaAs (BeamCal) New Segmentation
- > Fan Out (DC  $\rightarrow$  AC)
- > 4 8 channel FE ASIC's (AMS 0.35um) + 4 8 channel ADC ASIC's + FPGA concentrator (Xilinx Spartan 3E) + Power pulsing
- Connector between RO and Sensor board. 3 Read Out boards were equipped (LumiCal 2; BeamCal 1) All connect-able to each other
- > ASIC's with two technologies



#### **Test Beam Set UP**







#### **Test Beams**





Test Beams DESY II 2010 – 2011(Summer – Autumn)

LumiCal & BeamCal prototypes + Strip MVD ZEUS Telescope Validation of chain ( Sensor + Fan Out + FE ASIC's + CAEN ADC)– 2010 Validation of chain ( Sensor + Fan Out + FE ASIC's +ASIC's ADC)– 2011



#### What was Planed

#### > TB Plans:

- > S/N ratio,
- > CCE,
- > Position sensitivity,
- > Homogeneity for 32 channel system,
- > Crosstalk.
- > Behavior on the edges between pads,
- > 4 gains operation & Multi-particle irradiation.
- > Comparison with 2010 Test Beam Data.



# **Signal Analysis**





- Two ADC's were used (CAEN ADC 2ns & on Board ASIC's ADC 50ns sampling (ADC sampling rate is up to 20 MS/s)
- > 32 pads were read simultaneously (2011), 8 channels in 2010
- > Two different front-end electronics RC, FET
- >CMN observed



# **Signal Analysis Methods**





#### > 3 Analysis Methods

- > Signal Amplitude (Veta, Titi),
- > Signal Integral (Eliza),
- > Deconvolution Amplitude(Olga)
- > Two independent ADC's (shifted in respect to the trigger)
- > Time window is divided in 2 for baseline and signal calculations:
  - > 0-400 and 400-800 ns for CAEN ADC
  - > 0-16 and 16-32 sample ASIC's ADC
- > Amplitude sample with maximum value
- > Integral As a Fitting of the Signals
- > Deconvolution Amplitude Sum of two non zero bins



## **Common Mode Noise CAEN ADC**





- Correlation between pedestals values within 8 CAEN ADC channels and within 32 channels of ASIC's ADC
- CAEN ADC was connected to 2 FE ASIC's, odd and even channels. Two channels with high gain and two low gain.
- > Correlation is found to be within one FE ASIC's.
- > For 32 channels results will be shown below.



### **CAEN ADC Amplitude**





- > Saturation is a result of CAEN ADC dynamic range (0-255 ADC counts)
- > MPV is stable, S/N varies between 10 to 20
- > CMN was not subtracted

CAEN ADC Ch N	0	1	2	3	4	5	6	7
MPV	32.1	32.0	15.6	15.9	16.1	32.2	32.3	16.2
σ	1.43	1.42	1.01	1.4	1.14	1.74	165	0.99
S/N	22.4	22.5	15.0	11.4	14.1	18.5	19.57	16.4
Pad Number	26	30	28	32	7	1	3	7

# Proportionality





- > Correlations between different methods (from left to right):
- > FE ASIC's Amplitude vs CAEN ADC Amplitude
- > CAEN ADC Integral vs FE ASIC's Integral (integrals by summing up signal under curve)
- > CAEN ADC Amplitude vs FE ASIC's Integral



# **Common Mode Noise**







> Two different front-end electronics - RC, FET

CMN over each ASIC's – CMN subtraction algorithm from non hit channels – Red Curve after CMN subtraction (Deconvolution mode requires noise reduction)



## **Common Mode Noise Subtraction**



- > 0-1000 samples to calculate averaged pedestal for full event and for each sample.
- > Subtraction of the averaged pedestal values for each sample
- > Calculation of the CMN for each sample for each FE ASIC's, taking into account gains between 0-3 and 4-7 channels of each FE ASIC's
- > CMN is calculated for the channels which were not hit ( maximum value of the channel has to be less then 5 Pedestal Sigma)
- > CMN is subtracted for each chip individually.



## **Deconvolution Mode**





- > Deconvolution method was tried
- > Deconvolution formula works better after CMN subtraction
- > One or two non zero bins were found
- > Runs with synchronized and unsynchronized ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam)



#### **Deconvolution Mode**





- Sum of two non zero bins for two gains (Blue – first, Black second) – asynchronous
- > S/N ~30 for both gains



- > Pedestal distribution(Blue first, Black second gain) – asynchronous
- > For the window before the signal collect deconvoluted values for each bin
- > Pedestal Sigma differs in factor 2



#### Deconvolution





#### > ADC Clock source

- Internal (asynchronous with beam operation)
- External (beam clock used to synchronize with beam)
- Synchronized data show perfect correlation.



#### **Deposition in GaAs**





>	<b>Test Beam and</b>
	Sr90 Setup were
	simulated with
	Geant3
	(S.Schuwalow)

> Deposition in the GaAs sensors were collected for different electron energies

Thickness	Dep. En.	e-h energy	e-h pairs per mkm
500 mkm GaAs	$0.3455 { m MeV}$	4.3 eV	160,7 (2.0  GeV)
500 mkm GaAs	$0.3513 { m MeV}$	4.3 eV	163,4 (4.0  GeV)
500 mkm GaAs	$0.3526 { m MeV}$	4.3 eV	164,0 (4.5  GeV)



#### Conclusions



BeamCal prototypes were tested at the 2 - 4,5GeV electron beam in 2010 - 2011. It is showing perfect performance, S/N ~20-30

Functionality of the chain: ASIC's ADC + ASIC's FE + fan-out + sensors, positively verified on test beam

Beam test of 32 channel prototypes were successfully tested in 2011 including new ASIC's ADC with S/N > 20 and analysis is ongoing

CAEN ADC data is in agreement between 2010 and 2011

**CMN** was observed

Deconvolution method showed to be correlated with amplitude

Plans are to finish Test Beam Data analysis in this summer.

