BCM Data Logger

Aim

- We observe a readout bottleneck with the current TDC.
- David suggested a module to store the distribution of hits throughout a full orbit.
- Using the combination of a fast frontend (FPGA) with some processing power (single board ARM PC) one might be able to implement such a module.

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Key Parameters (1)

Channels

8 channels

ECL, 120Ω termination, removeable

sampling - 6.25ns

2 supplementary channels ('Bunch Filled' + spare)

ECL, 120Ω termination, removeable

or NIM, 50Ω termination

sampling 25ns

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Key Parameters (2)

Triggers

Orbit

NIM, 50Ω termination
leading edge
adjustable w.r.t. start of buffer in steps of bunch clock (range 6μs)

Bunch Clock

NIM, 50Ω termination
leading edge
PLL with board clock (160Mhz)
phase adjustable w.r.t. to board clock (range 6.25ns)

Beam Abort

NIM, 50Ω termination
leading edge
adjustable w.r.t. start of buffer in steps of bunch clock (range 2μs)

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Key Parameters (3)

Front Connectors

- 8x diff. ECL channels
- 2x LEMO channels
- 3x LEMO triggers
- 5x LVDS for status?

Front LEDs

- Module ready (FPGA & SBC configured)
- Module running (Sampling)
- Module stopped (Beam Abort)
- Module busy (Readout)
- Histogram overflow (at least one bin)
- Error
- 10x channel active
- 3x trigger active

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Functionality (1)

Sampling

simple track and hold or transition sensitive sampling?

Buffer

Depth of buffer

8 orbits - 700μs

16 orbits - 1.4ms

32 orbits - 2.85ms

48 orbits - 4.3ms

Double buffer for readout while running?

does readout fit into buffer fill time?

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Functionality (2)

Histogramming

- Binning
  - 6.25ns or wider?
  - *same for supplementary channels?*
- Depth (time for 100% occupancy)
  - 8bits - 23ms
  - 10bits - 91ms
  - 12bits - 365ms
  - 14bits - 1.45s
  - 16bits - 5.8s
- Double histogram for readout while running?