Concept Draft
for
Time Distribution Processing Unit

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Last Changes: 1/13/2012 11:23 AM by M.Penno

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Changes

Date	***Person(s)***	***Description***
2012-01-04	M.Penno	Creation of the Document
2012-01-05 - 2012-01-10	M.Penno/H.Leich	Adding results of the meeting 2012-01-05/10am (W.Lange, H.Henschel, M.E.Castro-Carballo, H.Leich, M.Penno)
2012-01-11 - 2012-01-13	M.Penno	Added Concepts, Waveforms, Cost Estimation

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1 Introduction

This document describes the concept of a *Time Distribution Processing* Unit (TDP). It is a VME hardware component that measures the time of events relative to the orbit trigger event.

The module processes events that are generated by a set of detectors installed close to the beam line. Therefore the module provides several input channels.

When particles in the beam line hit the detectors, they can generate an event on the detector channels. Because of the nature of the LHC accelerator, the beam line is constructed as a ring. Thus, the particles cycle in the accelerator. A complete cycle is an "orbit" and is signalled via the "orbit trigger".

Knowing the time of the orbit trigger and the time of "events" from the detectors allows reconstructing the distribution of particles in the accelerator ring. It is the purpose of the module defined in this document to do the reconstruction in hardware and provide the data to the control system.

2 Requirements

Some requirements have been collected and are summarized here. No guarantee for completeness and correctness yet.

2.1 Environment Usage

The module is to be used in these environments:

- CMS Underground Area S1, in VME Crate, standard background radiation, strong magnet fields
- Laboratory Room, in VME Crate, standard background radiation

The hardware design will not include any precautions against radiation exposure.

A Stand-Alone Operation is not foreseen.

2.2 Interface Description

The TDP has to provide several interfaces. The list that follows is a summary of all interfaces.

- Power via Crate via VME Interface
- VME Bus Interface
- 8+2 channel inputs:
    - 8 input channels dedicated for the detector channels, 6.25ns sample rate
    - 1 input channel dedicated for the Bunch Filled Signal, =25ns sample rate
    - 1 input channel as reserve, =25ns sample rate

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- input for an orbit trigger signal (NIM)
- input for a bunch clock signal (NIM)
- input for a beam abort signal (NIM)
- Network Connection
- USB Master and Slave Connections
- RS232 Serial Interface
- JTAG Connector

LED Indicators:

- Four LEDs (Red, Yellow, Green) that indicate the error status and operation mode of the module + FPGA configuration LED
- Each input channel is paired with a green LED, that indicate up to 2 different states: “event” or “no event”
- Each trigger channel is paired with a yellow LED, that indicates that a trigger event is received
- Each clock input channel is paired with a yellow LED, that indicates that the PLL is locked on the clock

Switches:

- (Optional) Switch/Key to reset the Hardware
- VME base address switch (4x 4 bit rotary switches)

VME Interface

The VME Interface is used to control the TDP’s functionality. The VME Bus Interface is not intended to be used for heavy load data transfers to avoid interference with other VME modules.

The parameters of the interface are:

- Slave Interface Implementation
- A32/D16
- Support for Block transfer
- No support for interrupts

TBD: define the size of the occupied address space

Comment [m1]: I suppose to add the ability of irq, so that it is possible to add this functionality later, if needed. Reason: Even with small payload, irq are a good way to make the daq more efficient and avoid polling. IRQ Support t usually is put into the driver core.

VME Address Switch

The VME base address offset is configured via 4x 4bit hex rotary switches.

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Input Channels

An input channel receives the digitized signal from the corresponding channel of a discriminator unit. The transmitted signal shows if the corresponding detector has "seen" an event above threshold or not.

- ECL Type
- Differential line termination resistors 120Ohms (optionally removable!)
- Logical '1' means "Hit/Event detected"
- electrically not decoupled → common ground
- Pulse Width: >= 14ns
- Connector Type: 16 pin 2 row header, 2.54 mm pitch

Input for orbit trigger

The dedicated input for the orbit trigger. A pulse is received at the start of an orbit. The signal is used to tag the acquired data internally.

- Signal Type: NIM
- 50 Ohm termination
- Trigger: on falling edge
- Pulse width: ~15ns
- Connector Type: Lemo
- Fixed period: 89.1µs (11223.3KHz)
  - ~~6~~µs (earlier) shifted in respect to the start of the circulating bunch train

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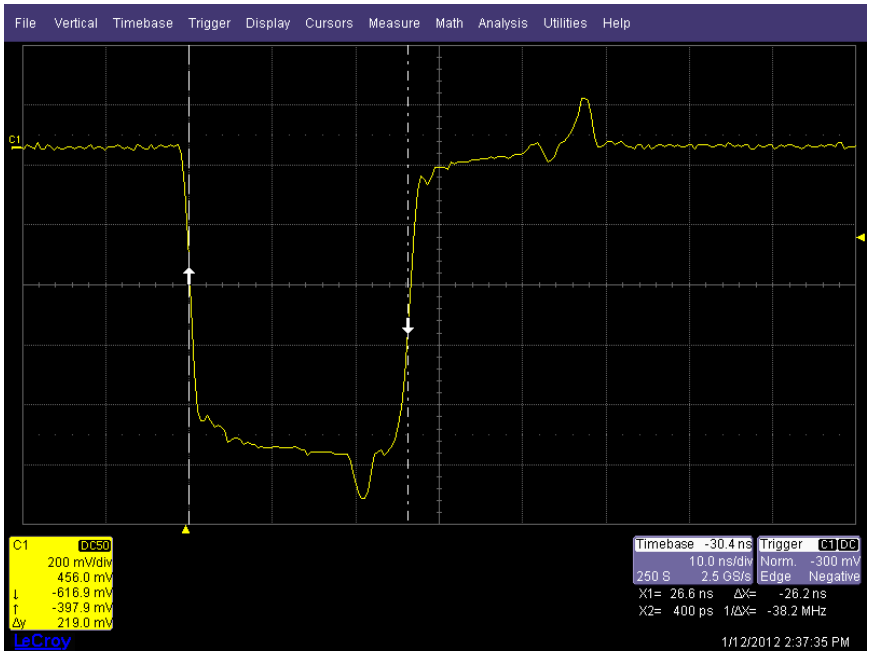

Figure 1 – Orbit Trigger from FIFO

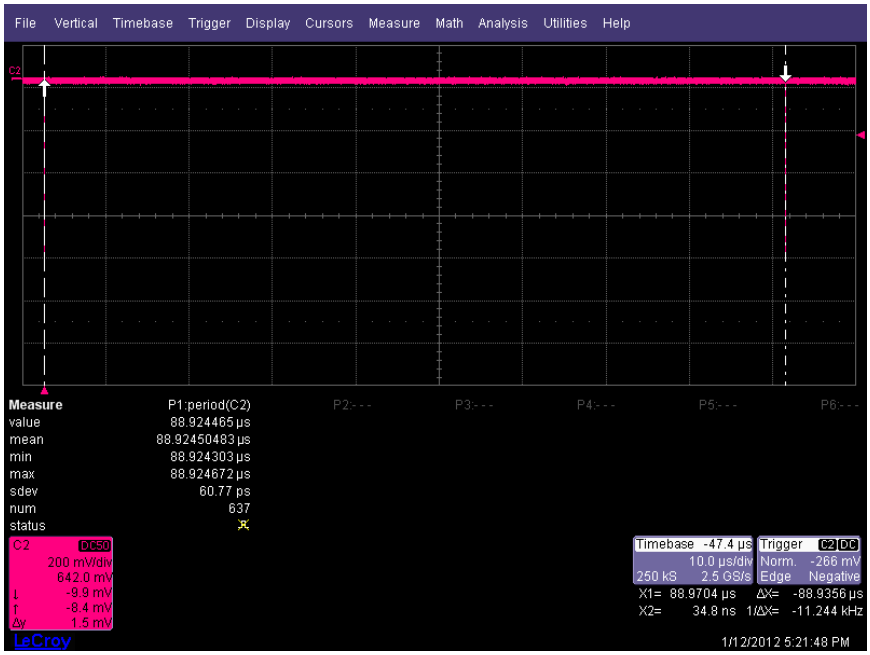

Figure 2 - Orbit Trigger Period

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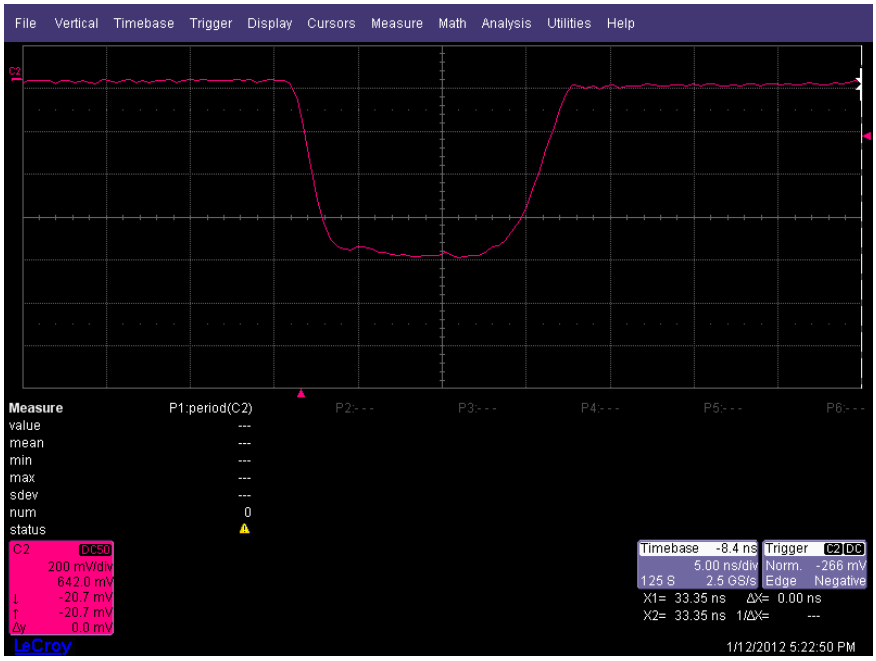

Figure 3 - Orbit Trigger Pulse Shape

Input for bunch clock

A dedicated input for the bunch clock. A pulse is received for every possible bunch within the orbit, hence it is a continuous clock. The signal is used to feed the PLL that generates the internal clocks for the acquisition.

- Signal Type: NIM
- 50 Ohm termination
- Trigger: On rising Edge
- Pulse Width: 10ns
- Connector Type: Lemo
- Fixed Period: 25ns (40MHz)
- The clock shows a pulse at every possible position of a bunch

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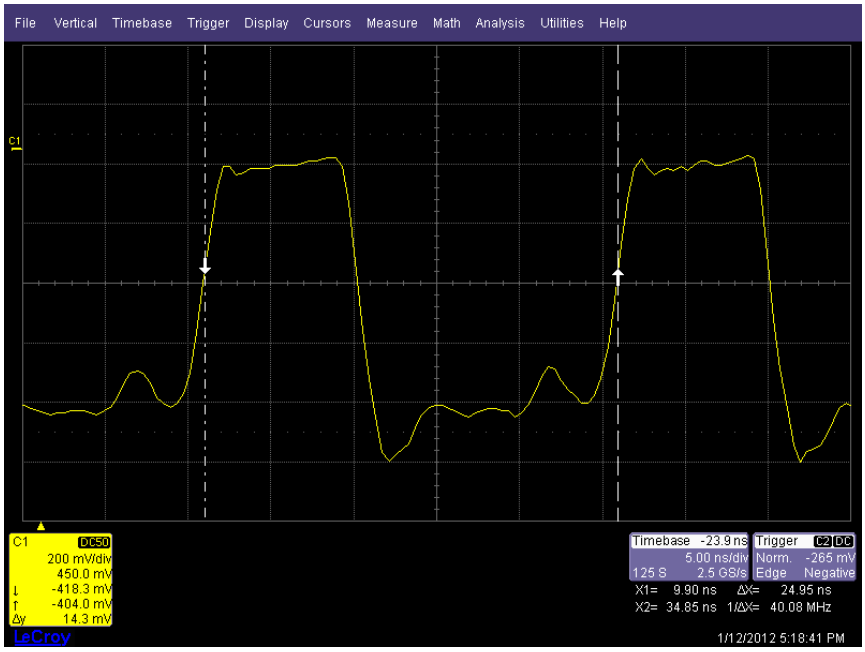

Figure 4 - Bunch Clock Shape

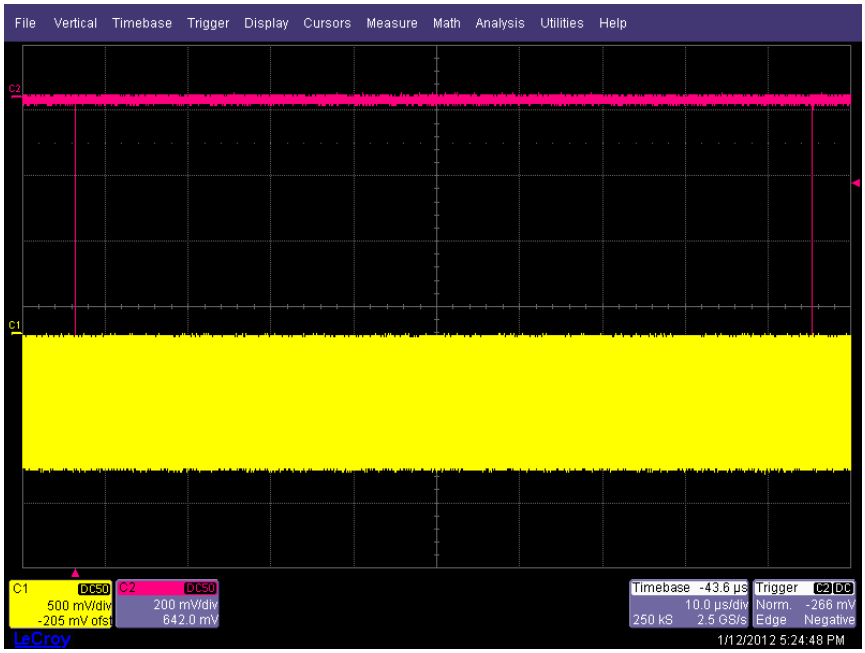

Figure 5 - Relation Ship Orbit Trigger (Upper Graph) and Bunch Clock (Lower Graph)

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Figure 6 – Phase relationship Orbit Trigger (Upper) and Bunch Clock (Lower)

Input for bunch filled

A dedicated input that gives a pulse for every bunch that contains particles. The signal must be recorded as well into the history buffer and the histogram buffer with a min. resolution of 25ns.

- Signal Type : NIM or ECL?
- TBD: Pulse Width, Osci Screenshoot, Connector Type

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Input for beam abort

A dedicated input for signalling a “Beam Abort” event. If signalled, it tells the module to stop acquisition after finishing the actual orbit. Thus receiving the next orbit trigger.

Comment [m2]: Need to clarify, at which time acquisition should stop exactly. Ex.g. if acquisition should continue for N orbits.

- Signal Type: NIM
- 50 Ohm termination
- Connector Type: LEMO

TBD: Pulse Width, Trigger on rising Edge

TBD: Scope Screen Shoot

Network Connection

A network connection is provided to

- allow transfer of heavy payloads as alternative to the VME bus.

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- give ability to control the system remotely
- Connector: RJ45

USB Slave Connection

An USB slave connection is provided to

- allow transfer of heavy payloads as alternative to the VME bus.
- give ability to connect a computer directly to the system
- Connector: USB B

RS232 Serial Interface

The RS232 Interface is used to connect to the Single Board Computer (SBC). It provides a root console to the embedded operating system. It is needed to setup the software running on the SBC and for debugging purpose. It is not used for receiving measurement data.

- 10Pin Header at the PCB with RS232 voltage level
- Connection to pc via adapter cable (Header10 to SUB9 Male) and Null Modem Cable (Female-Female, RX/TX Crossing)

Comment [m3]: Or better to have the connector at the front panel?

JTAG Connector

The JTAG Connecter is used to program the FPGA and its flash device.

- 10Pin Header at the PCB

LEDs

Four LEDs are used to indicate the status of the module:

- LED “FPGA Conf”: Green, Off: FPGA not configured, On: FPGA Design configured
- LED “Error”: Red, On: Error detected, Off: No Error
- LED “Attention”: On: Beam Abort Detected, Acquisition Stopped
- Optional: LED “Acquisition running”: On, if the board is taking measurements

For each input channel and trigger channel a led can be used to indicate, if a trigger signal is received. The LEDs provide feedback about the characteristic of the signal and if cabling is done correctly.

3 Schematic Overview

The following figure describes an abstract block schematic of the module.

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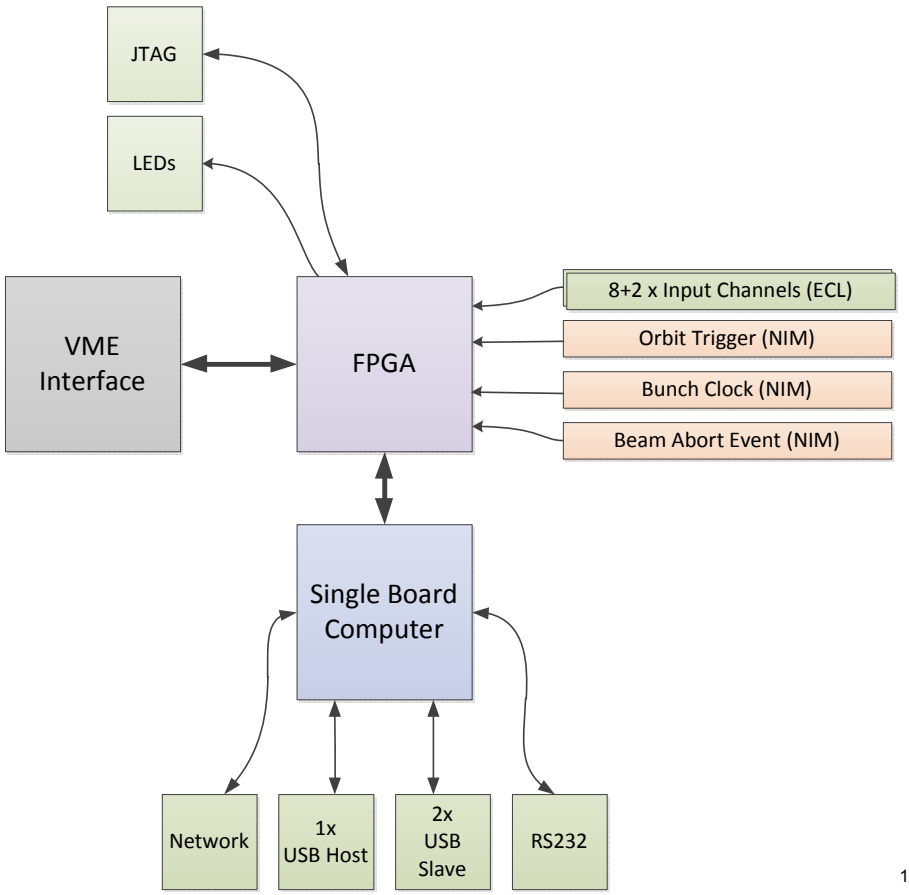

[1]

Figure 7 - Schematic Overview

The following figure shows the module in an example application setup.

[1] SBC – Single Board Computer

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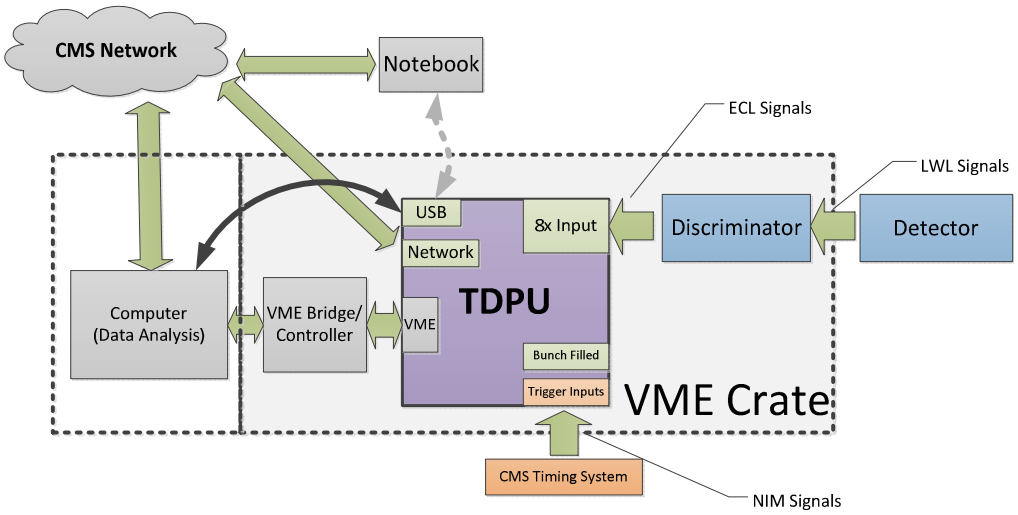

Figure 8 - Bird Eye View: Example Application Setup

4 Acquisition

The data acquisition is the same for every input channel. For each channel, two data buffers are allocated.

An orbit contains 3564 bunches of which up to 2808 might be filled. The sample rate for the input channels is set to 6.25ns (160MHz) to achieve 4 times oversampling. Each channel can produce within each orbit a total of 14256 events.

Because the event is binary (event detected yes/no) this produces a data throughput of 14256 bits per channel per orbit.

4.1 Post Mortem Buffer

This buffer is used to store the sequential occurrence of events for at least the last 8 orbits per channel. This buffer is organized as a ring buffer. When a beam abort is received, the acquisition is stopped and the post mortem buffer does contain the last few orbits of interest.

It is required that the post mortem buffer contains at min. 8 orbit for each channel.

The following table contains the estimated need of memory for different count of history depth (numbers include the two supplementary channels with lower resolution).

Number of Orbits	*Bits per Channel*	*Total Bits (all channels)*
8	114048	969408~~912384~~
10	142560	1211760~~1140480~~

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Number of Orbits	Bits per Channel	Total Bits (all channels)
12	171072	14541121368576
14	199584	16964641596672
16	228096	19388161824768

Table 1 – Different Memory setups of the Post Mortem Buffer

To reduce the amount of memory used, a loss less compression algorithm (. run length encoding) could be used.

TBD: Define at which time the acquisition has to be stopped exactly on beam abort

4.2 Histogram Buffer

This buffer is used to provide a statistical overview of the counts of events in respect to several orbits. The orbit is divided into bins. Each bin represents the count of events relative to the orbit trigger.

The histogram size/bin has been set to 16 Bit. Like this, the histogram is able to accumulate events over 65535 orbits, which is 5839.1 ms. After this time the histogram needs to be read out to avoid data loss. An overflow of a counter of a bin is prevented; the value will remain on its max. (ex.g. 16Bit → 0xffff).

~~As an option to save memory, it is thinkable to combine neighbouring bins into pairs, quadruples, etc. This will result in a less detailed histogram.~~

~~Because of the "Abort Gap" the last 3024 samples are less important and the histogram memory footprint could be reduced there by using less bits for counting and combine bins.~~

The acquisition process is a continuous process. Thus, the histogram might get alternated, while software is trying to readout the data. To avoid data loss or inconsistency during readout, a double buffered system should be used.

Without a double buffer, the acquisition must be stopped during readout to avoid data inconsistency.

When a beam abort is received, the acquisition is stopped to allow post mortem analysis.

TBD: The number of Orbits to be contained in the histogram max.

TBD: Define at which time the acquisition is to be stopped exactly on beam abort

TBD: Is a double buffer needed or is it acceptable to lose some orbits histogram data (might be 20-40 orbits missing each 5sec.)?

4.3 Internal Clock Generation

The Bunch Trigger Input is used to create an internal clock of 160MHz (4 times bunch clock) to allow a 4x oversampling. Thus the sampling period is 6.25ns.

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4.4 Implementation into Hardware

In the following table shows memory footprint and the parameters for the setups that provide full time resolution.

Comment [m4]: Hans: Double Buffer for Histogram is not needed

Setup	Required Bits
8 input channels, no double buffer ***Histogram Buffer: 14256 bins, 16 Bit per bin*** ***Post Mortem Buffer: 8 Orbits a 14256 Events***	2.737 MBit
8 input channels, no double buffer ***Histogram Buffer: 14256 bins, 16 Bit per bin*** ***Post Mortem Buffer: 16 Orbits a 14256 Events***	3.649 MBit
8 input channels, double buffered ***Histogram Buffer: 14256 bins, 16 Bit per bin*** ***Post Mortem Buffer: 8 Orbits a 14256 Events***	4.561 MBit
8 input channels, double buffered ***Histogram Buffer: 14256 bins, 16 Bit per bin*** ***Post Mortem Buffer: 16 Orbits a 14256 Events***	5.474 MBit

Table 2 – Examples of Memory Footprints

The following table shows some FPGAs from Altera and its memory resources.

Device	Memory Resources
EP3C40 EP3C40F324C6N, EP3C40F484C6N	1.161 MBits
EP4CE55 EP4CE55F484C6N	2.34 MBits
EP3C55 EP3C55F484C6N	2.396 MBit
EP4CE75 EP4CE75F484C6N	2.745 MBit
EP3C80 EP3C80F484C6N	2.810 MBit

Table 3 - Memory Resources of some Altera FPGAs, Cyclone III / IV Family

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Because of the large amount of memory needed, the implementations of the example setup in Table 2 are difficult to fit or not fitting at all into the low cost FPGAs[2] that are today available[3].

To address the memory problem, a high speed external memory (ex.g. SRAM[4]) can be used.

TBD: To make further design decisions, the final requirements of the memory must be set

4.5 Solutions

One FPGA Solution

- Use FPGA that is big enough to fit everything
- Positive:
  - One big Design, fair complex design
- Negative
  - Difficult, Risk to Design PCB
  - Very expensive FPGA 2-5K / Piece
  - Heavy Heat Production, Enhanced Power Needs

Multiple FPGA Solution

Many FPGAs are used to divide the problem and memory footprint. Therefore, more communication abilities must be established using parallel busses or a Daisy Chain.

- Use for a group of 5 channels per FPGA (or each 2 channels one low cost FPGA)
  - 2 Channels per FPGA Solution
    - No Double Buffer
    - Double Buffer
  - 5 Channels per FPGA
    - No Double Buffer
    - Double Buffer
- Positive:
  - Same Design for each FPGA possible (when not Daisy Chaining)
  - Good heat Distribution on the PFGA

[2] Taking into account the FPGAs Families, the developer and authors are familiar with.

[3] Excluding Altera Stratix Family and Altera Cyclone V Family. More power full FPGAs will result in higher costs and a more complex systems.

[4] DDR Ram Interface is excluded because of need of IP core license and an overall more complex design

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- fair complex design because reduced channel count
- using low-cost FPGA, cost reduction for PCB parts
- Might allow double buffer feature (thus more expensive FPGAs)

- Neutral
  - Fair Complex PCB Design, when using Daisy Chain for communication between FPGAs and a Single FPGA as Bus Bridge
- Negative:
  - Two FPGA Designs when using Daisy Chain
  - Complex, expensive PCB Design when using no Daisy Chain, because of many pins to route, 2 or 5 times crossing bus systems (of VME and SBC)
  - more power needs
  - no correlation between channels possible (not needed anyway)

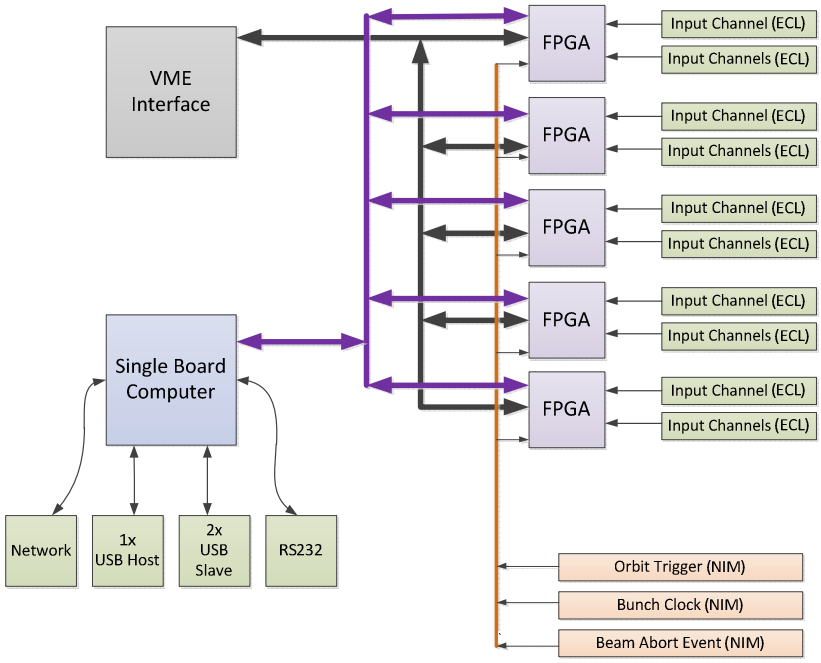

Figure 9 – Multiple FPGA Solution with 5 sections, parallel Bus Design

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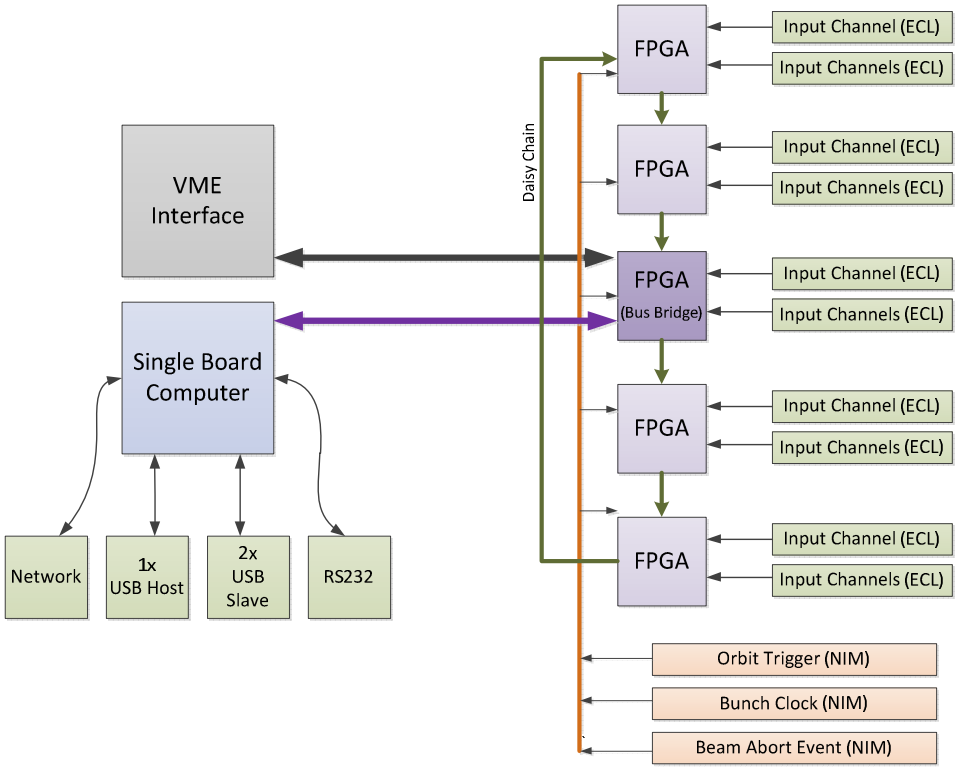

Figure 10 – Multiple FPGA Solution with 5 sections, Daisy Chain Design

External RAM Solution

- Use one low cost FPGA
- Use external Memory components as data storage
- Positive:
  - Fair costs on PCB components[5]
  - Plenty of memory gives opportunity to increase post mortem buffer
  - Might allow double buffer feature (but more complex pcb design!)
- Neutral:
  - complex but fair PCB Design without double buffer
- Negative
  - complex FPGA design, because accessing the external memory in high speed through special burst modes

[5] ex.g. 0.7MBit/Euro at Farnell #1447526

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- special high speed RAM chips needed, might be difficult to order
- even more complex PCB Design with double buffer

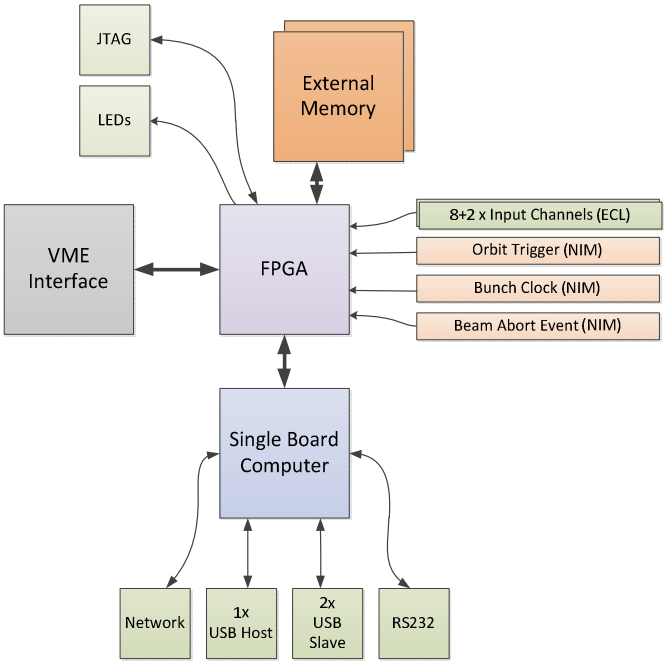

Figure 11 - Solution Single FPGA with ext. RAM

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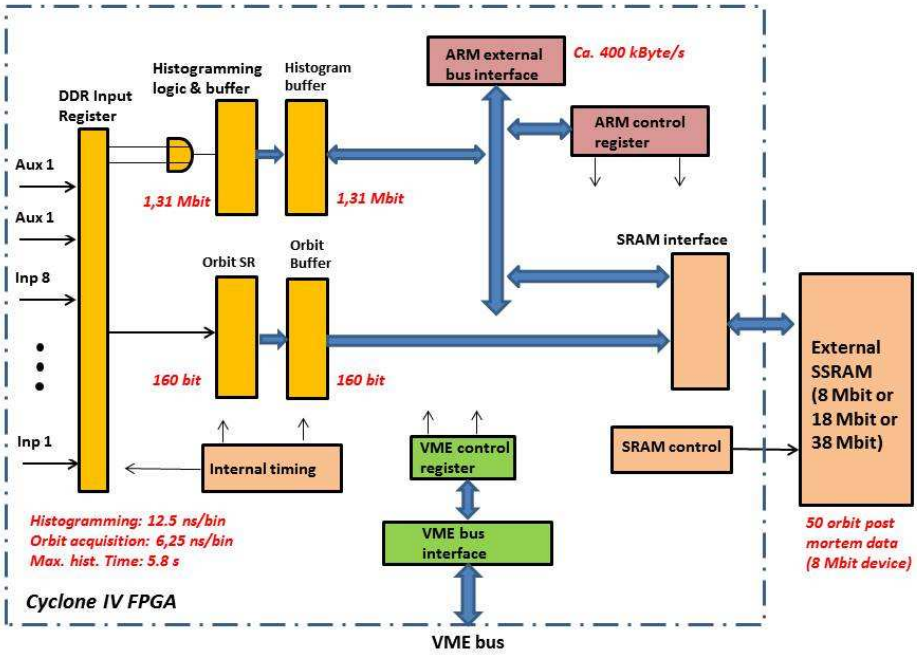
4.6 Detailed single FPGA/external SSRAM implementation schema



- histogramming for up to 10 channels at a rate of 12 ns/bin
- data acquisition of orbit data on all input channels at a rate of 6.25 ns/bin
- time before buffer overflow (histogramming channels): 5.8 ms
- post mortem buffer depth: 50 orbits (in case of a 8 Mbit device)

The histogramming buffers can be read out at any time during data acquisition, so histograms over a longer time may be build by software
To read out the post mortem buffer, the data acquisition has to be interrupted (stopped).

4.7 Cost Estimation

To help select a fitting solution, an estimation of costs has been made based on the variable costs of each solution. That is, the sum of the costs of the FPGA chip and the routing costs. For each pin, whether connected or not, PCB routing costs 1.50Euro.

The total cost will be: Variable Costs + Fixed Costs.

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Fixed Costs are not yet possible to estimate but might be around 2-4 KEuro excluding developing costs.

	A	B	C	D	E	F	G	H	I	J
1		Euro	Kbits	5 FPGA No Dbl Buf	5 FPGA Dbl Buf	2 FPGA NO DBL BUF	2 FPGA DBL BUF	1 FPGA No Dbl Buf	1 FPGA dbl buf	External RAM
2	Memory Need in Kbit	-	-	912	1368	2281	3421	4561	6824	-
3	EP3C40F484C6N:	109.62 €	1161	4,178.10 €	-	-	-	-	-	935.62 €
4	EP3C40F324C6N:	125.00 €	1161	3,055.00 €	-	-	-	-	-	711.00 €
5	EP4CE55F484C6N:	170.00 €	2340	4,480.00 €	4,480.00 €	1,792.00 €	-	-	-	996.00 €
6	EP3C55F484C6N:	179.36 €	2396	4,526.80 €	4,526.80 €	1,810.72 €	-	-	-	1,005.36 €
7	EP4CE75F484C7N:	230.00 €	2754	4,780.00 €	4,780.00 €	1,912.00 €	-	-	-	1,056.00 €
8	EP3C80F484C6N:	258.00 €	2810	4,920.00 €	4,920.00 €	1,968.00 €	-	-	-	1,084.00 €
9	EP3SE50F484C3N	599.21 €	5328	6,626.06 €	6,626.06 €	2,650.43 €	2,650.43 €	1,325.21 €	-	1,425.21 €
10	EP4SGX70DF29C4N	629.92 €	6462	8,999.61 €	8,999.61 €	3,599.84 €	3,599.84 €	1,799.92 €	-	1,899.92 €
11	EP4SGX70DF29C4	692.91 €	6462	9,314.57 €	9,314.57 €	3,725.83 €	3,725.83 €	1,862.91 €	-	1,962.91 €
12	EP3SL110F780C3N	1,232.28 €	4203	12,011.42 €	12,011.42 €	4,804.57 €	4,804.57 €	-	-	2,502.28 €
13	EP3SL150F780C4N	1,720.46 €	5499	14,452.32 €	14,452.32 €	5,780.93 €	5,780.93 €	2,890.46 €	-	2,990.46 €
14	EP4SGX110DF29C4	2,078.74 €	9793	16,243.70 €	16,243.70 €	6,497.48 €	6,497.48 €	3,248.74 €	3,248.74 €	3,348.74 €
15	EP3SE110F780C3N	2,237.01 €	8936	17,035.04 €	17,035.04 €	6,814.02 €	6,814.02 €	3,407.01 €	3,407.01 €	3,507.01 €
16	EP2S180F1020C5N	4,830.71 €	9383	31,803.54 €	31,803.54 €	12,721.42 €	12,721.42 €	6,360.71 €	6,360.71 €	6,460.71 €
17	euro dollar	1.27								
18	ram costs	100.00 €	Legend:							
19			Best Choice							
20			Close to Best Choice							
21			Not acceptable							

Figure 12 - Estimated variable costs per solution (prices 2012/01)

5 Firmware

5.1 State Machine

When the module receives a “Beam Abort” signal, it has to stop operation. After the post mortem buffer has been read successfully, it continues normal operation.

Therefore the module must run in different operation modes:

Configuration Mode

- The acquisition process is stopped
- Configuration registers can be written

Normal Operation

- The acquisition process is running
- Post Mortem Buffer is filled continuously
- Histogram Buffer is filled continuously

Post Mortem Readout Mode

- Activated by “Beam Abort” Event
- The acquisition process is stopped

Comment [m5]: May be not needed

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- Post Mortem Buffer is ready for read out
- Histogram Buffer is ready for read out
- Software must put state machine back into “Normal Operation” after readout is finished

TBD: Automatic switch state after timeout?

5.2 Register Interface

TBD: Fine Adjustment of the Timing via registers?

- Hans: Adjust correlation between orbit clock and actual position in ring buffer
- Hans. Fine adjust phase relative between input sampling and bunch clock (which resolution)
- Hans: Adjust correlation between Beam Abort signal and position in ring buffer
- Counter, that counts number of Orbits received since last read out
- Control Register to change Operation Mode:
- Control Register to clear/zeroset Histogram Buffer

TBD: Adjustments in which scale, ns, us?

6 Hardware

6.1 Frontpanel

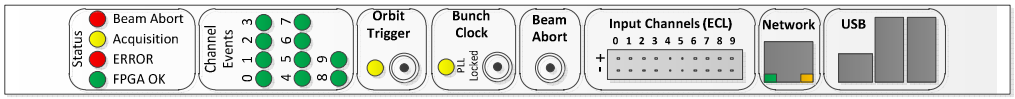

Figure 13 - Draft of the Frontpanel

7 Things to clarify

Please see to all TBD markers in this document.

- Input Channels
  - Which Connectors to use: ECL Signals: 2.54mm Pin Header, NIM: LEMO
  - Final Time Resolution of Histograms: 6.25ns
- Functions of the Hardware Logic
  - Parameters of the acquisition process
  - etc.

Comment [m6]: Hans: If no double buffer is implemented, we need a 4th mode: Acquisition running but Histogram Buffer Filled stopped while Histogram is read out

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8 Additional Sources

8.1 Physics

Filling Scheme

25ns Physics Beam. Filling scheme

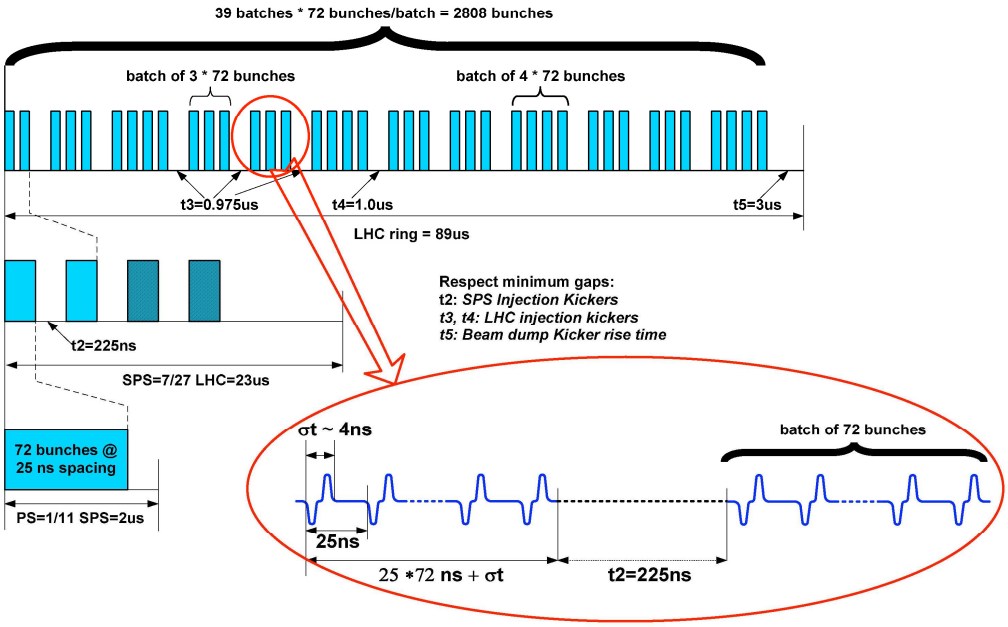

Figure 14 - LHC Beam Filling Scheme

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Location of the Detectors

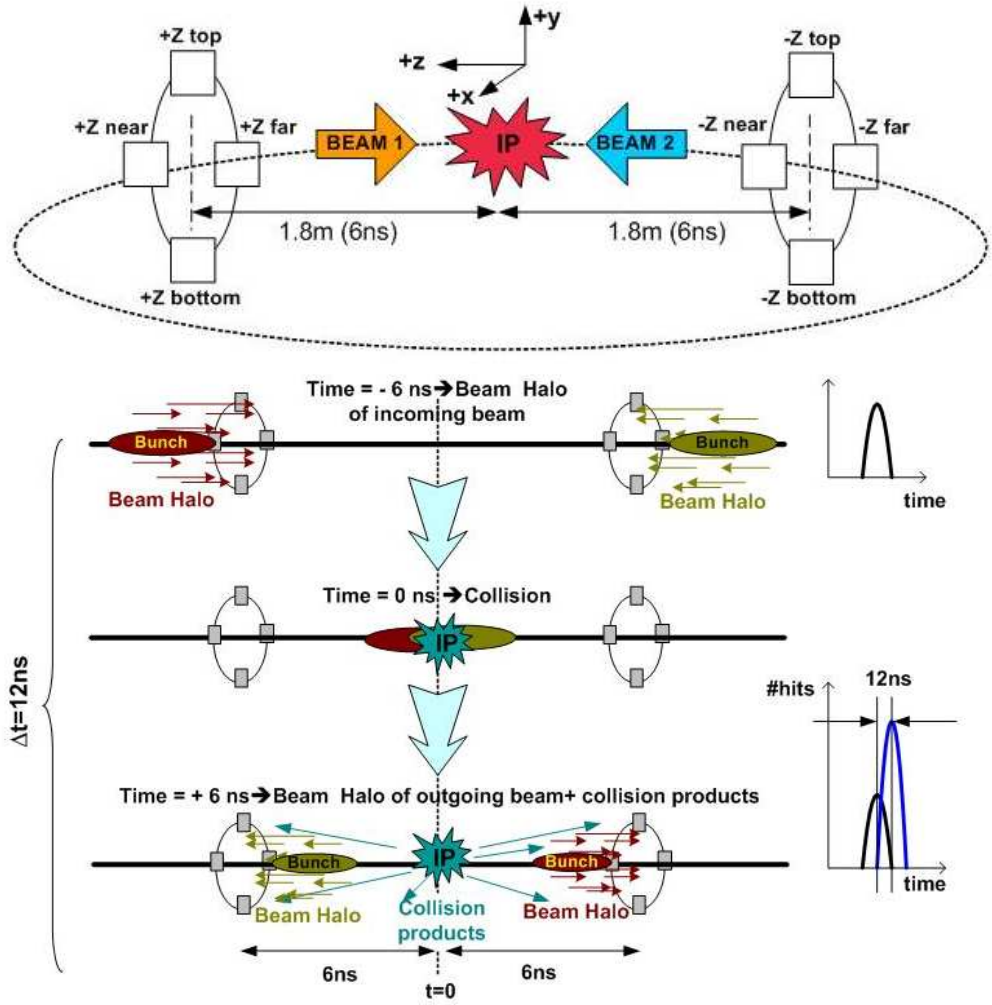

Figure 15 - Location of the 8 detectors according to the interaction point

8.2 Mails

Mail received 2012-01-05

Received from Maria Elena Castro Carballo

Concerning the orbit clock and bunch clock signals, both are synchronous. Roberval Walsh, our colleague from Hamburg doing the data acquisition with the TDC and the analysis, when he wants to plot all of the ~3000 bunches in a 89us orbit, introduces a time correction of around 6us in order to shift bunch #0 to the beginning of the orbit.

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This time correction might change depending of the length of the cables we work with or the additional daq modules we introduce in the daq chain.

Mail 2, Received 2012-01-04

Received from Maria Elena Castro Carballo

Hi,

I send you a schematic diagram with the timing of the signals from the diamond sensors.

We have bunches of the so-called Beam 1 and Beam 2, coming from -Z and +Z sides, every 25 ns.
Let's consider a single diamond on +Z side, if there are not colllisions then, first Beam 1 halo (halo are the particles that travel with beam going through the beam pipe) particles hit the diamond. 12ns later, the beam halo of Beam 2 hit the diamond again. If we make a histogram, we will have 2 gaussians of same height with peaks spaced by 12 ns.

Imagine now there are collisions, now, after colliding in the Interaction Point (IP), the collision products are also detected. The result is a double peak gaussian, where the peak corresponding to the collision products is higher.

Elena

8.3 Single Board Computer

CPU-Modul mit AT91SAM9G20

Für industrielle Anwendungen geeignet

Breite Anschlussmöglichkeiten

Power Management Funktionen

Industrietaugliche Stecker

Stromsparend und langfristig verfügbar

OS Linux oder Windows

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