Pixel test plans 1st half of 2012

Daniel Pitzl, DESY DESY CMS Tracker Upgrade, 10.2.2012



- new ROC design
- beam tests



Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012 D. Pitzl (DESY): Pixel test plans

- PSI46xdb: Enlarged data buffers, reduced crosstalk and better level distribution; - 3 DACs
- PSI46dig_trig: Digital readout added; 4 DACs
- PSI46dig: Trigger mechanism removed; read back; 7 DACs
- 2 TBM versions
- DLT Digital Level Translator for POH, replacing the ALT
- LCDS/LVDS level translator for test boards (LCDS not a standard)
- Other test structures (ADC, PLL)
- Tape out: January 2012 to IBM
- 6 wafers in May 2012 (not yet confirmed from IBM)

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012 https://indico.cern.ch/conferenceDisplay.py?confId=172930 D. Pitzl (DESY): Pixel test plans 3 DESY CM

Data Rate, Efficiency:

- Extended data buffer $32 \rightarrow 80$ cells
- Extended time stamp buffer $16 \rightarrow 24$

Crosstalk, threshold uniformity:

- 6 metal layer (process option)
- Thick top metal (LM instead of MZ process option, +37%)
 - \rightarrow better power and ground distribution (lower resistance)
 - \rightarrow better threshold uniformity
- New routing for calibrate signal \rightarrow less crosstalk of calibrate signal
- Better decoupling of comparator and digital voltage \rightarrow less crosstalk
- Different other minor layout changes to reduce crosstalk

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DAC:

- 3 DACs removed: VRGPR, VRGSH and Vleakage
- All DAC's with power on reset for low power ROC configuration
- Current control instead of voltage control for S&H and analog power supply \rightarrow easier and independent setup

Timing:

- Small performance optimization in column drain mechanism (timing)
- Modified comparator with reduced timewalk
- Same analog read out as PSI46 \rightarrow same test board

Comparison possible between PSI46 and PSI46xdb

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PSI46xdb pixel unit cell



modified in PSI46xdb



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Pixel plans for 1st half of 2012

• Visit to PSI

end Jan

- brought back 5 single chip modules, one full module
- Prepare ROC efficiency measurement:
 - use 2nd CMS pixel plane as timing reference
 - take reference data with present ROC
- New ROCs: PSI46xdb, PSI46dig
 - in production at IBM
 - lab tests with PSI46xdb
 - test beam with PSI46xdb

TB 21, Feb

TB 21, end April

expected at PSI in May early June TB 21, end June-July

2 pixel chips in the EUTelescope

CMS pixel as timing plane

> need general broken line fit for combined tracking

CMS pixel under test

common scintillator trigger

up to 30° tilt

test beam 21: **1-6 GeV** positrons

efficiency measurement

- Trigger and DAQ for 2 test boards and telescope established
- Software to be written:
 - Ink telescope track to hit in timing plane.
 - need General Broken Line fit, taking material into account,
 - with interface to MillePede II for common alignment.
- efficiency = DUT / (Telescope track && timing hit)
 - as function of position, angle, bias voltage, threshold, timing, ...

D. Pitzl (DESY): Pixel test plans

CMS Pixel in the DESY test beam

http://adweb.desy.de/~testbeam/

20.01.2012



CMS Pixel Sensors



design: Tilman Rohe, PSI

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- 60 wafers under production at CIS (Erfurt)
 - standard CMS pixel sensor design (double sided, n-in-n, p-spray insulation).
 - for Karlsruhe, INFN, CERN/Taiwan, MRI, Purdue, DESY.
 - 5 wafers with increased bump pad passivation opening: 30 µm, for DESY.
 - Delivery in Mar 2012.
- Full sensors for first bump bondings.
- Single chip sensors for tests with new ROCs.