# Pixel chip testing at DESY

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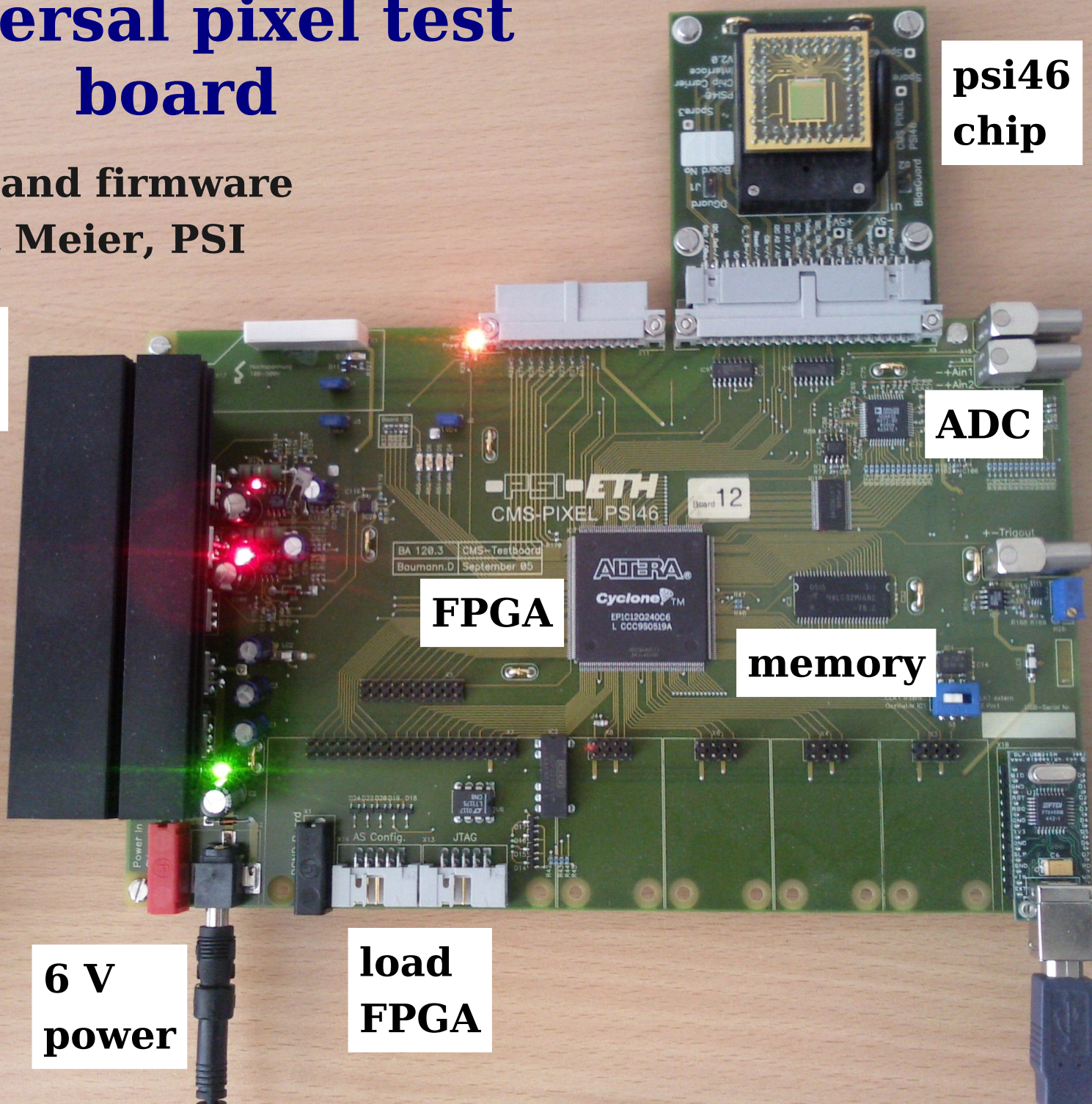
Meeting at PSI, 24/01/2012

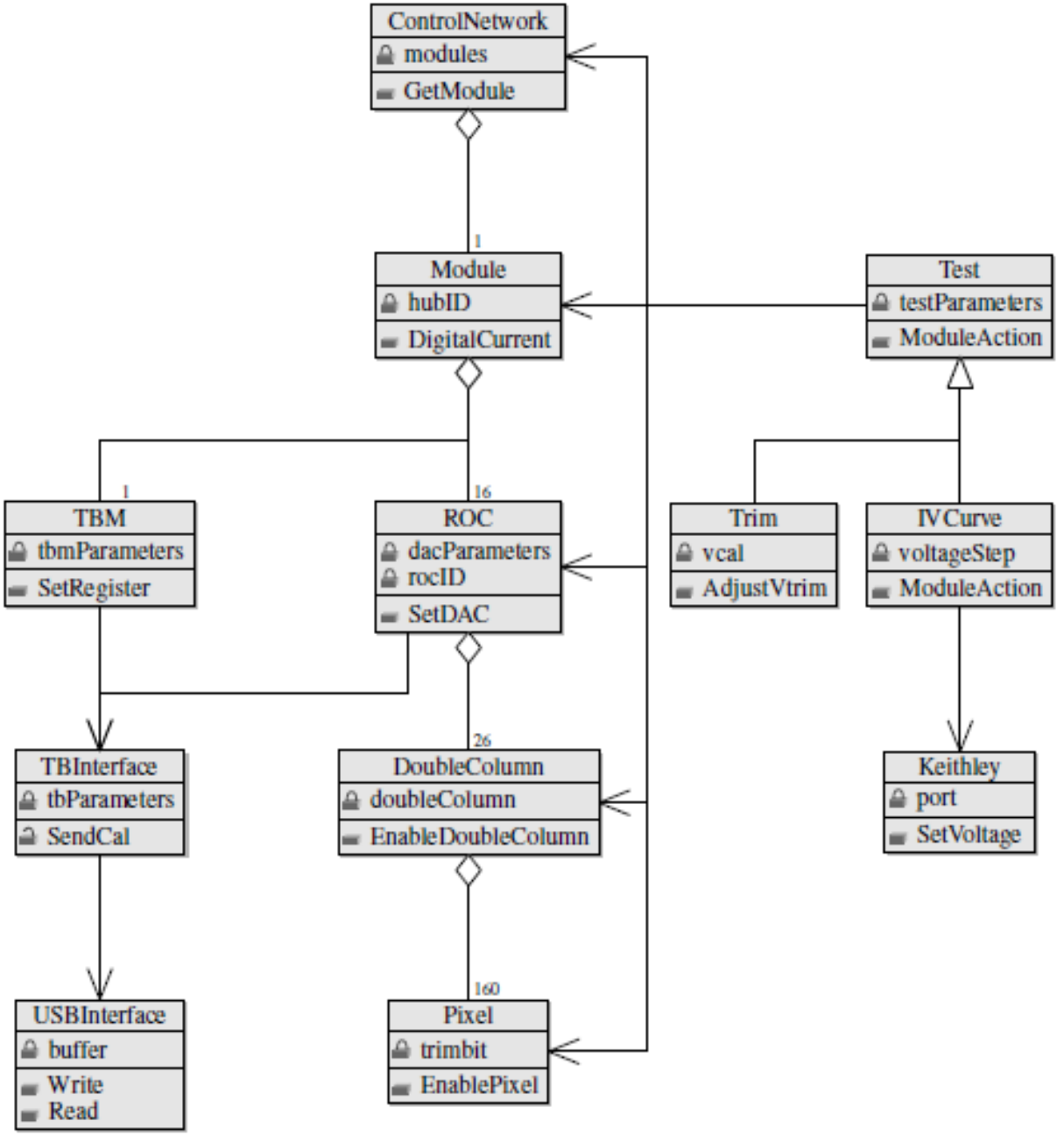
- Installation at DESY
- Some test results
- Known issues, open questions

# Universal pixel test board

**Design and firmware**
**by Beat Meier, PSI**



# psi46expert software




- C++ class library.
- Written by Peter Trüb (ETH, 2005-2007) for Scientific Linux 32 bit.
- Now compiled with g++ 4.4.5 under Ubuntu 10.10 and SL6 64 bit.
- USB interface required some changes (long → int).

# Configuration

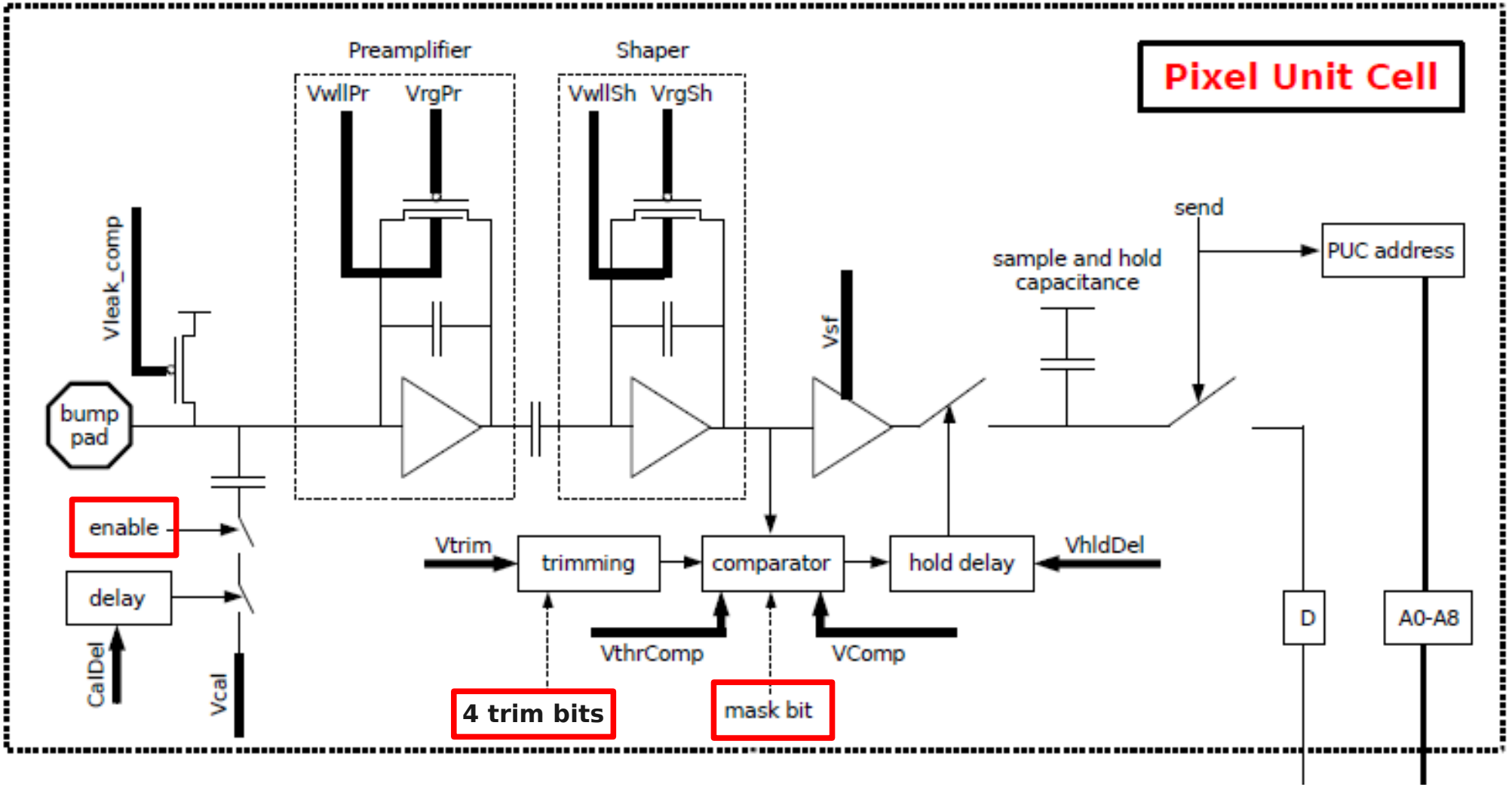
- Configuration files for test board and readout chip imported from PSI:
  - board name,
  - run in 40 MHz mode,
  - set 26 DACs and Control Registers on the ROC,
  - define timing sequence: reset - cal - trigger – token,
  - read and load calibration and trim values,
  - run in 'psi46expert' or 'takeData' mode

# psi46 DACs

| | | |
|---|---|---|
| 1 | Vdig | 6 |
| 2 | Vana | 150 |
| 3 | Vsf | 160 |
| 4 | Vcomp | 10 |
| 5 | Vleak_comp | 0 |
| 6 | VrgPr | 0 |
| 7 | VwllPr | 35 |
| 8 | VrgSh | 0 |
| 9 | VwllSh | 35 |
| 10 | VhldDel | 130 |
| 11 | Vtrim | 7 |
| 12 | VthrComp | 124 |
| 253 | CtrlReg | 0 |
| 254 | WBC | 20 |

| | | |
|---|---|---|
| 13 | VIBias_Bus | 30 |
| 14 | Vbias_sf | 10 |
| 15 | VoffsetOp | 55 |
| 16 | VIbiasOp | 115 |
| 17 | VOffsetR0 | 120 |
| 18 | VIon | 115 |
| 19 | VIbias_PH | 130 |
| 20 | Ibias_DAC | 122 |
| 21 | VIbias_roc | 220 |
| 22 | VIColOr | 100 |
| 23 | Vnpix | 0 |
| 24 | VSumCol | 0 |
| 25 | Vcal | 200 |
| 26 | CalDel | 125 |
| 27 | RangeTemp | 0 |

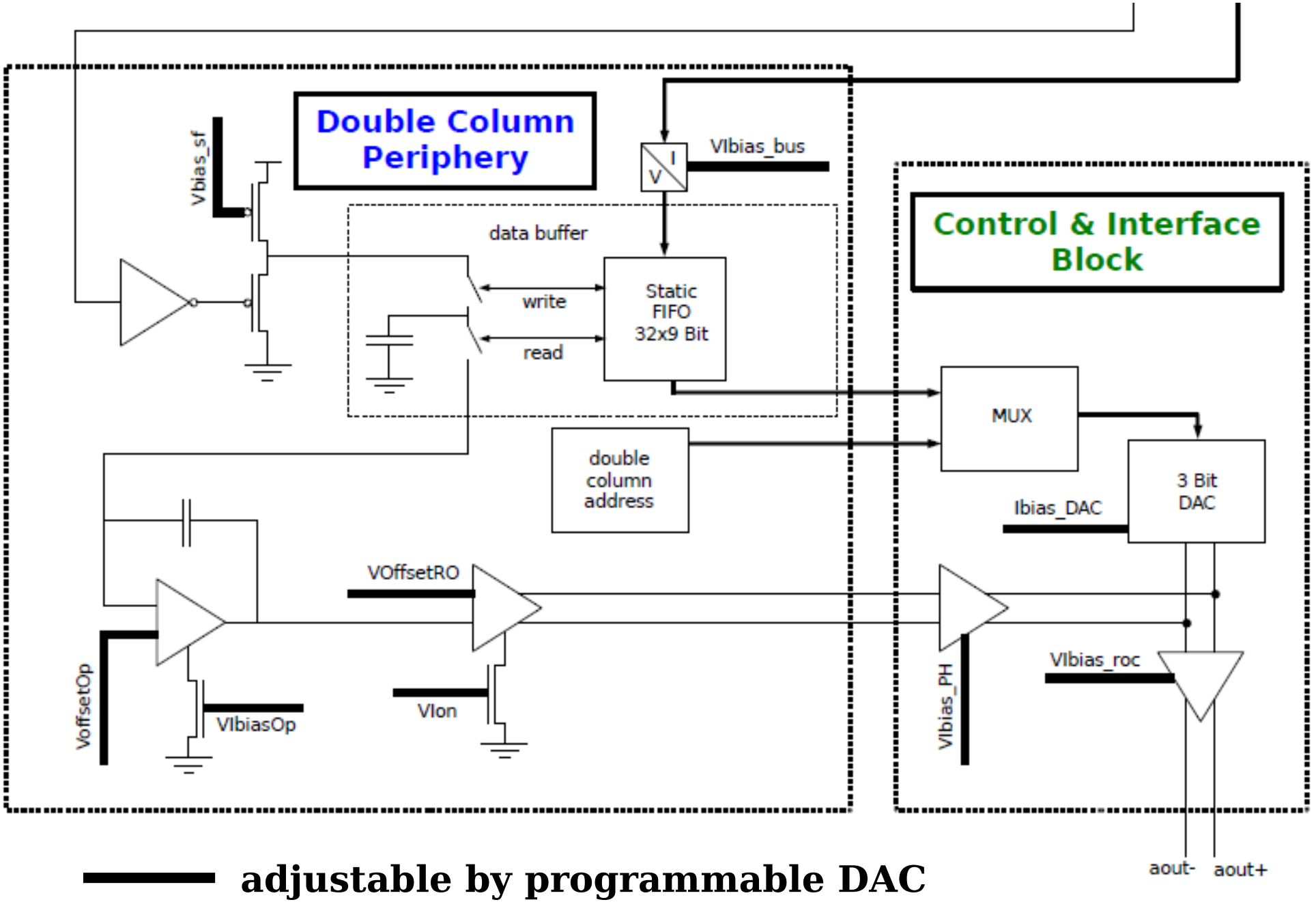
# psi46 pixel readout chip




**adjustable by programmable DAC, per ROC**

**programmable register, per pixel**

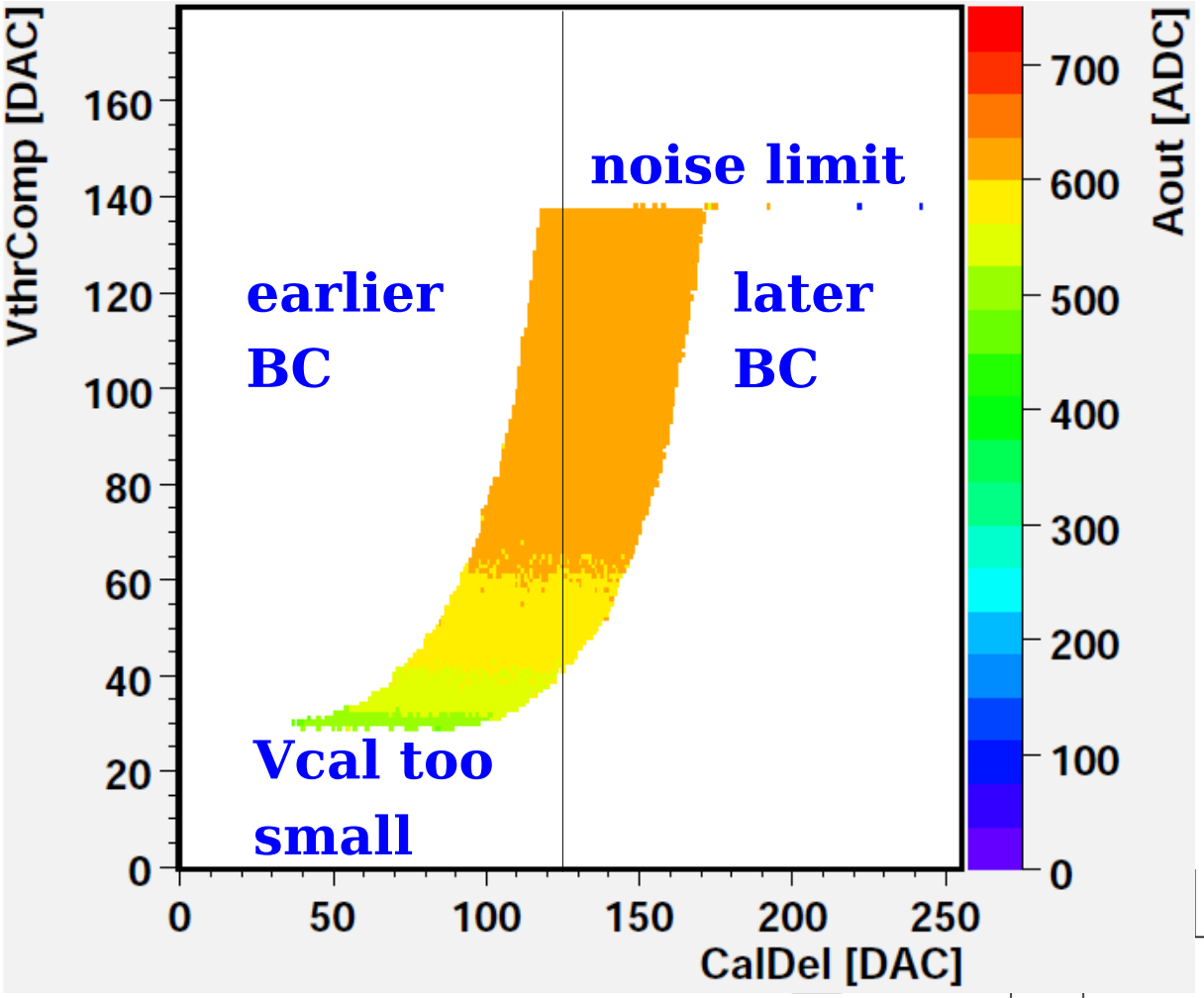
# psi46 pixel readout chip



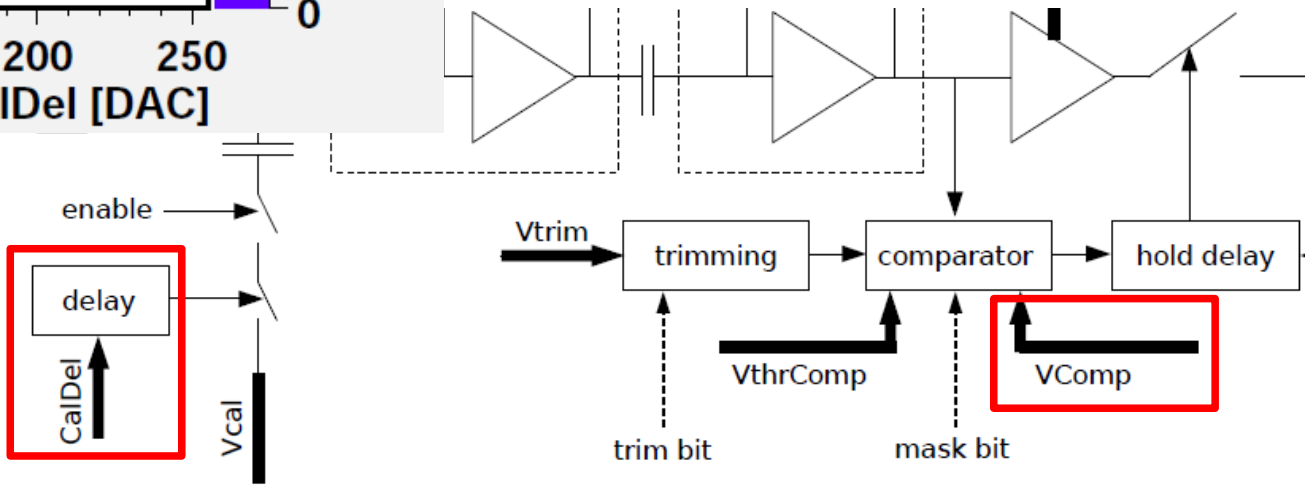

**adjustable by programmable DAC**

# Some test results

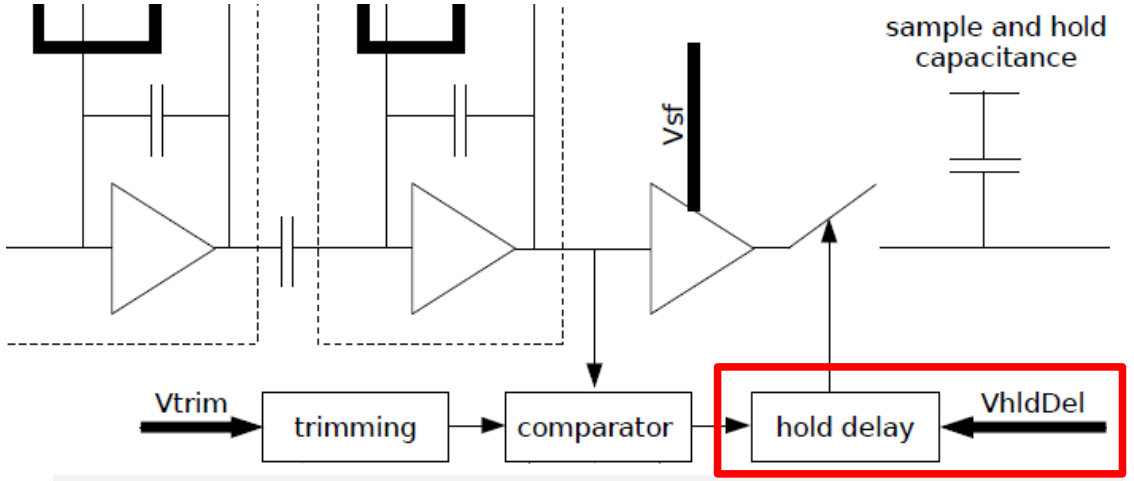
# CalDel and Time walk

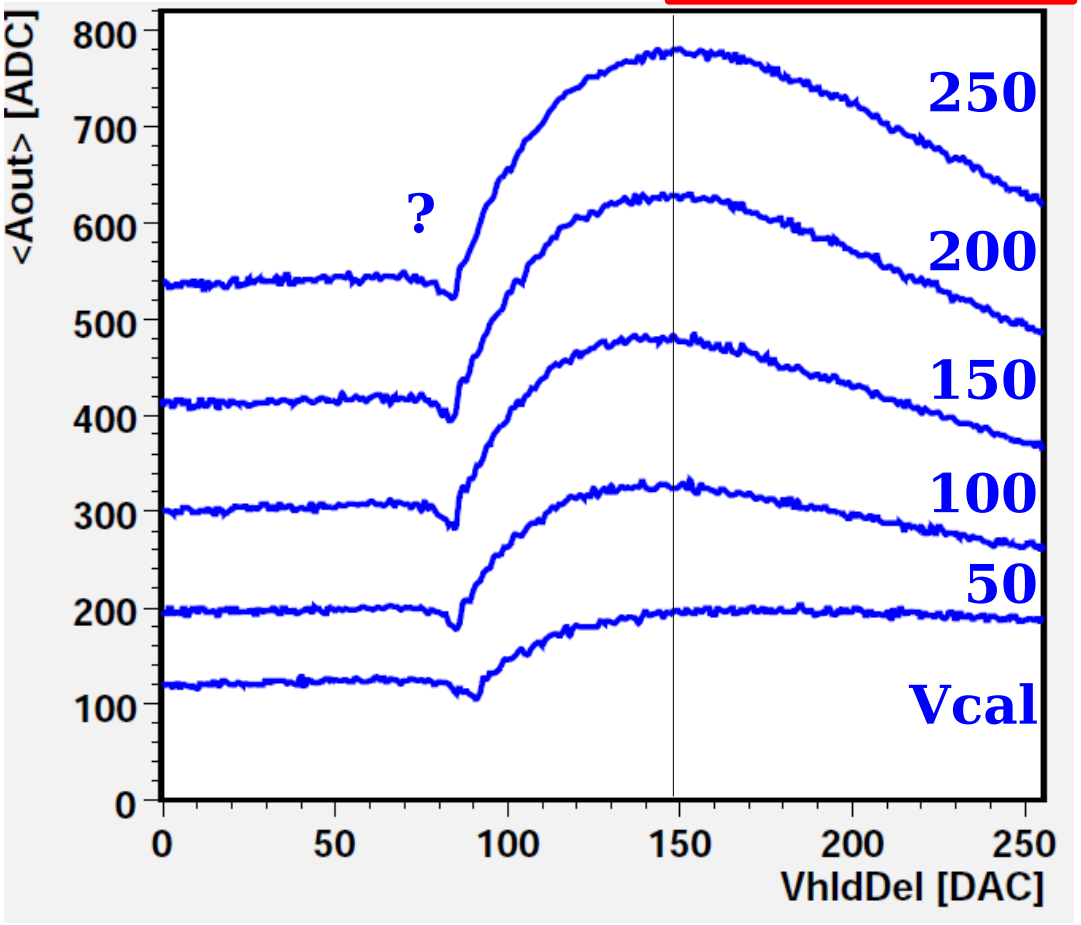



- One pixel.
- Vcal 200 small DAC.
- Moving the threshold shifts the timing:
  - time walk.



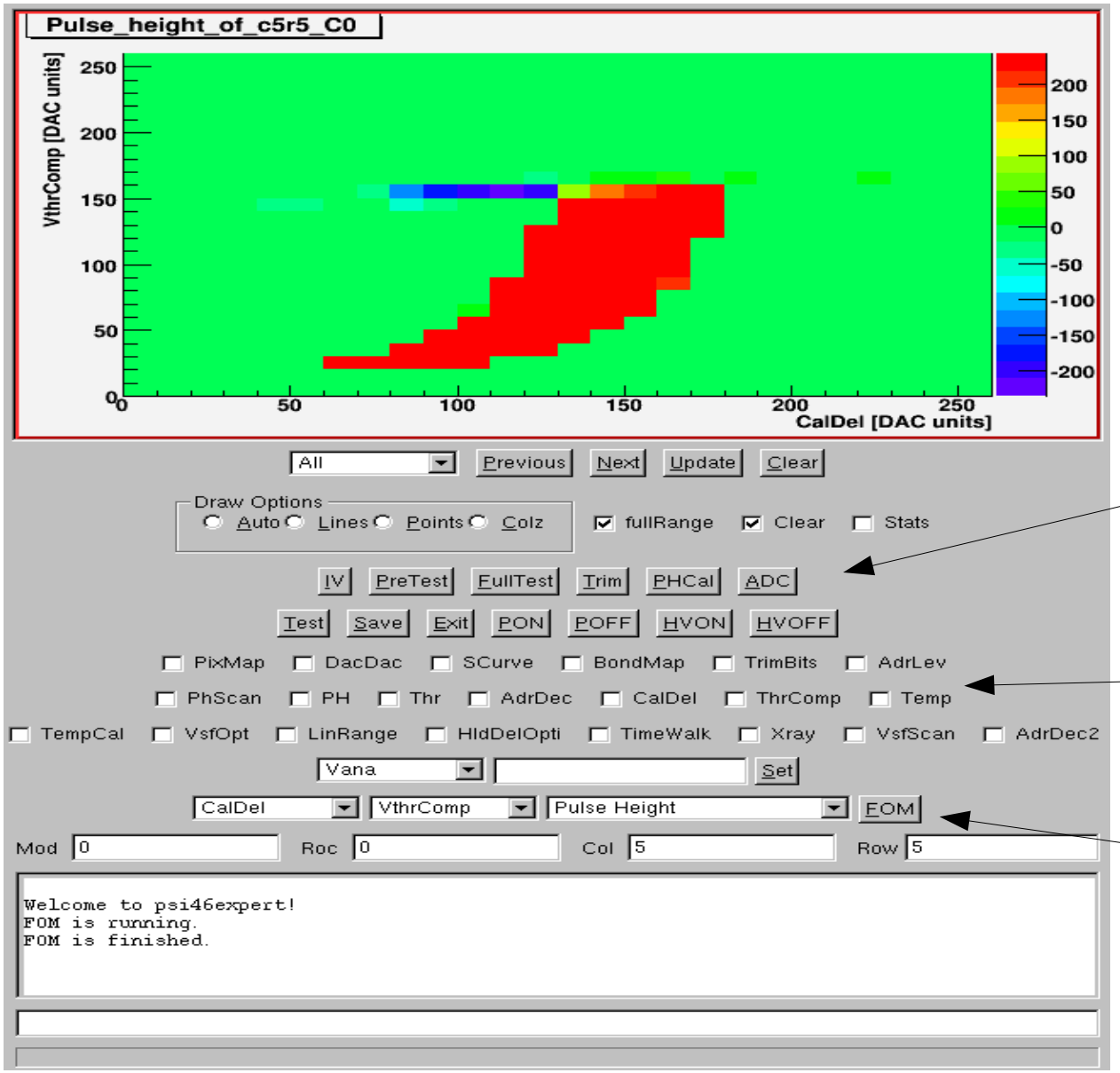
# Sample and hold timing




- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 150 is compromise

# GUI




**Calibration tests**

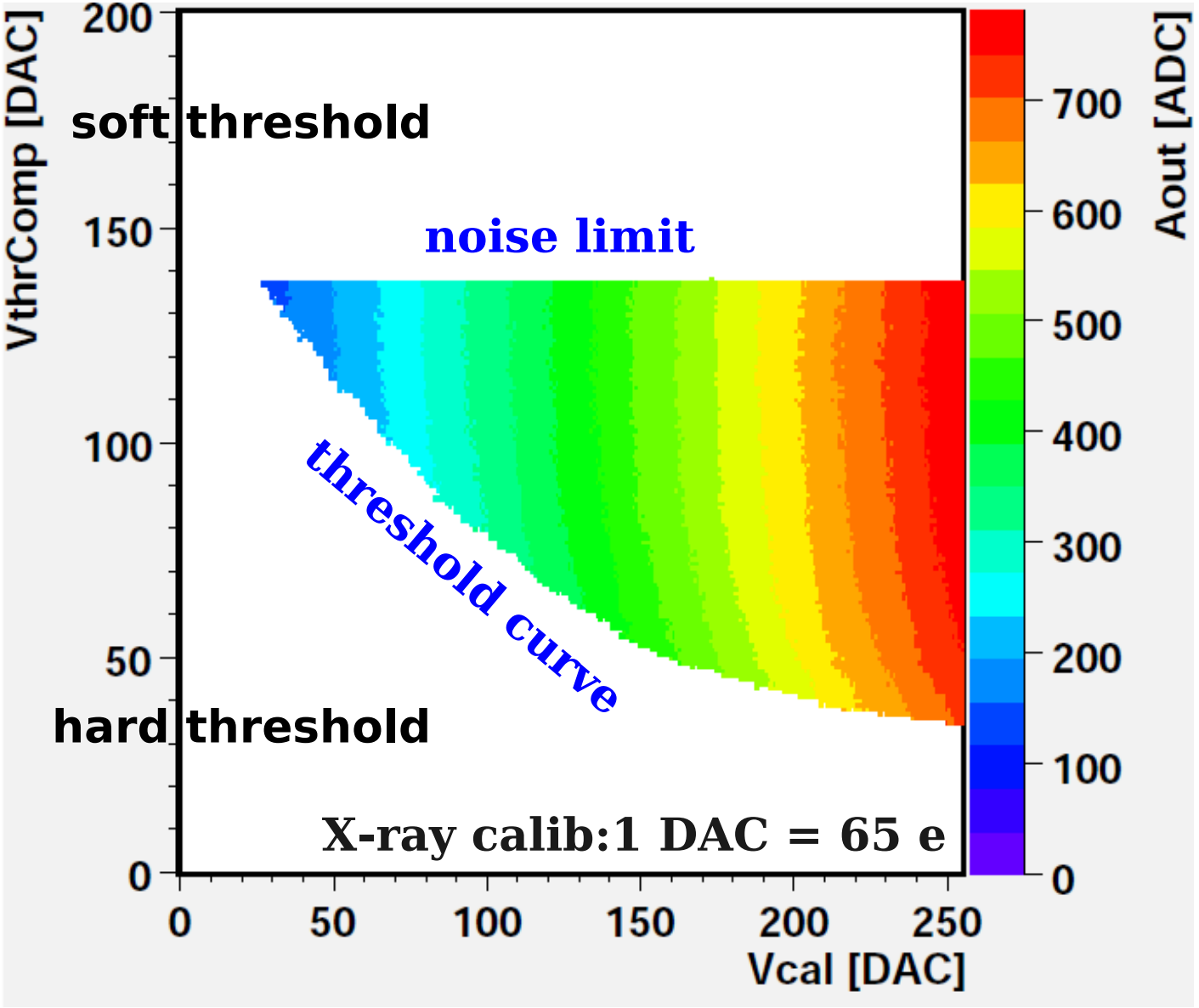
**Individual tests**

**Parameter adjusting**

# Threshold optimization algorithm

- If comparator thresholds are adjusted with global VthrComp only: spread of thresholds in ROC ~300 $e^-$ due to transistor mismatches
- Unify pixel thresholds by 4 trim bits (values from 0 to 15) and scale with Vtrim DAC
- Each trim bit value is set such that Vcal -threshold of the pixel differs least from the selected target threshold in the procedure
- threshold spread reduced to 50(80) $e^-$ after the optimization chip without(with) sensor

# Comparator threshold

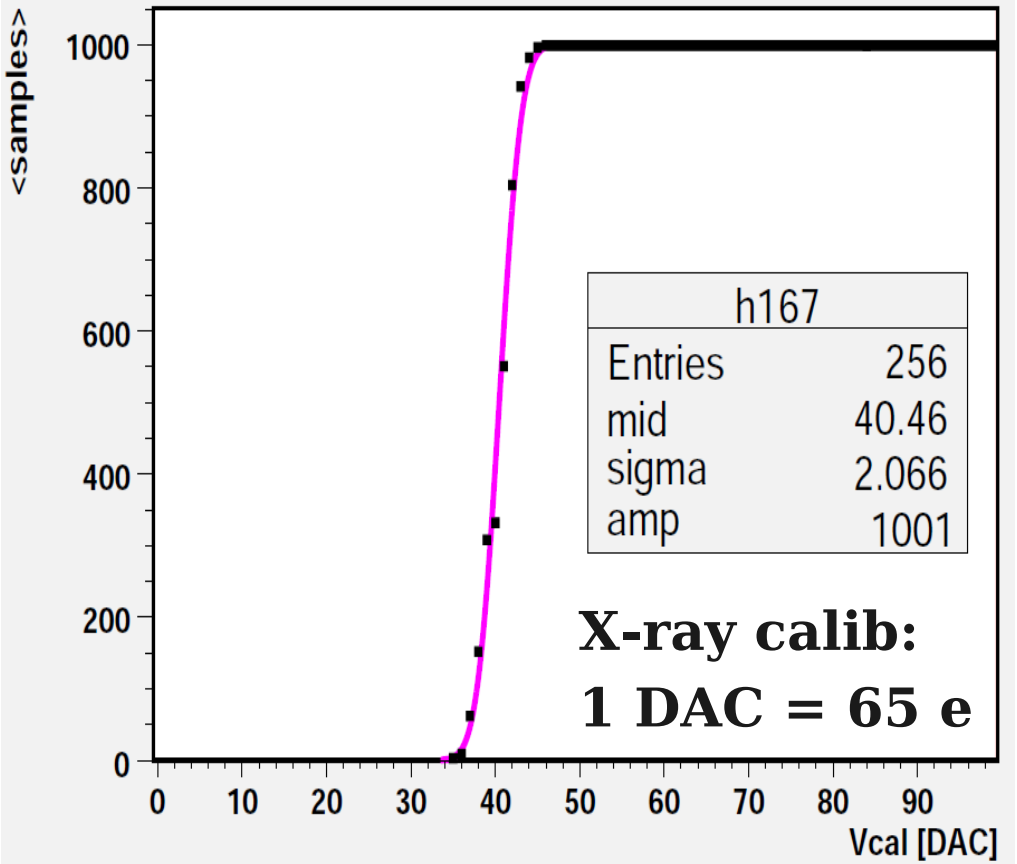



- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

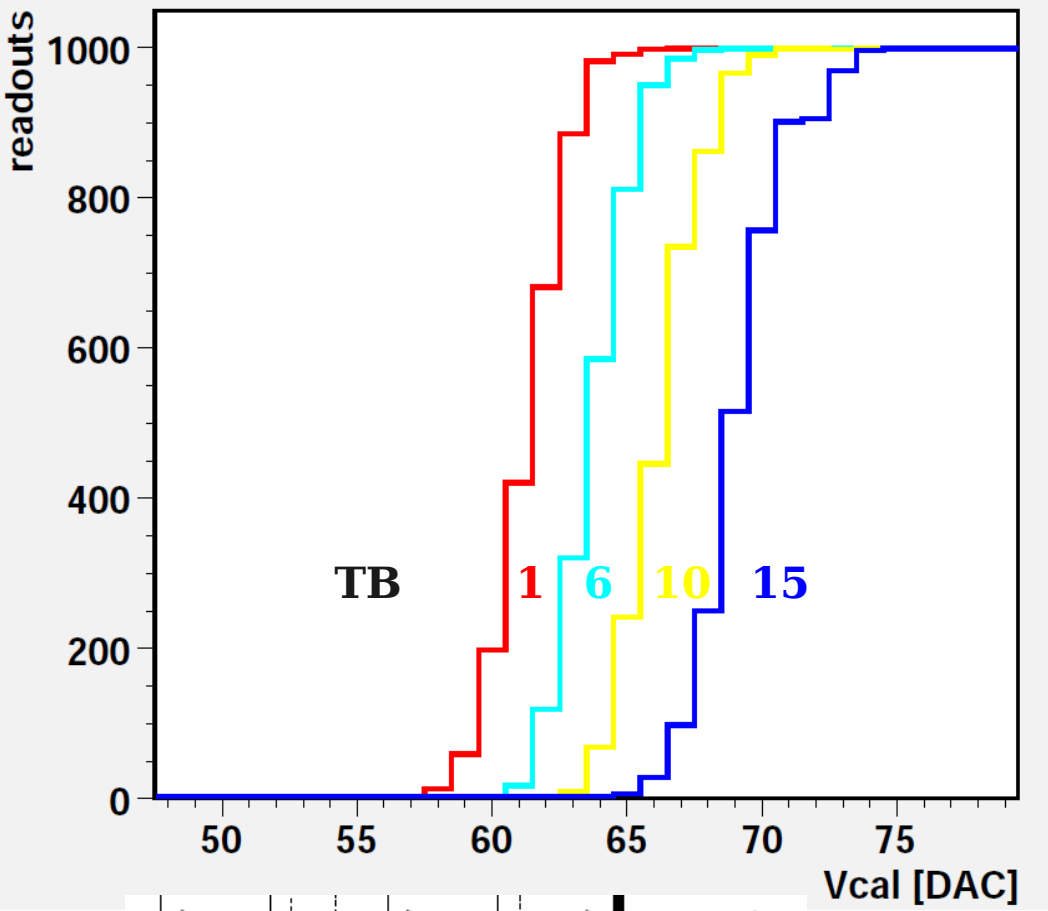
# Threshold curve

## one pixel

### vary test pulse amplitude



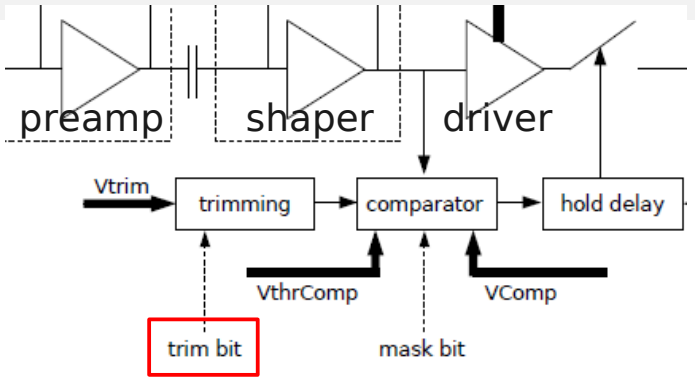

### vary trim bits




**threshold broadened by noise**

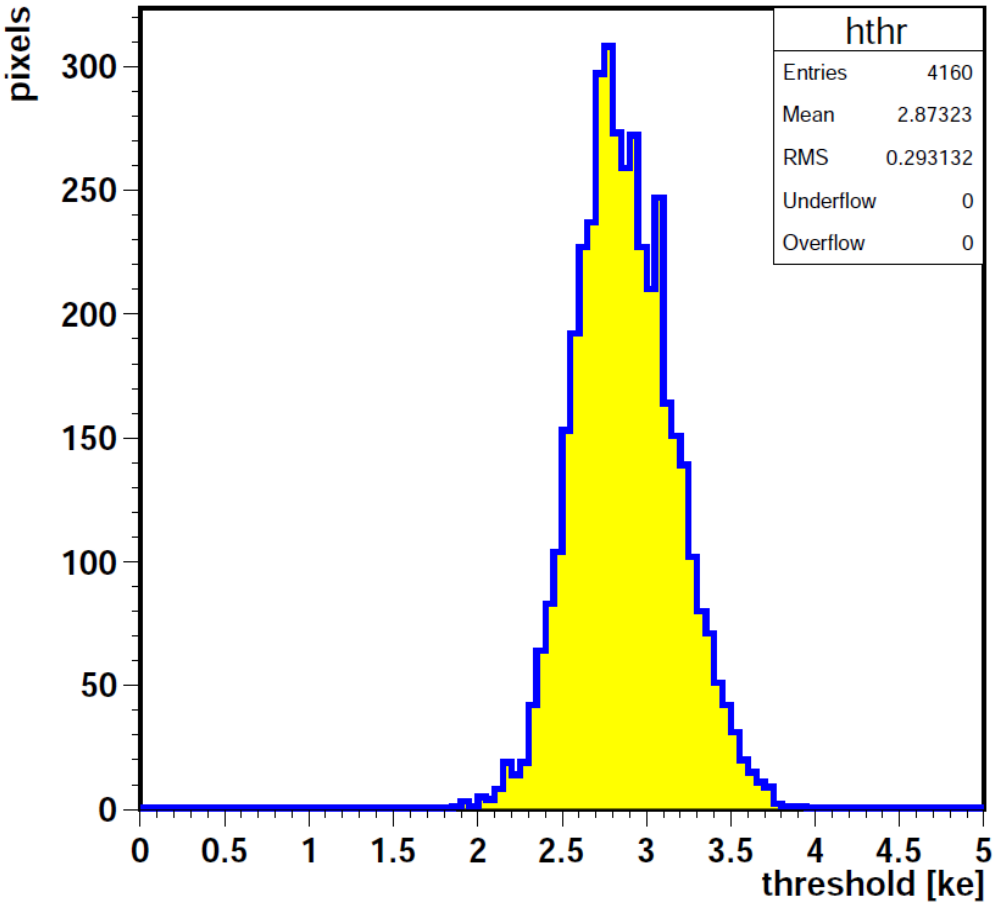
**fit by error function**

**noise: 130 e**

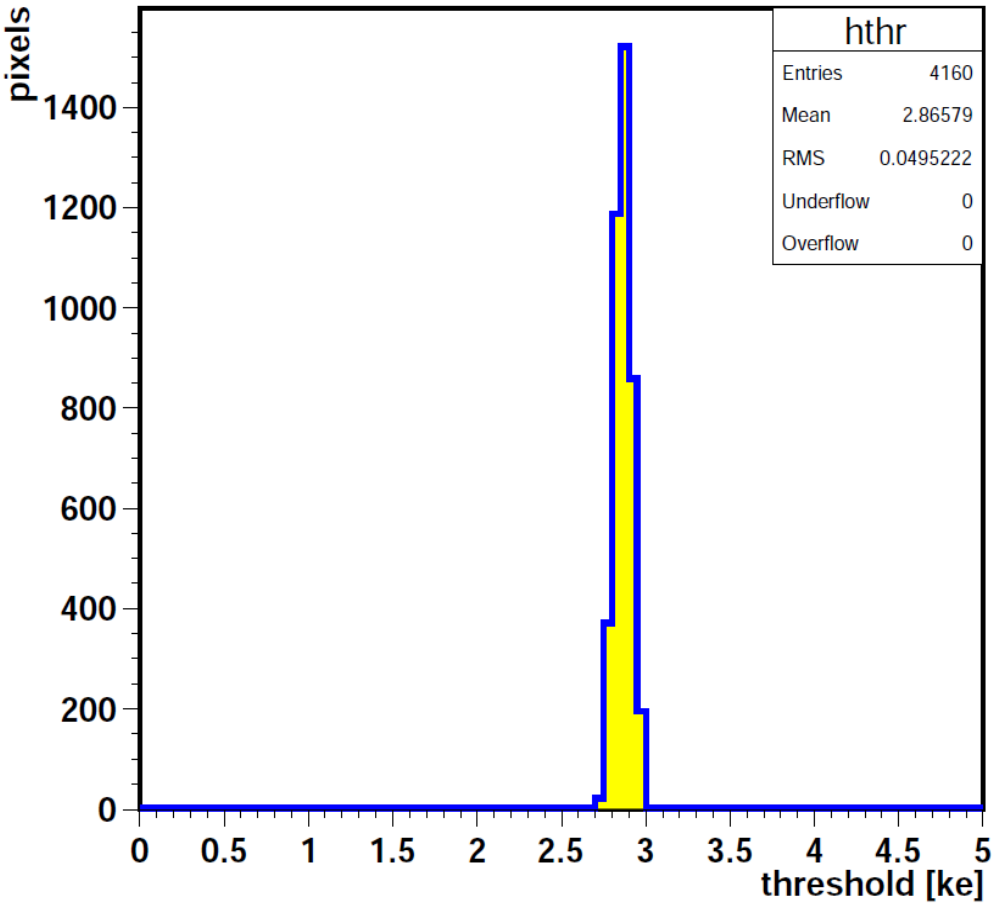


# Threshold variation

**4160 pixels / cip**



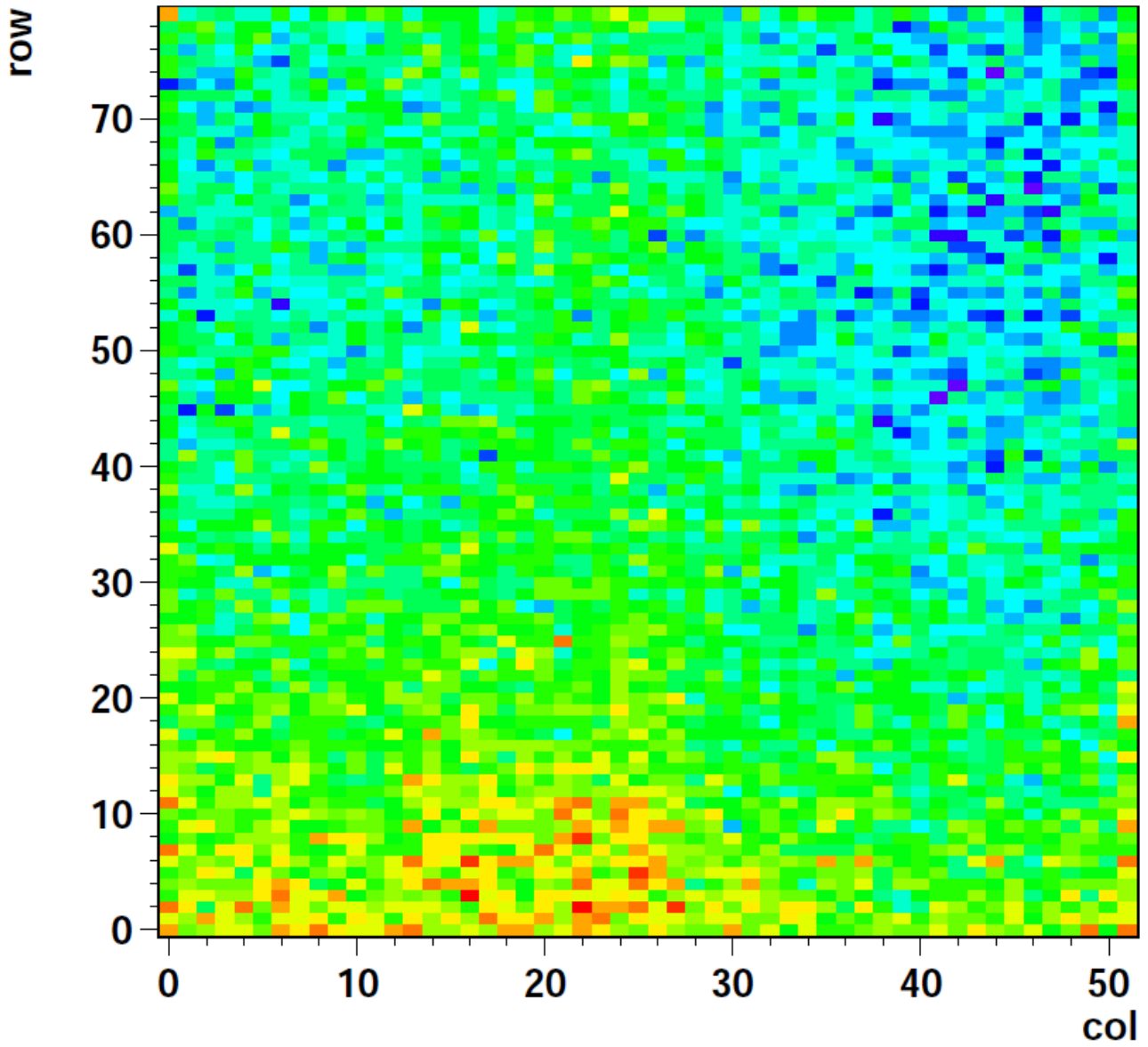

**the same chip, trimmed:**




**CMS transistor variations: threshold spread 290 e**

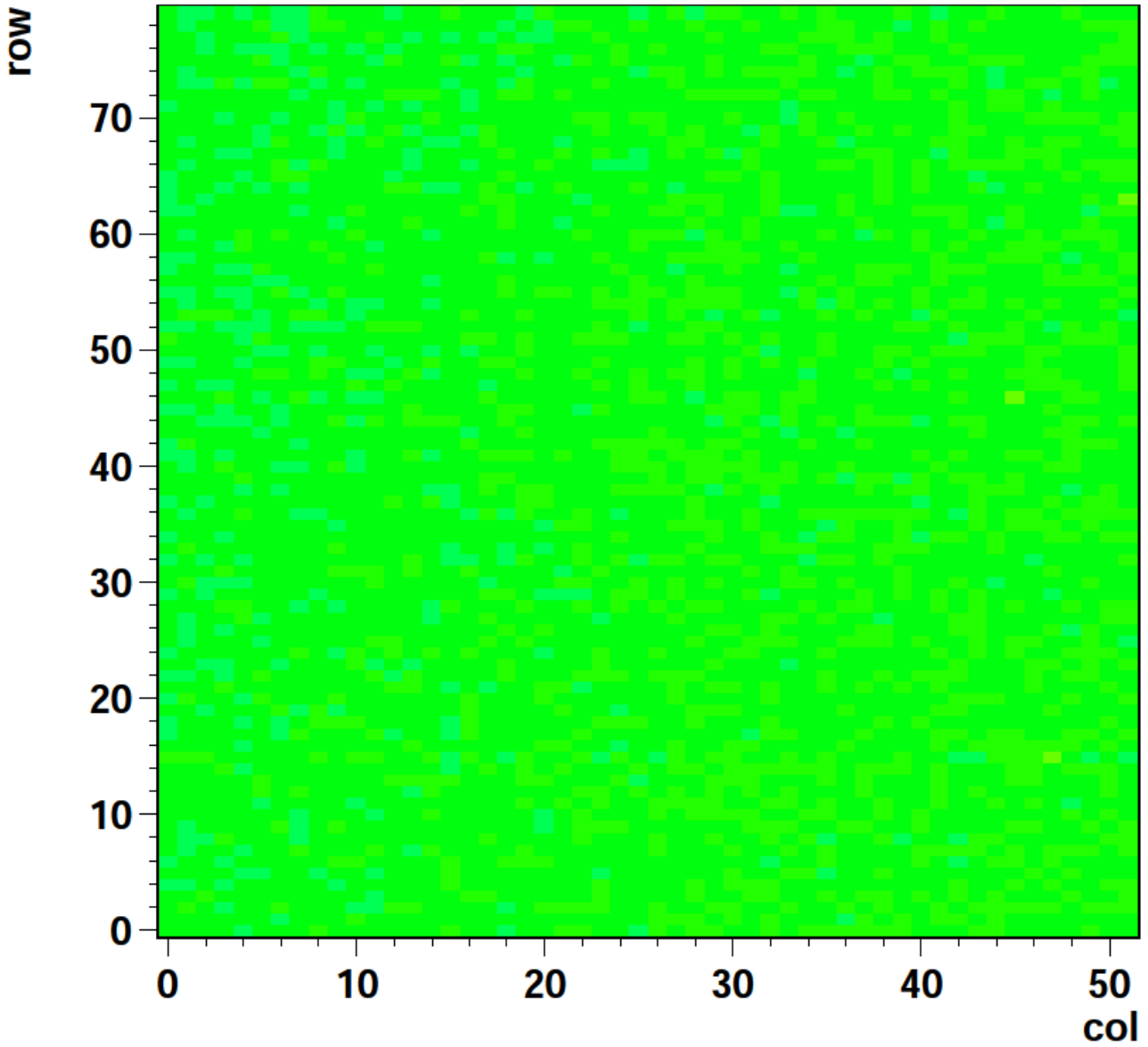
**4-bit DAC trimming: threshold spread 50 e**

# Threshold variation untrimmed




- Vertical scale – threshold in ke
- Chip 0 (no sensor)
- VthrComp 124
- 10% spread

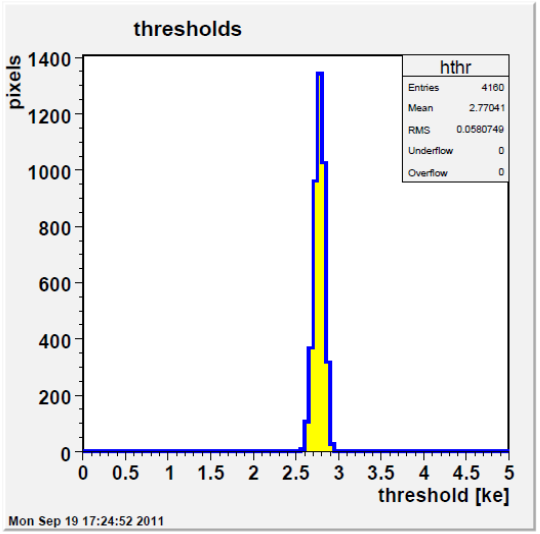
# Threshold variation trimmed

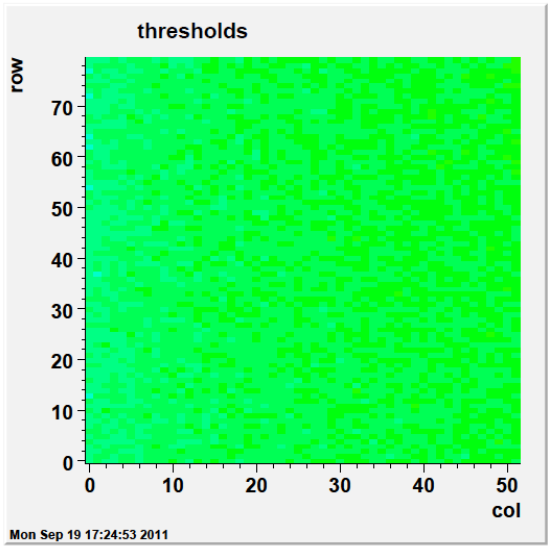



- Chip 0 (no sensor)
- VthrComp 112
- Vtrim 104
- 4160 TrimBits set.
- time: 3 min / chip
- 1.7% spread
- 50 e threshold variation!

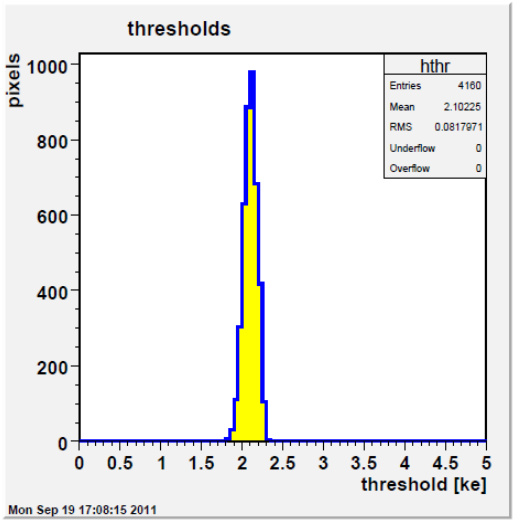
# Towards the minimum TrimVcal

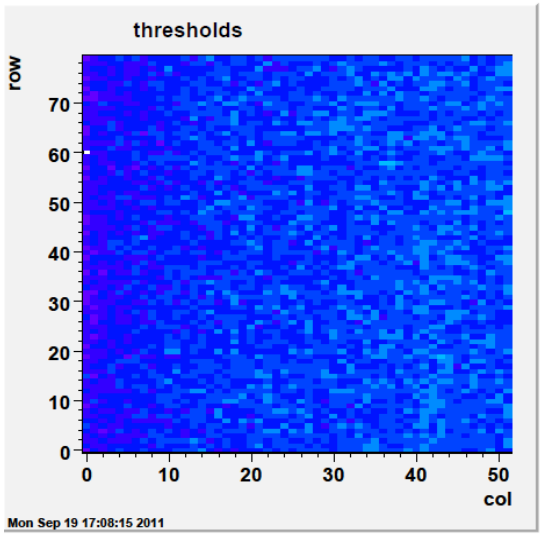
## TrimVcal=40



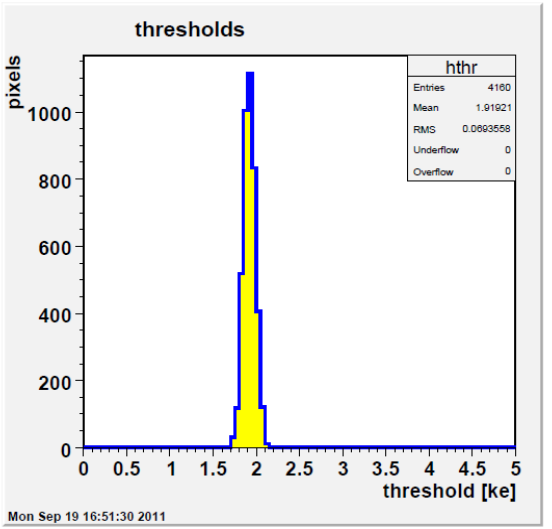



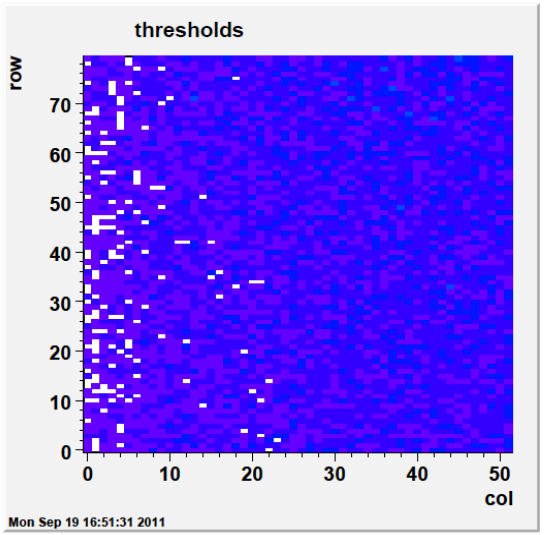

## TrimVcal=32




## TrimVcal=28



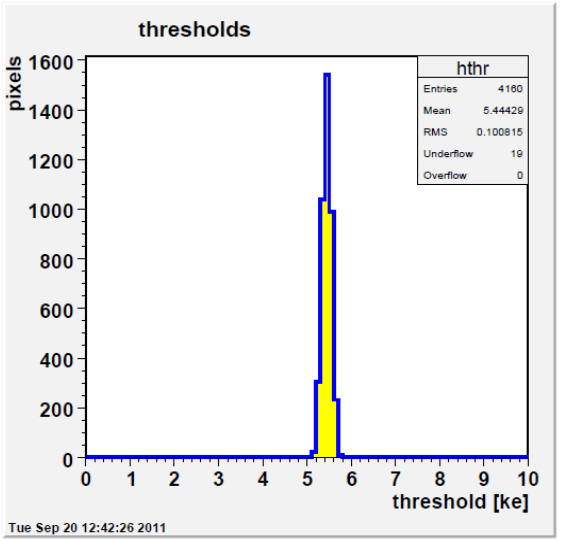



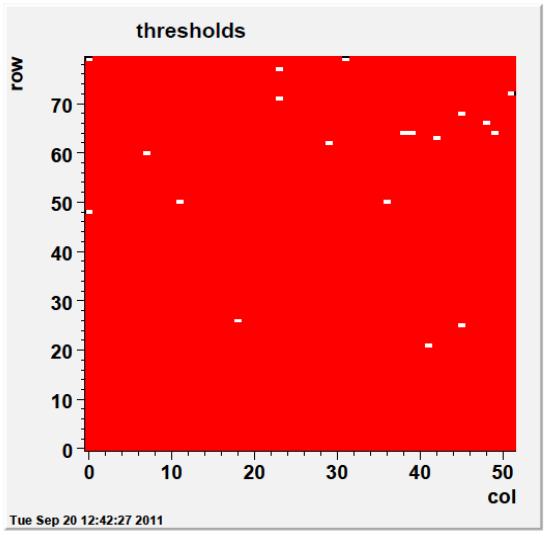

**Use as low as possible target Vcal: good charge sharing, good for radiated chip with low charges.**

**Chip2 (no sensor)**

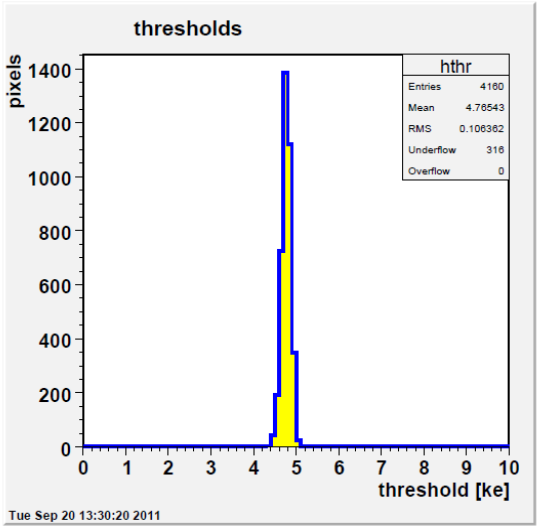
# Tests with sensor

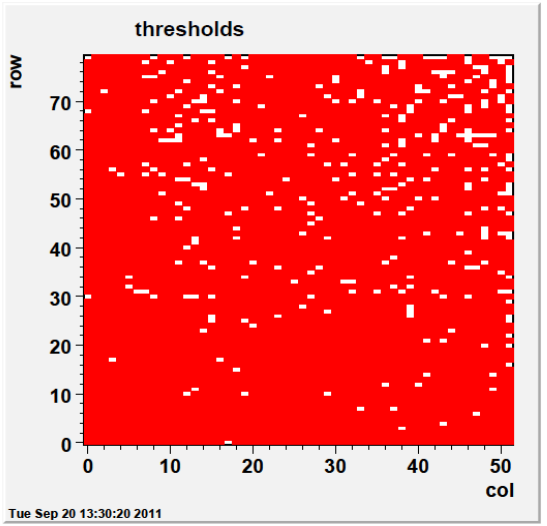
## TrimVcal=80



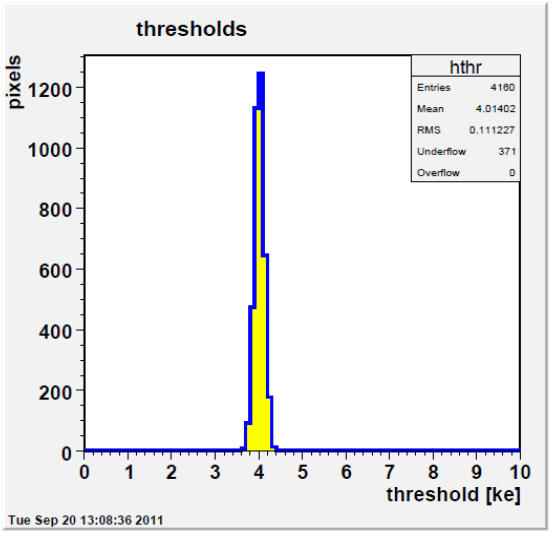



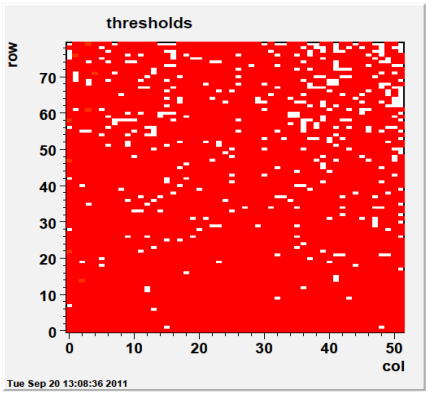

## TrimVcal=70

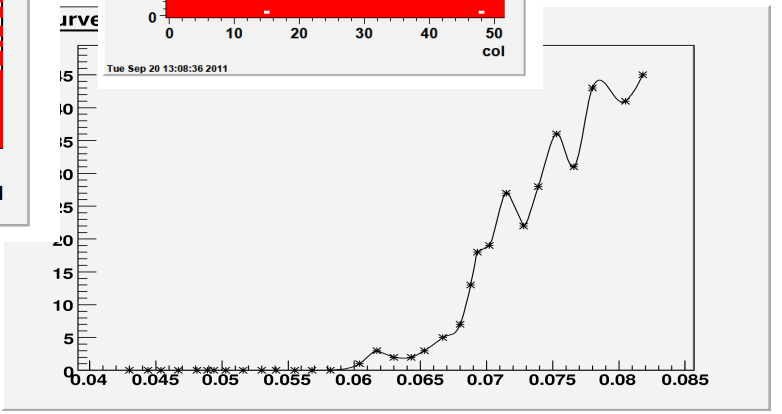



## TrimVcal=60



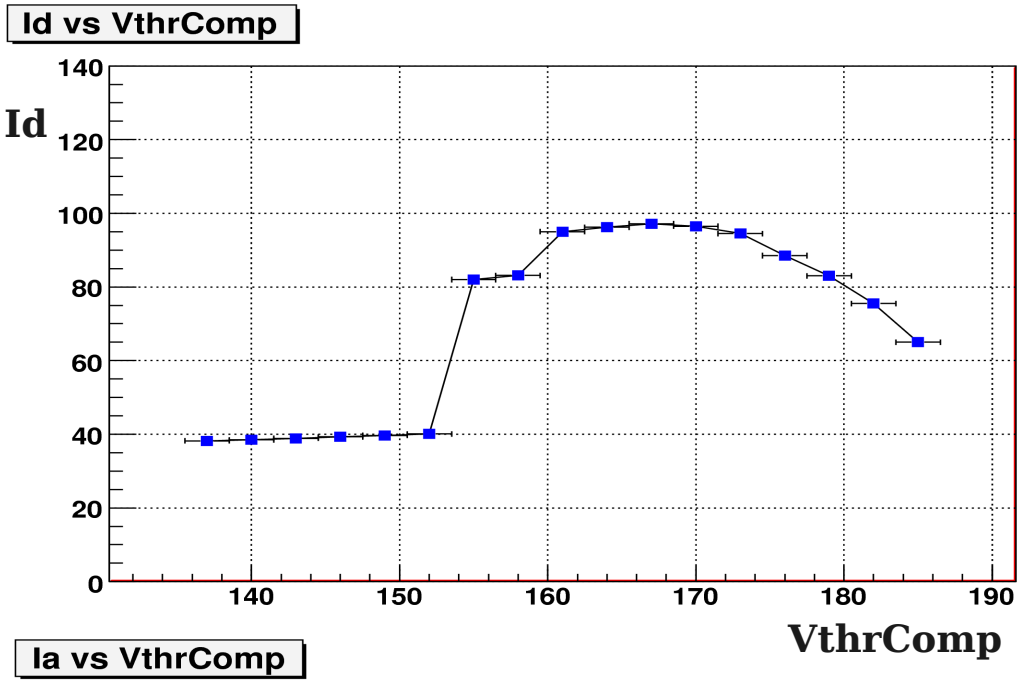



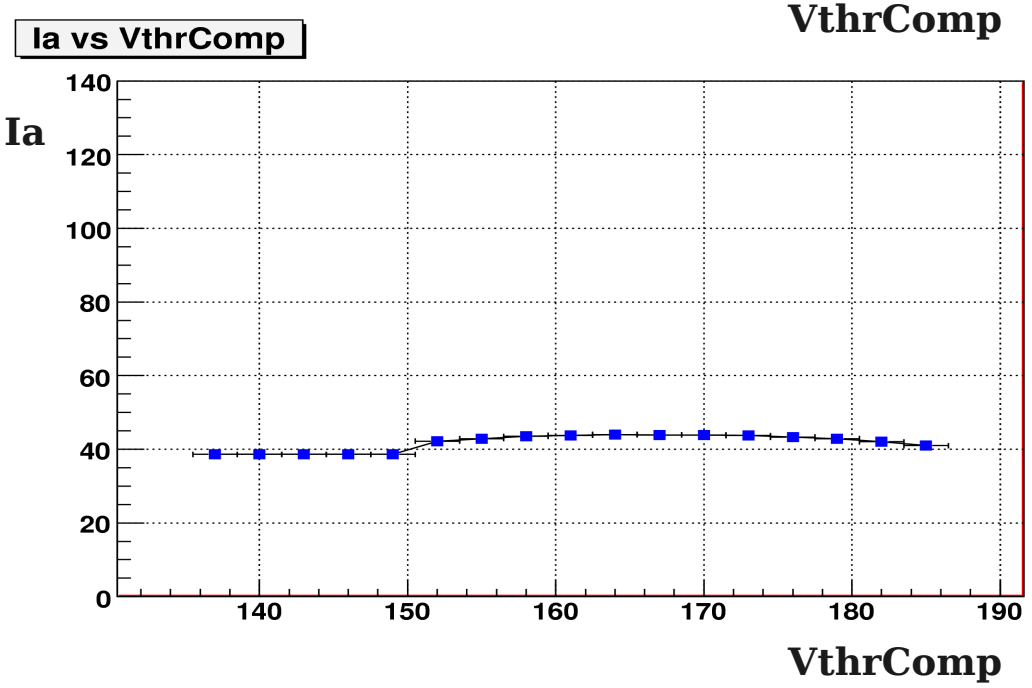
**Underflows: bad fit of SCurves**

**<u>Chip6</u> (with sensor)**

# Threshold Scan and Power



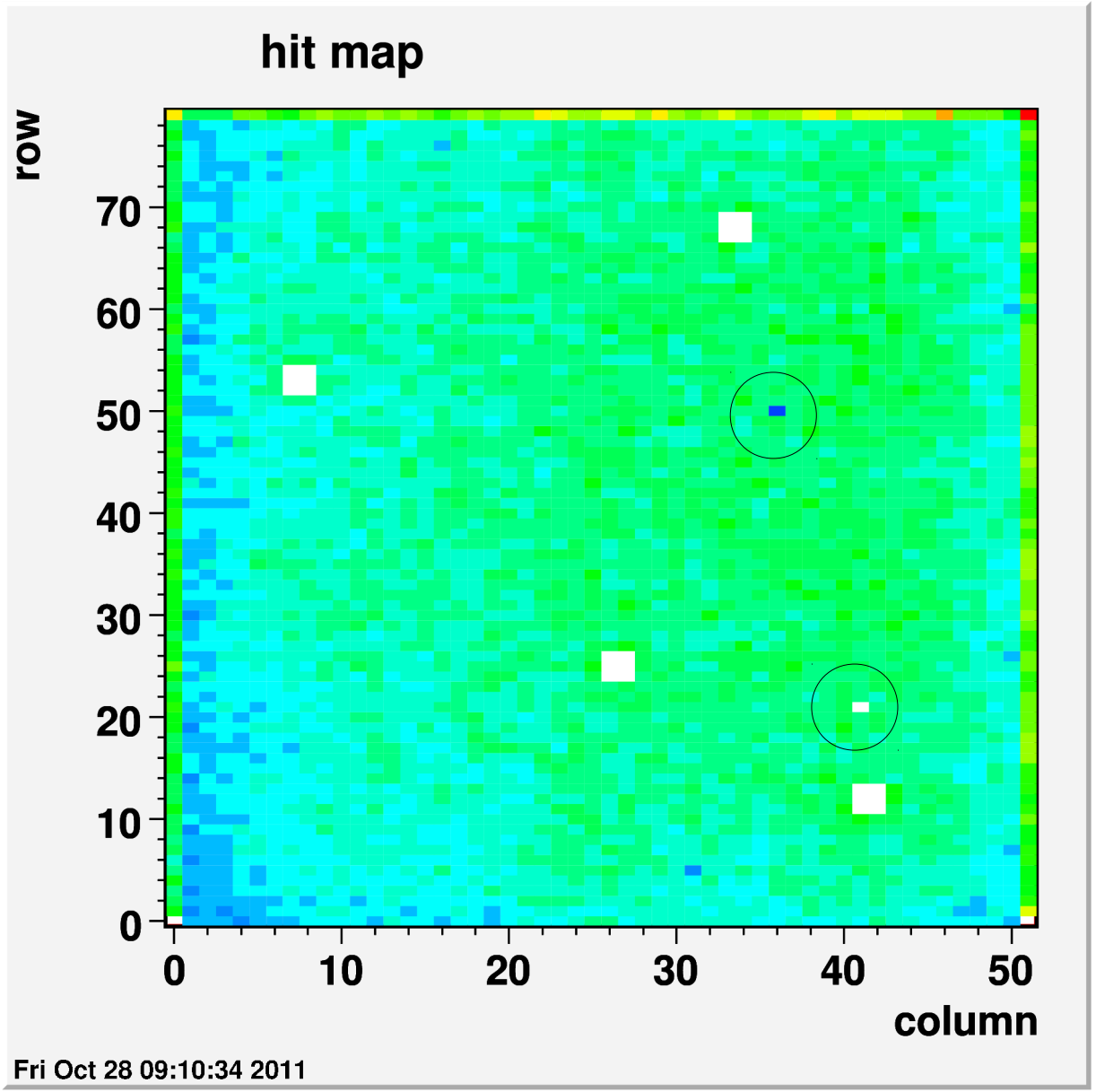

- Chip 2 (no sensor)
- Id (mA) vs VthrComp
- Threshold into noise
- Chip consumes 2.5 times more power at low threshold (high VthrComp)




- Chip 2 (no sensor)
- Ia (mA) vs VthrComp
- Small effect at low threshold

- The same trend for Chip 6 (sensor)

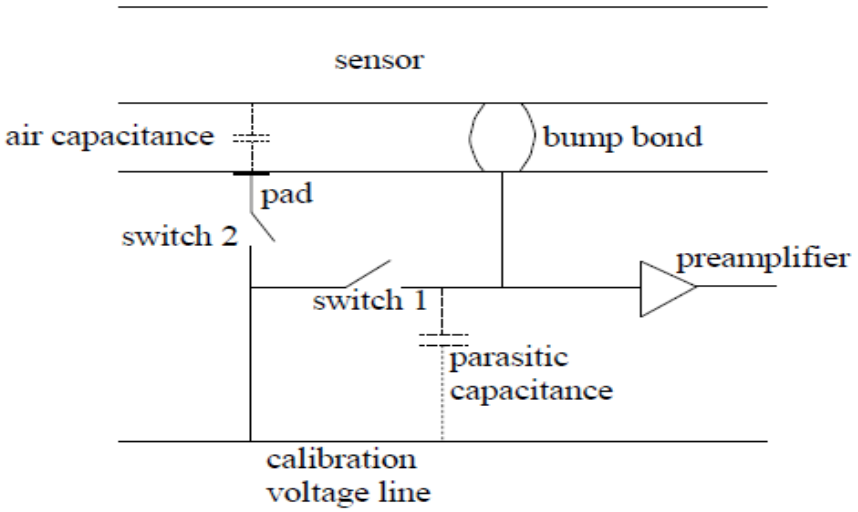
# Test beam hit map



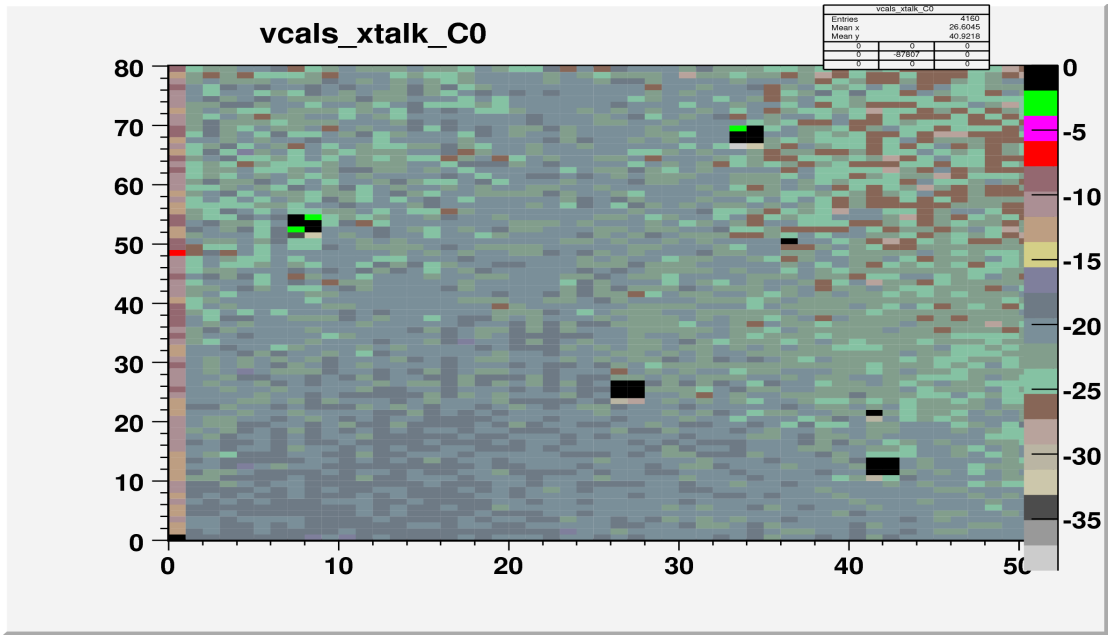

- 2 GeV e+ test beam
- Chip 6 (sensor)
- 2 dead pixels
- 4 dead regions
- Use 'psi46expert' to test bump bonding

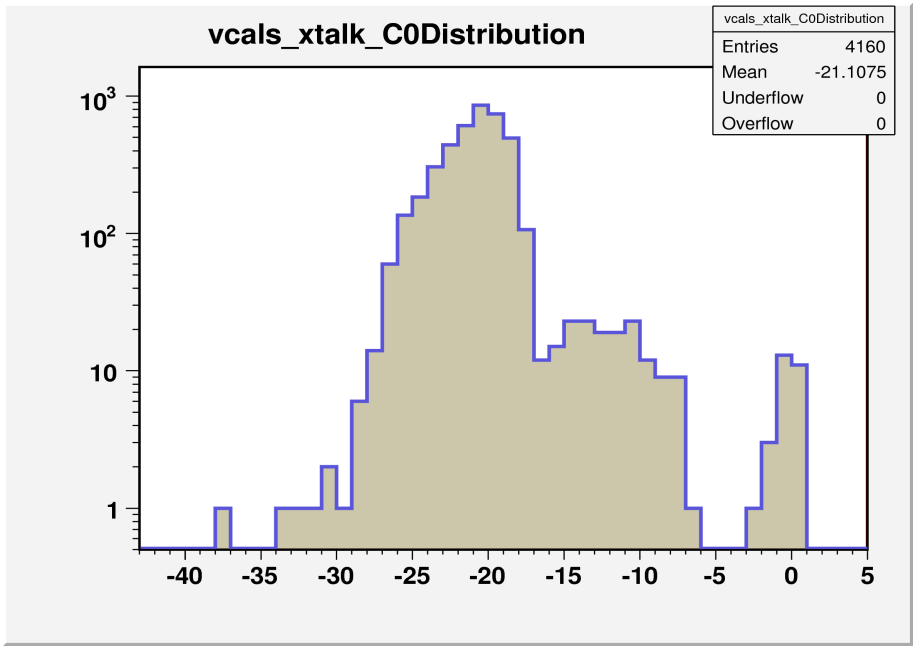
# Bump Bonding Test Procedure

- Vcal to switch 2 induces a signal in sensor. If bump bond (bb) is present it is seen by preamplifier: missing bb can be identified
- Problem: cross-talk via a parasitic coupling between the calibration voltage line and preamplifier can fake a signal even without bb
- Determine Vcal_Thr2 for the signal injection through the sensor
- Measure Vcal_Thr1  for the parasitic cross-talk (with both switches open)
- |Vcal_Thr1 – Vcal_Thr2| < 5 DAC units → defect bump bonding



# Bump Bonding Test Results

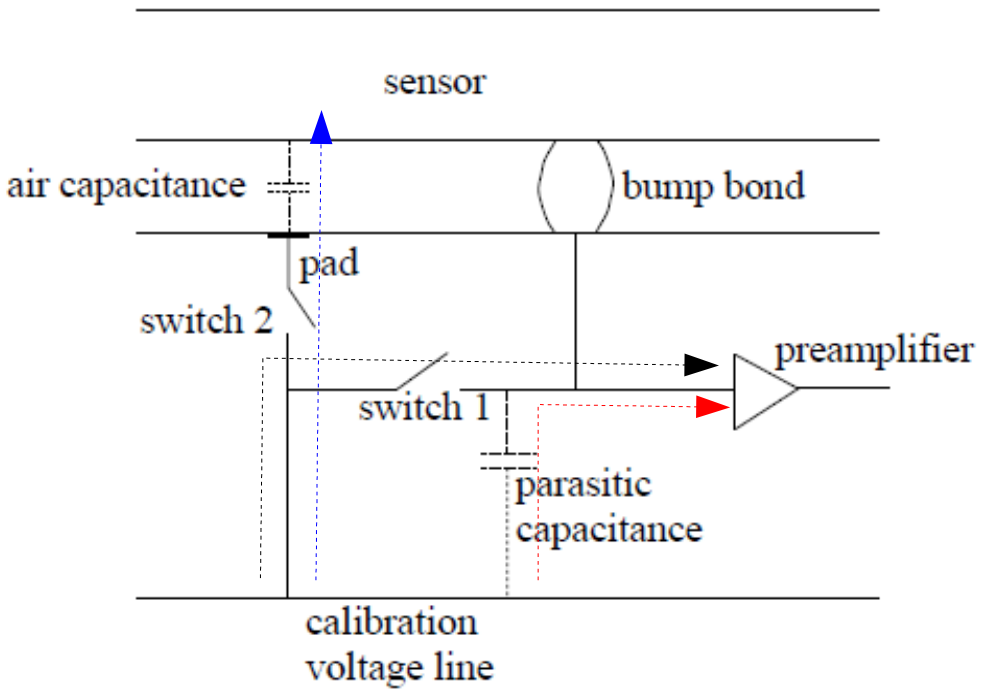



**Δ Threshold**

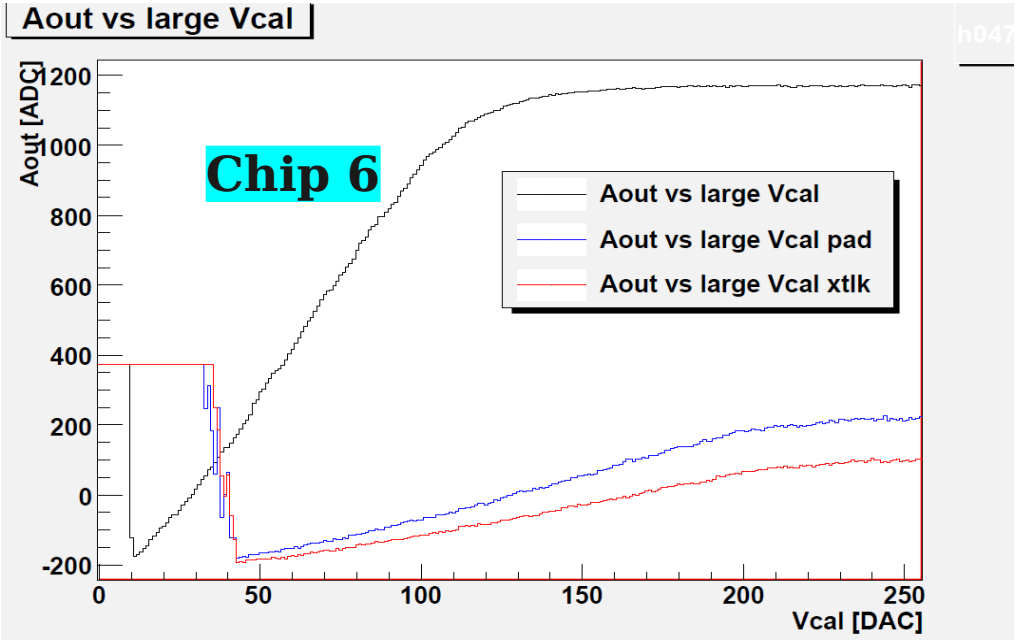
- Threshold difference: expected defects from beam test are correctly identified by 'psi46expert'
- Peak at Δ Threshold ~ -20 → good bump bonds. Peak at Δ Threshold ~ 0 → bad bump bonds

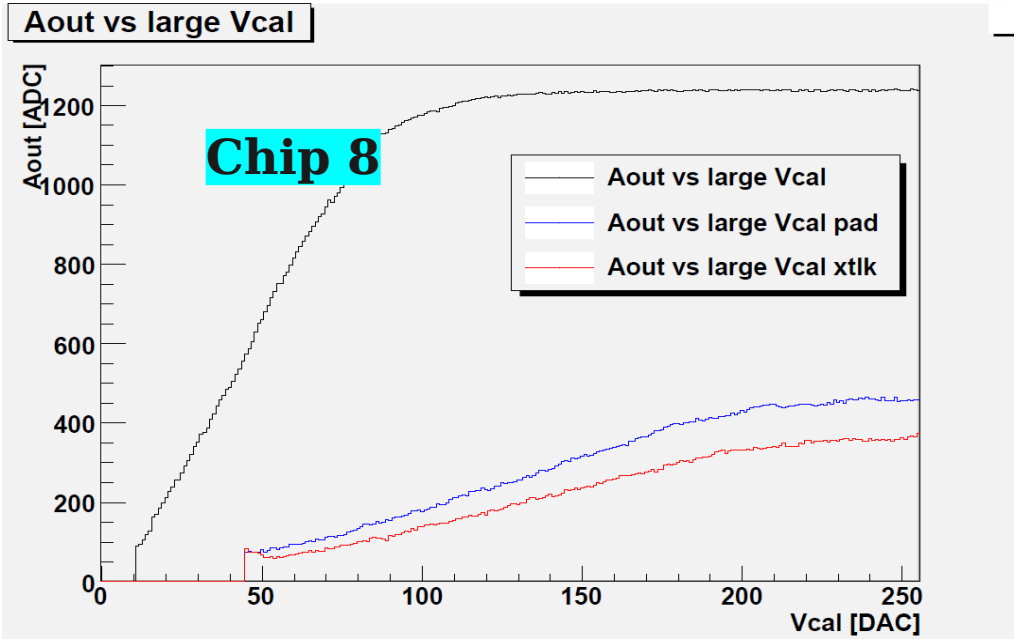
# Arm Pad, Xtalk




- Three ways to inject charge: Standard (used so far), via 'pad' and through 'Xtalk'
- Different signals can be used for bump bonding test of modules, cross calibration of ROCs and some other purposes ?

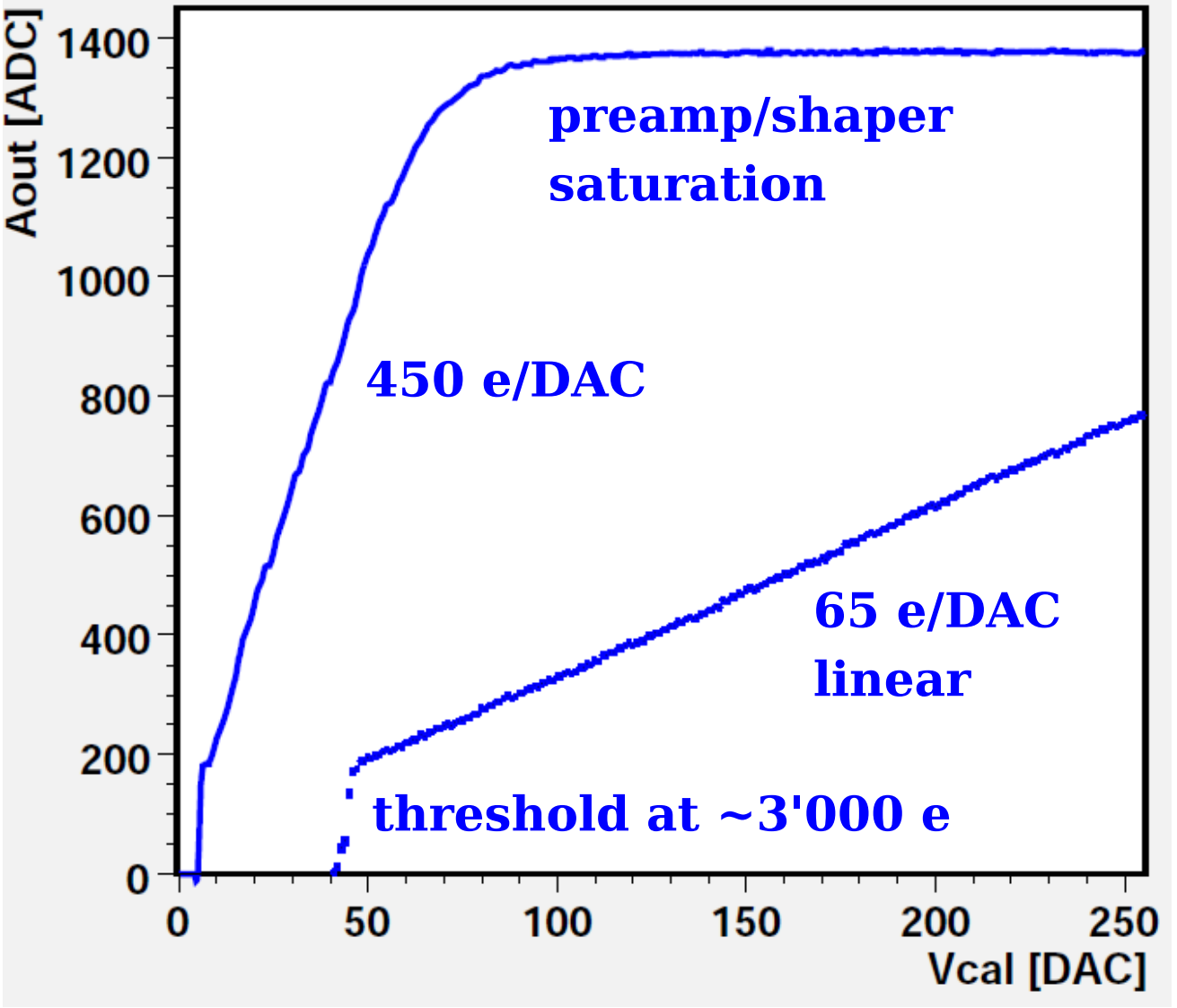
# Arm Results



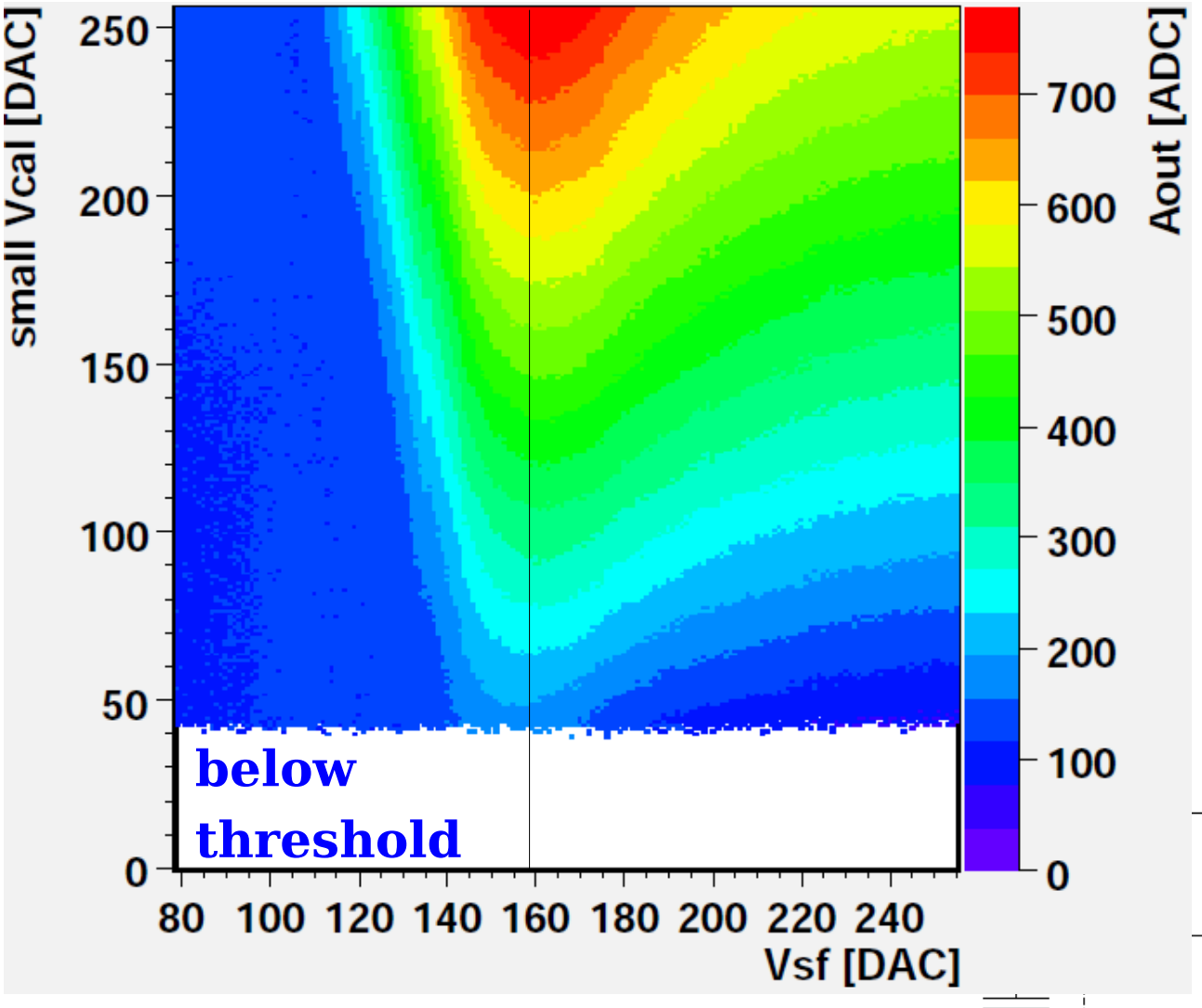

- Use three different capacitances to inject charge: **direct**, **via sensor**, and **crosstalk**:
  - $Q = C_x \cdot Vcal$
- One pixel activated.
- Draw PH [ADC] vs calibrate amplitude for large Vcal (450 e/DAC)
- Use sensor type ROCs
- Chips 6, 8 show similar behaviour but PHs are different (different config. parameters for analog gain and offset)
- Blue and Red curves start to saturate later compare to black - ?

# gain and linear range

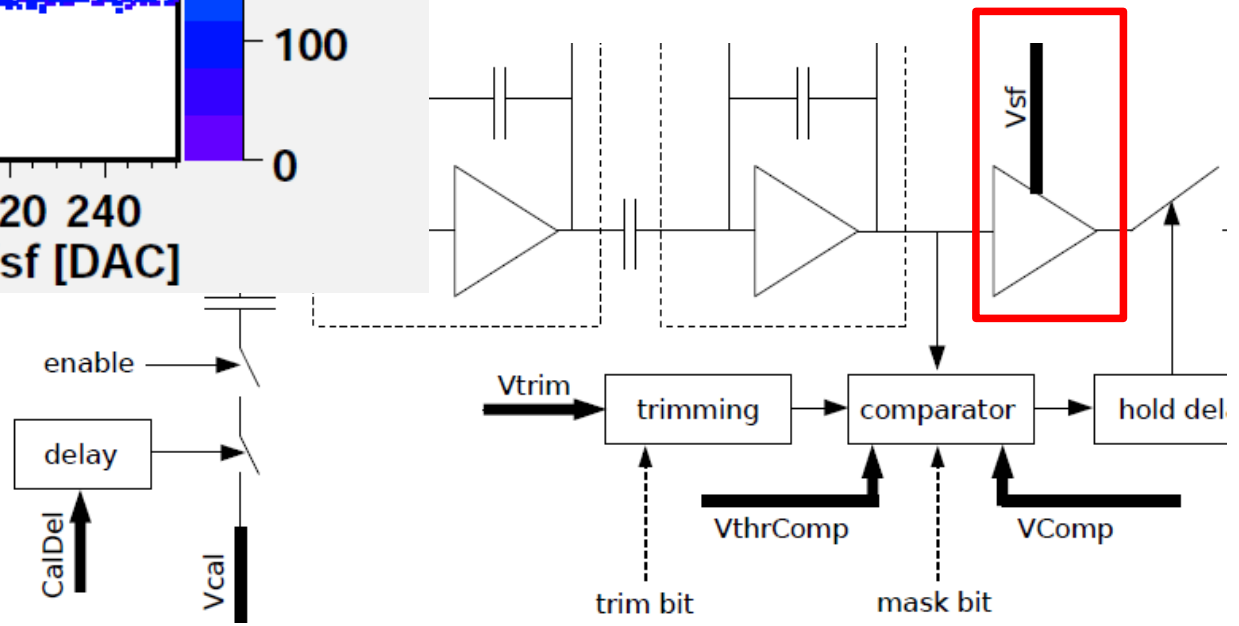



- One pixel.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.
- Linearity for small pulses important for spatial resolution using charge sharing.
- Saturation around 36'000 e (~1.6 MIP).

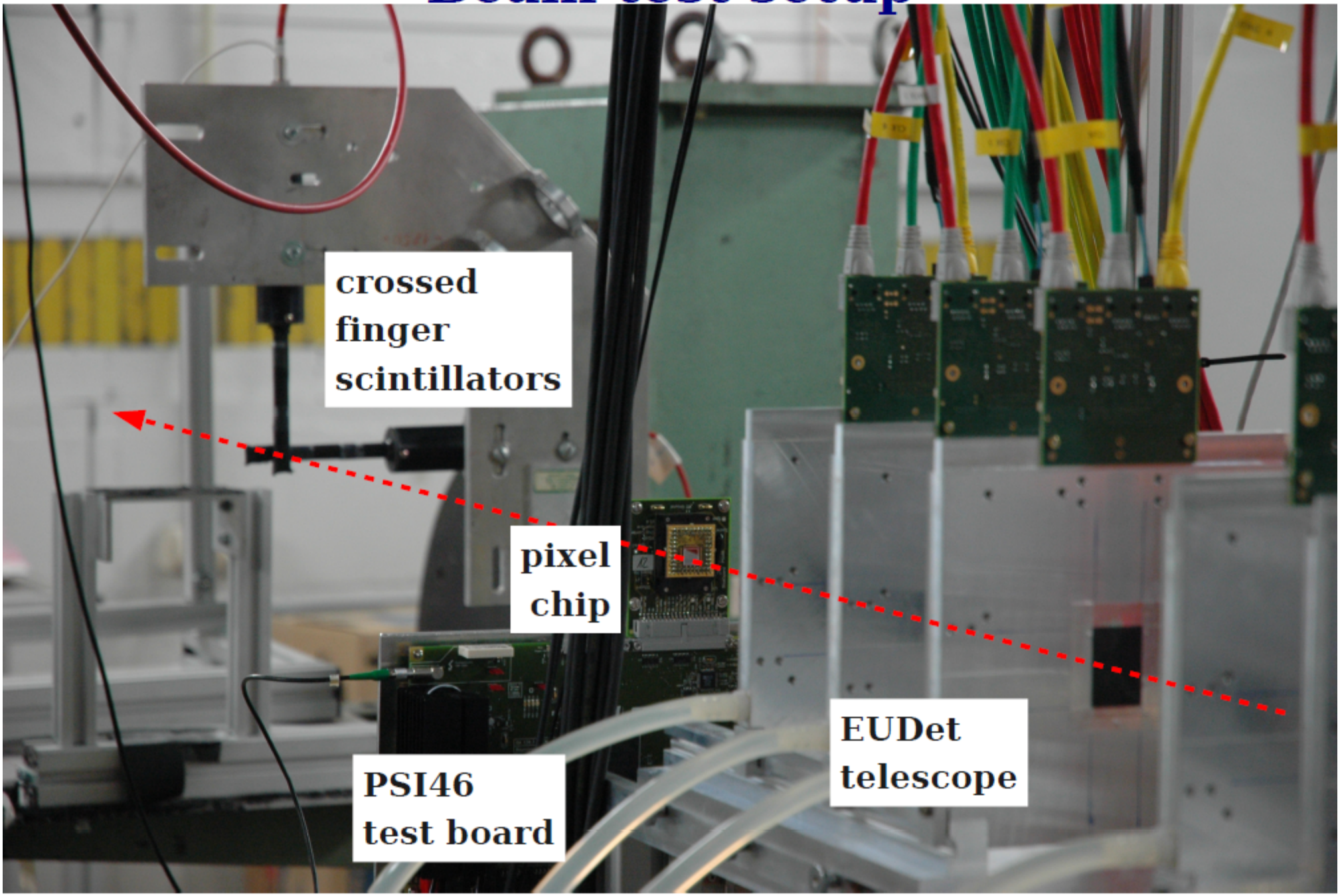
# Linear range vs Vsf



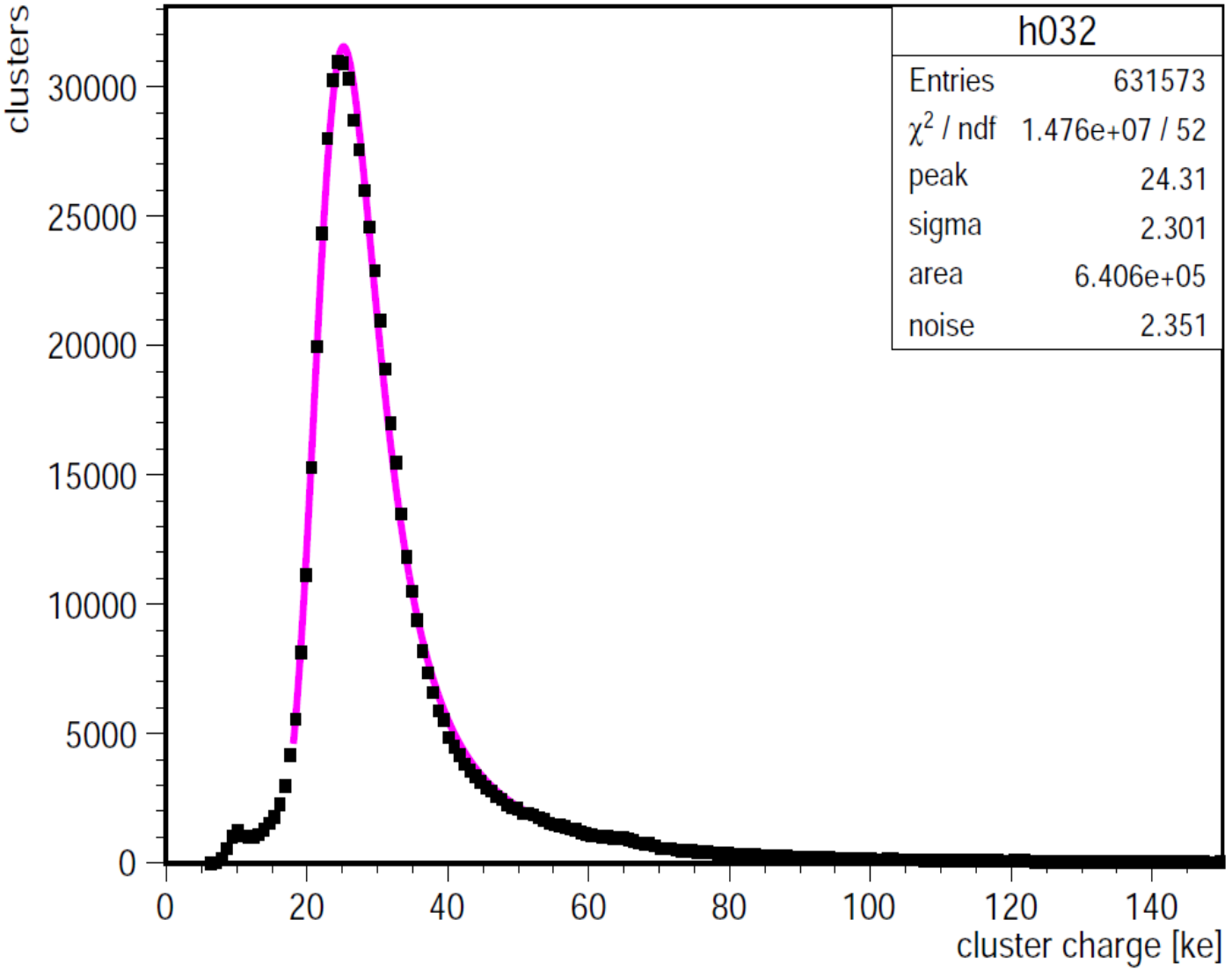

- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Best linearity in valley.



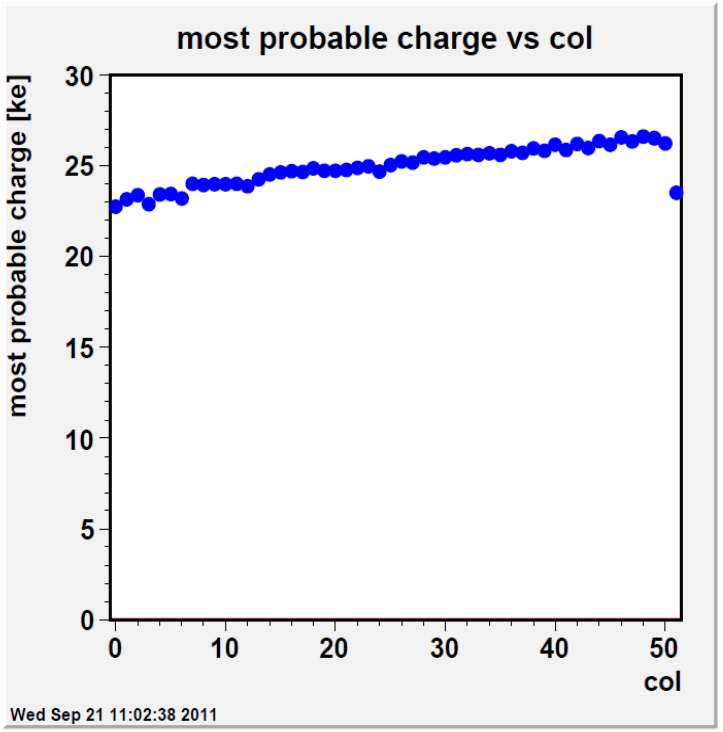
# Beam test setup

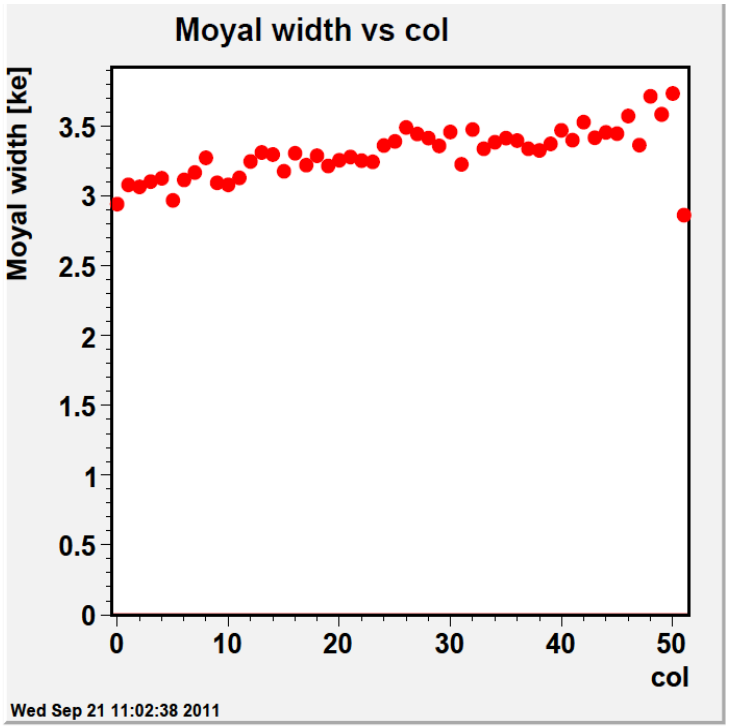


# Pixel detector in DESY test beam




- 2 GeV $e^+$ beam.
- Landau ⊗ Gauss:
  - Fit not perfect:
  - Peak position and width OK for 285 um silicon,
  - noise too large.
- Small peak at small pulse height:
  - Wrong timing due to missing synchronization between clock and beam.



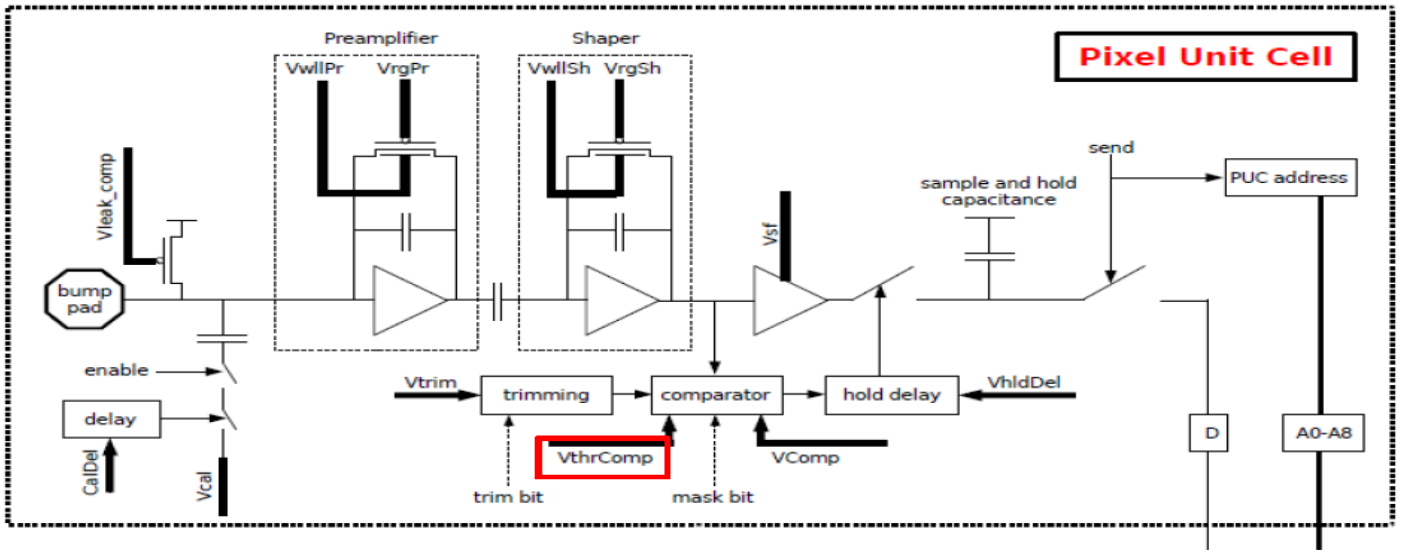




# Cluster charge

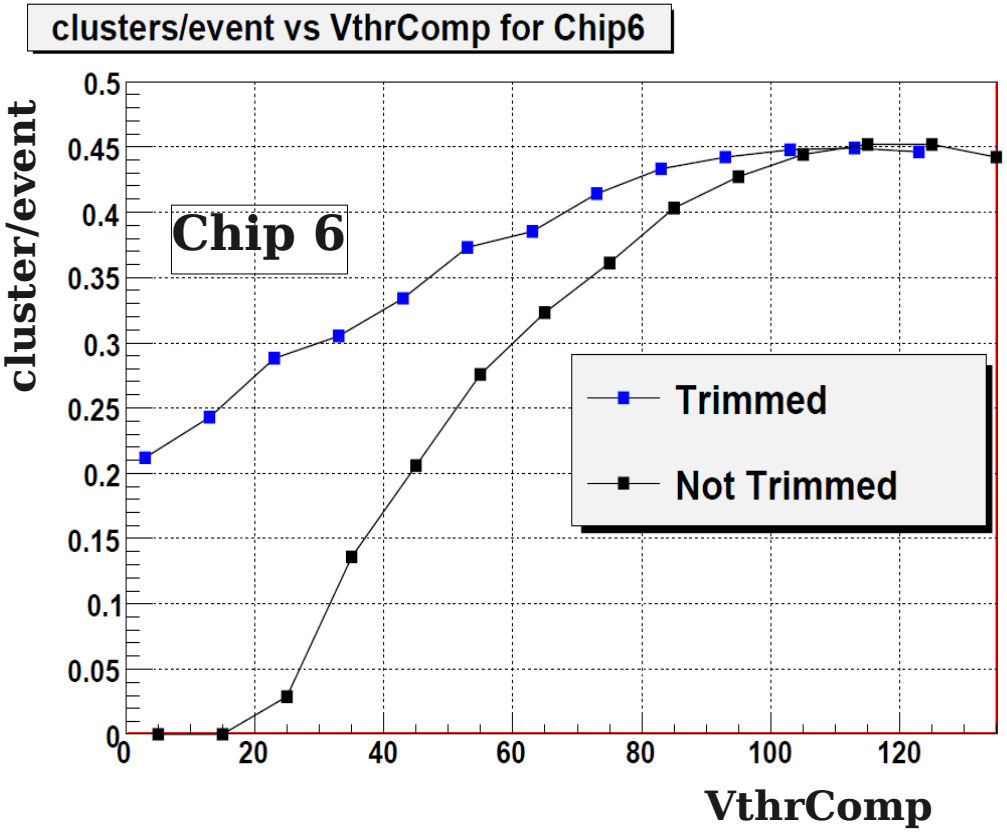
- 2 GeV e+ beam test
- No magnetic field
- Test pulse gain calibration applied
- Chip 8, all pixels
- Moyal fit to each column
- Expect ~25 ke from 285 µm silicon
- Observe ~8% gain variation across chip8:
  - Test pulse (calibration) problem?
  - Check with X-ray source?

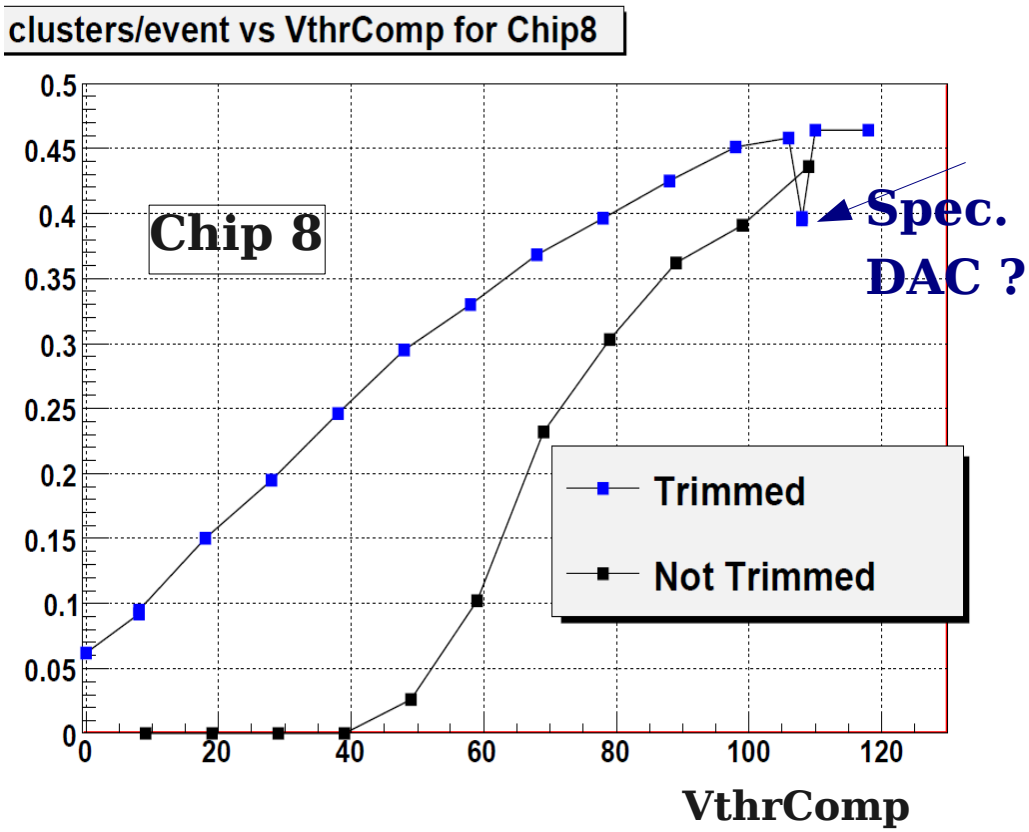
# Threshold Scan Procedure

- DESY 2 test beam: 2 GeV e+, 5 kHz scintillator trigger, Vbias -90 V
- Chips 6, 8 (sensor), calibrated, trimmed, optimal DAC parameters
- 50 sec runs, 0 – 140 k clusters per run
- Change VthrComp from lowest to optimal DAC units. Large DAC = soft threshold



# Threshold scan in the test beam

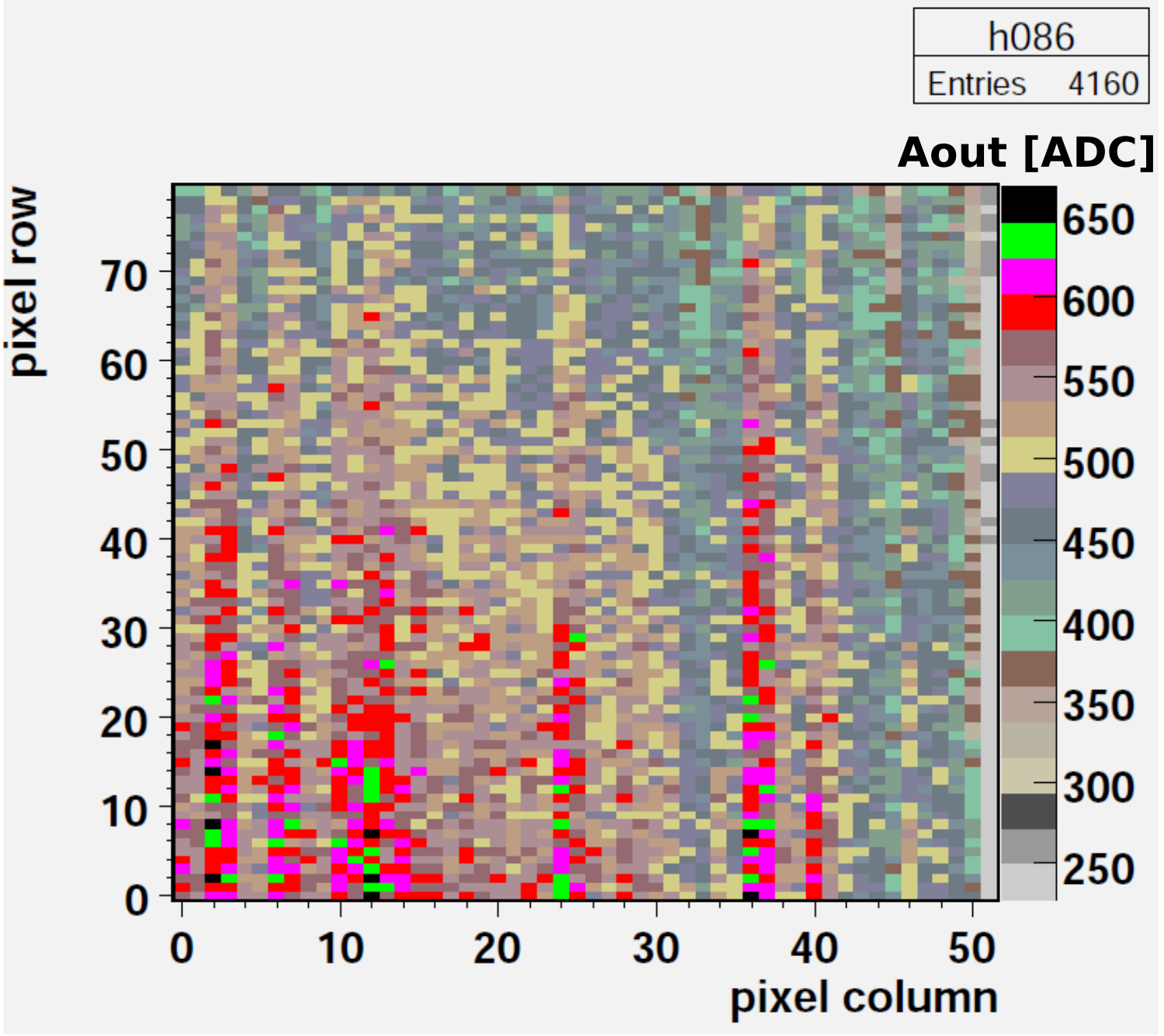



- Uniforming of thresholds brings more clusters per event
- Different chips show closer behavoiur after the trimming procedure
- Special DAC value found for Chip 8?

# Known issues

# Pixel map




- 52 × 80 = 4160 pixel per chip.
- Vcal = 200 DAC
- VthrComp = 80
- Strong pulse height variation:
  - gain?
  - timing?

# Open questions

- Many optimization procedures use fast reading of FPGA data (scurve data) but it works in TBM emulator mode only
- We can not see UB level in TBM emulator mode. Firmware VersionATB V6.1 (27.08.2010 15:35) ID=22A71BED TS=4C84D636.

  Done so far:

  - 3d scans: clk (LHC clock), sda (DACs programming), rda (token out signal). Takes 2 hours each, ~2 days in total → no UB level
  - TBM DAC 'Dacgain' (UB TBM) and 'Ibias_DAC' (UB ROC to UB TBM) have no effect to UB level
  - No TBM:

**Data: 6 : -211 17 126 : -45 15 190 73 -44 189 : 7 8 7 8 7 9**

  - TBM (gain 4, longer header and trailer):

**Data: -750 -750 -750 0 374 374 186 : 374 68 500 : -172 64 752 292 -176 764 : 32 -750 -750 0 0 374 -188 186 -188**

- We need to use bigger time delays between FPGA and USB before data transfer to PC. Fast computers, slow USB-1 ? Example:
  - Data lost at beam test: slow USB, time window was not wide enough for sending of large data blocks. Solved by reducing of data block size sent via USB from $2^{15}$ to 10.000

# Back up slides

# Temperature test [Temp]

- The CMS pixel readout chip has a built in temperature sensor  designed to measure temperatures in the range [-30°C, +70°C]

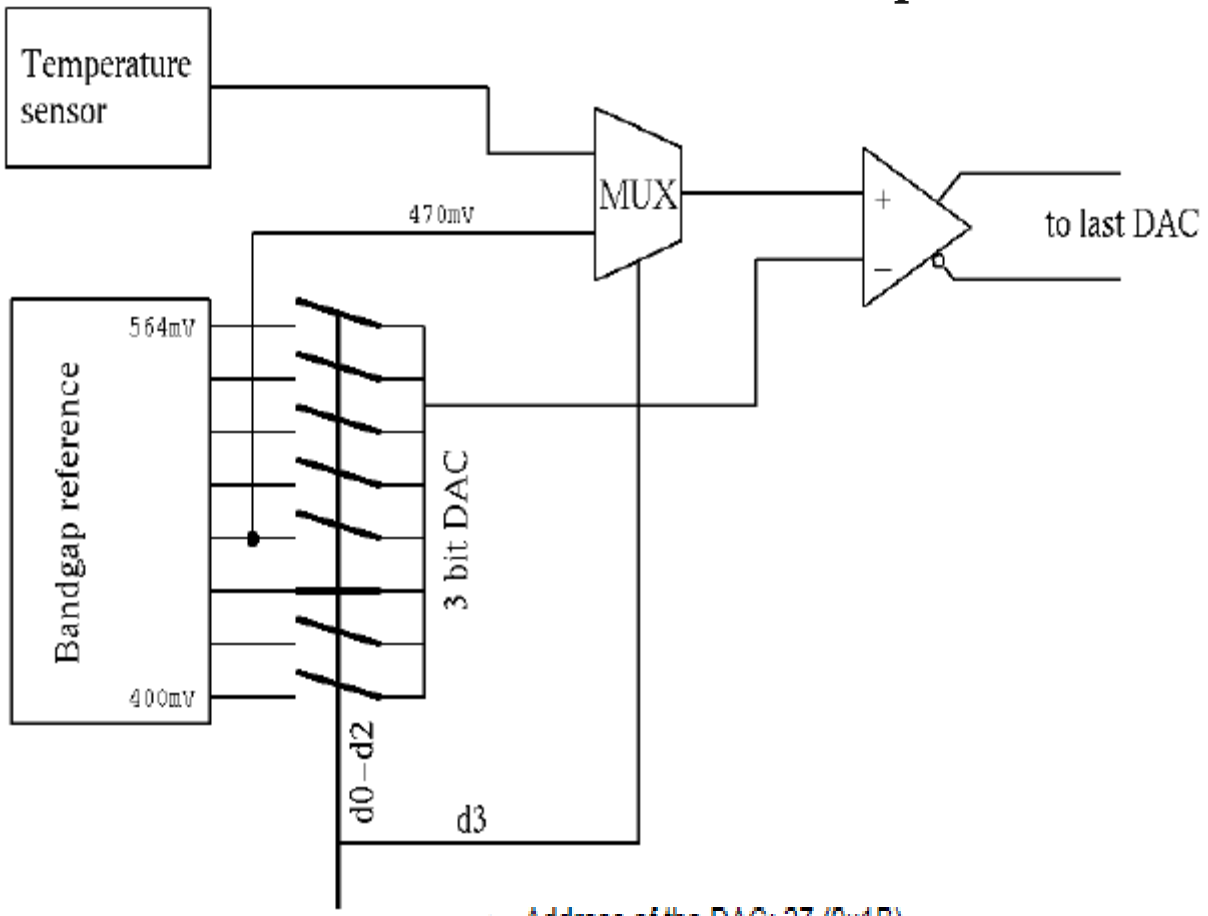
- Test signal is a LastDac ADC signal (LD) ~ to voltage difference between T sensor (temperature dependent) and reference (temperature independent)

- For better accuracy 8 different windows (reference voltages 400 – 564 mV) of measurement are defined: one part of T° measurements compared to one V window, another part to another V window etc. Windows are programmed by register 27 'RangeTemp'

- Calibrate output signal to extract the voltage difference from the measured LD ADC value. The sensor output signal is replaced by 470 mV for calibration. Make a linear fit to the calibration points differ from the ROC Black level. This fit is used to determine the measured voltage difference, which is finally added to the known reference V to get a sensor voltage

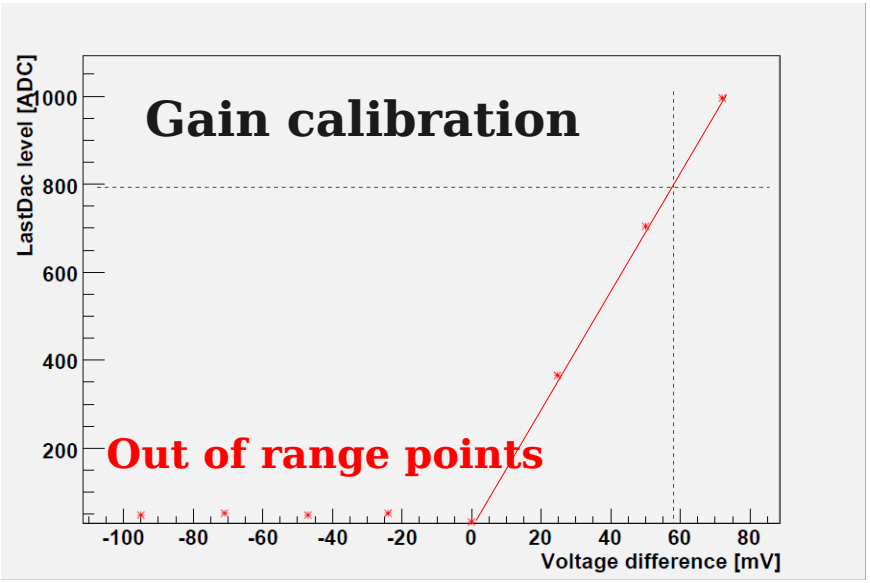
# T measurements

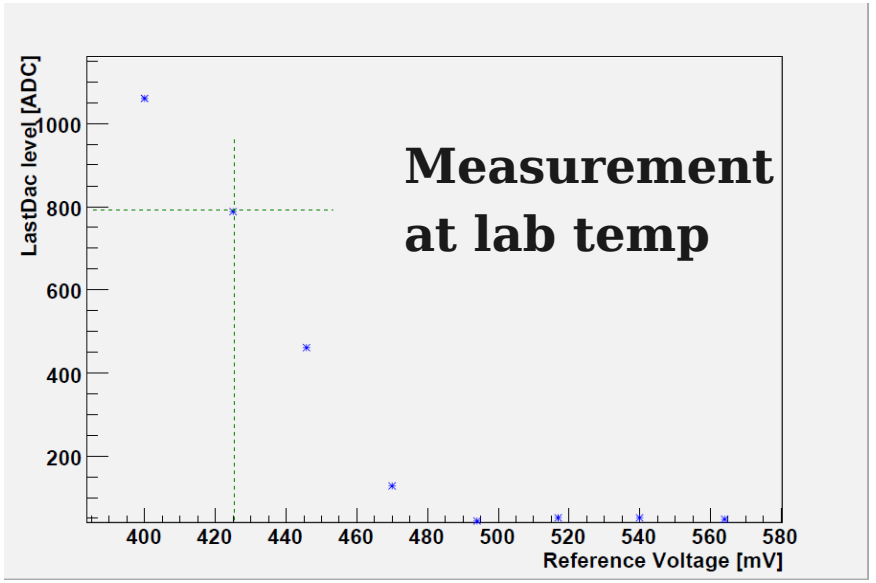
**PSI46 Specification:**




- Address of the DAC: 27 (0x1B)
- The first 3 data bits set the reference voltage in the range [399.5mV, 564mV] in steps of 23.5mV (unirradiated).
- Bit 4 switches between the temperature sensor output voltage (bit cleared) and a fixed voltage of 470mV (bit set).

# Temperature test results




Voltage difference = Vref – 470 mV

- Example chip 2:
  - Look at ref. Voltage = 425 mV
  - measure LD = 800 ADC,
  - => V difference = 58 mV
  - Sensor Vtemp = 425 + 58 = 483 mV
  - T = 0.625 ( Vtemp – Vmid )

**Average temperature (°C) measured by different ROCs**

| Chip 0 | Chip 1 | Chip 2 | Chip 3 | Chip 4 | Chip 5 | Chip 6 | Chip 7 | Chip 8 |
|---|---|---|---|---|---|---|---|---|
| 17 | 16 | 21 | 19 | 17 | 21 | 20 | 17 | 16 |

**Temperature may increase by 3°C during test**