Pixel module testing at DESY

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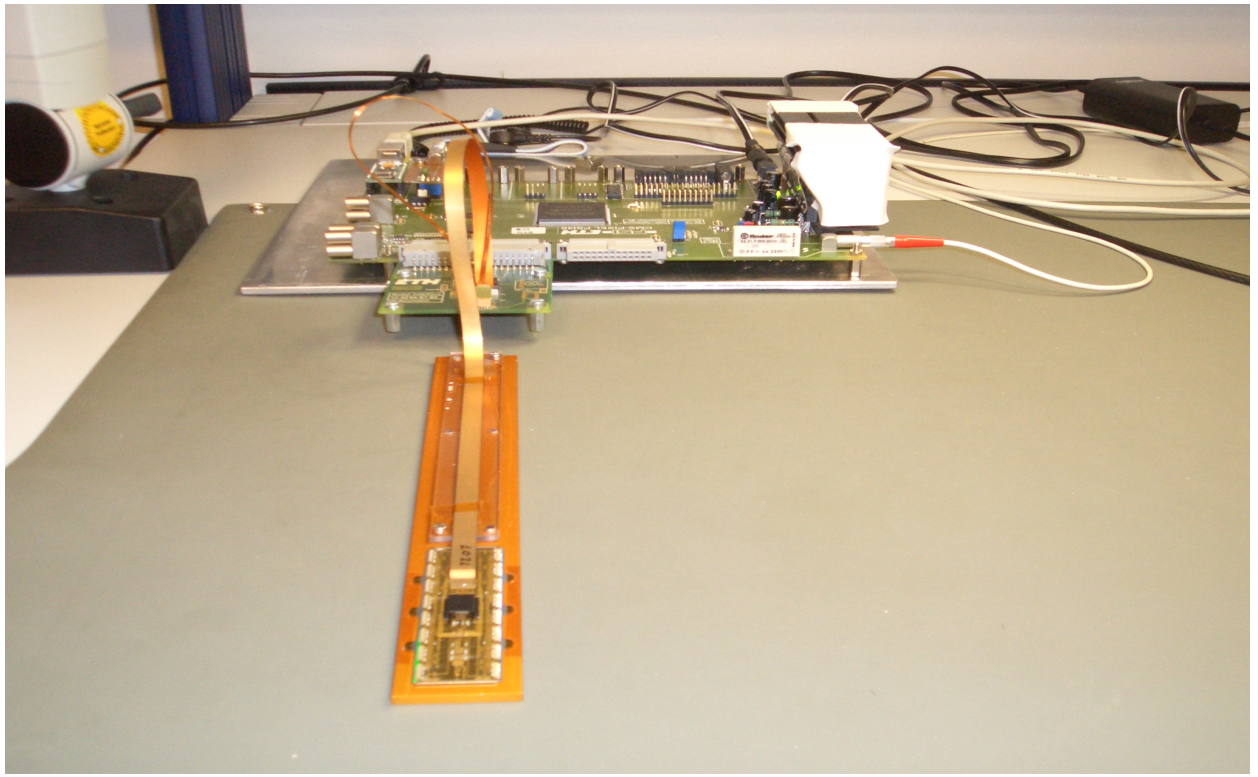
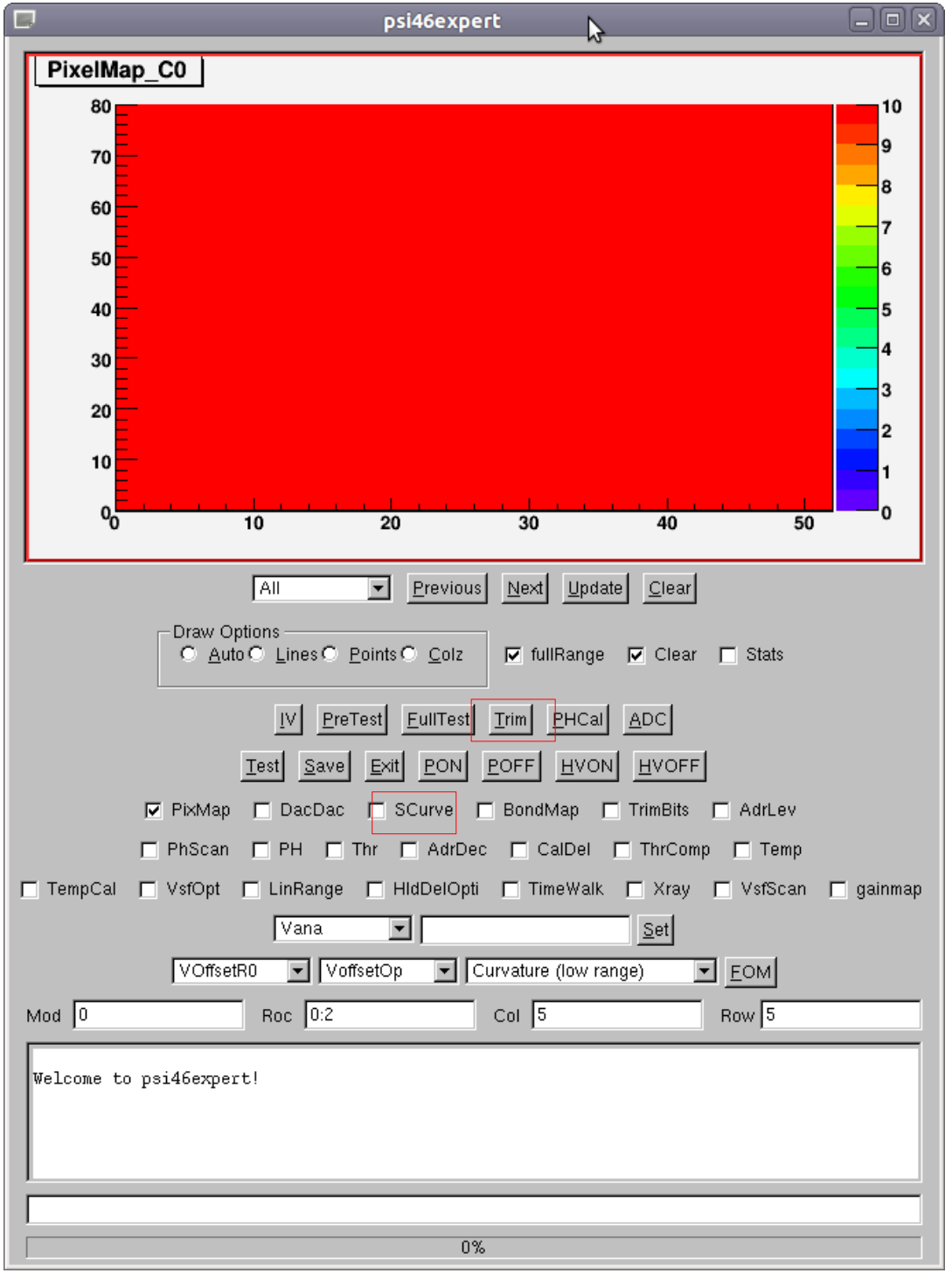


- Progress in threshold optimization

GUI

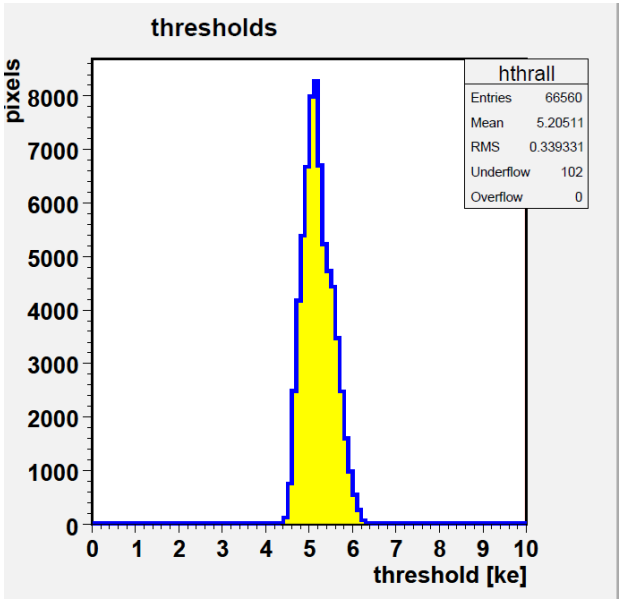

psi46expert
PixelMap_C0
All
Previous
Next
Update
Clear
Draw Options
Auto
Lines
Points
Colz
fullRange
Clear
Stats
IV
PreTest
FullTest
Trim
PHCal
ADC
Test
Save
Exit
PON
POFF
HVON
HVOFF
PixMap
DacDac
SCurve
BondMap
TrimBits
AdrLev
PhScan
PH
Thr
AdrDec
CalDel
ThrComp
Temp
TempCal
VsfOpt
LinRange
HldDelOpti
TimeWalk
Xray
VsfScan
gainmap
Vana
Set
VOffsetR0
VoffsetOp
Curvature (low range)
FOM
Mod 0
Roc 0:2
Col 5
Row 5
Welcome to psi46expert!
0%

Threshold optimization algorithm

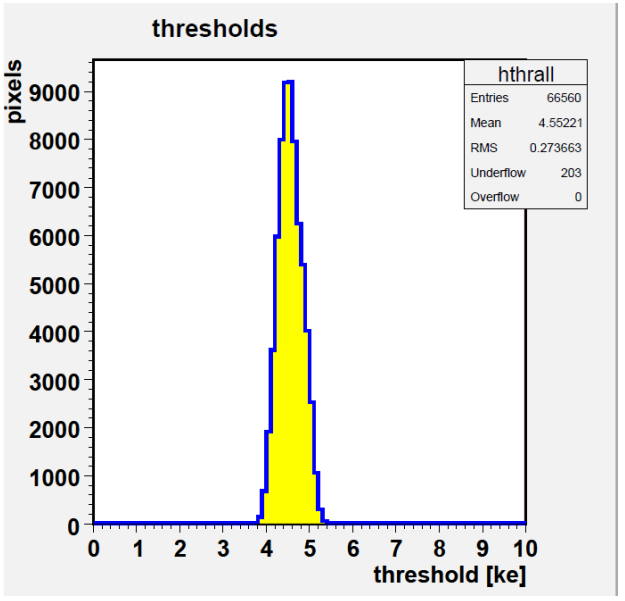
- If comparator thresholds are adjusted with global VthrComp only: spread of thresholds in ROC ~300 e^- due to transistor mismatches
- Unify pixel thresholds by 4 trim bits (values from 0 to 15) and scale with Vtrim DAC
- Each trim bit value is set such that Vcal-threshold of the pixel differs least from the selected target threshold in the procedure
- Use as low target Vcal as possible: good charge sharing, good for radiated chips with low charges

Trimming results, Feb. 24

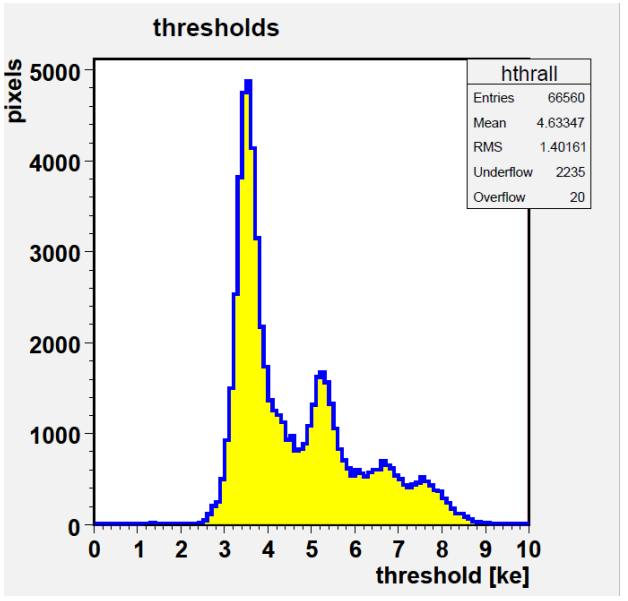
TrimVcal=60

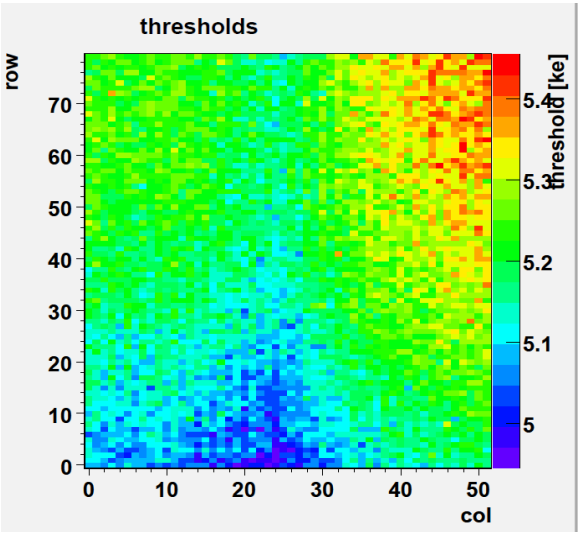


TrimVcal=50



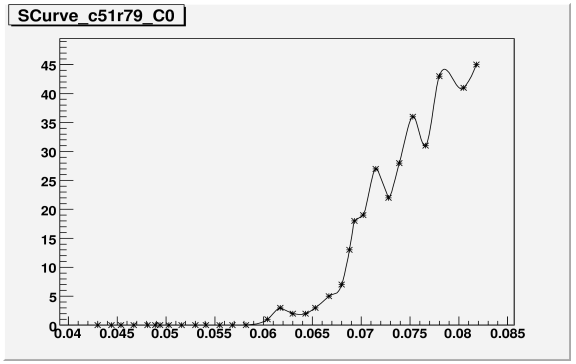
TrimVcal=40





- M1207, all pixels
- 4160x16 TrimBits set
- 6% spread: better than for single chip before trimming

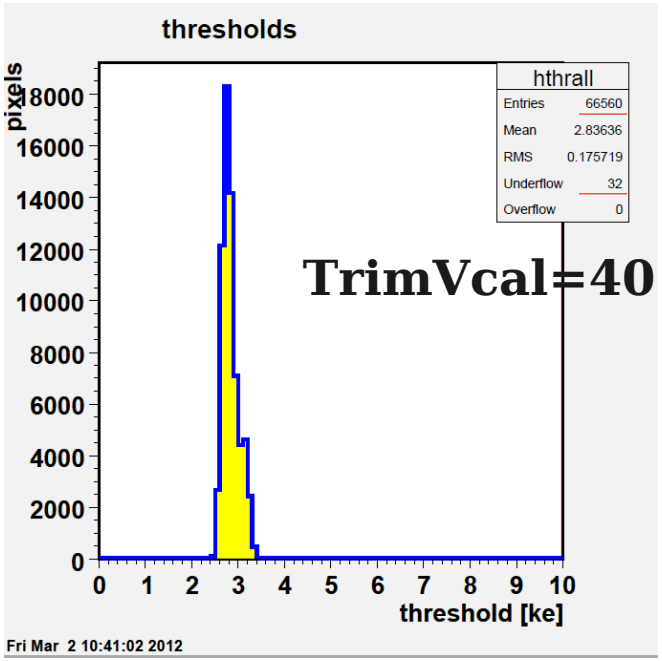
- Underflows: bad fit of Scurves
- Peaks are ~30% higher than expected (?)

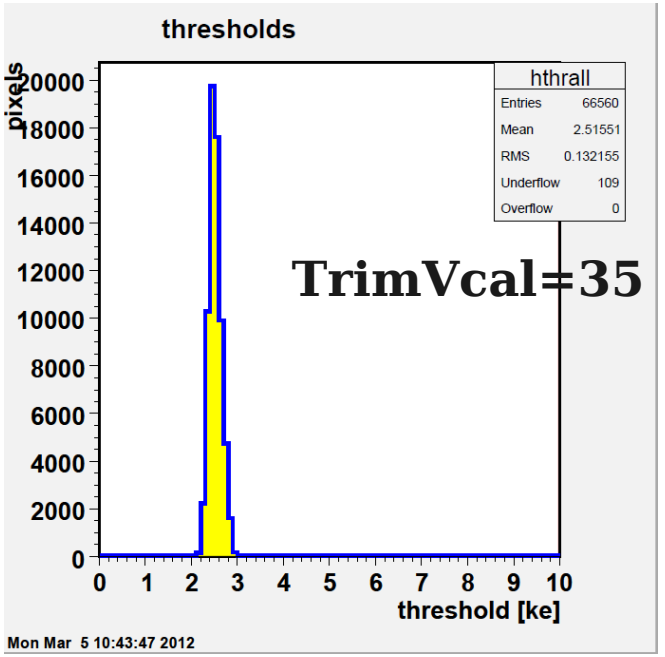


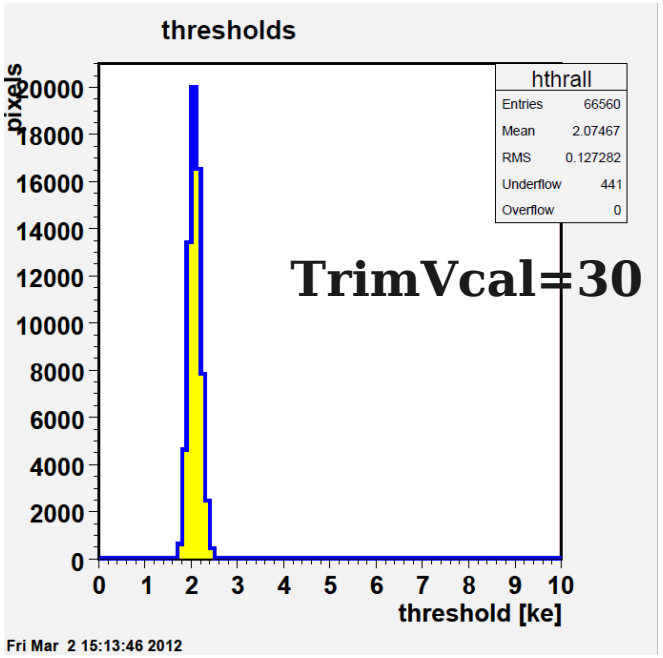
Changes in the algorithm

- In Chip Thresholds definition: longer time delay between FPGA and USB before data transfer to PC. Time consuming procedure: sending 10 commands to FPGA and waiting for response of each pixel. It helps to avoid crashes in the beginning of procedure
- Use only 1 BCrossing: brings thresholds peak to nominal position
- Total time per module: 80 → 100 min.

Trimming results, new

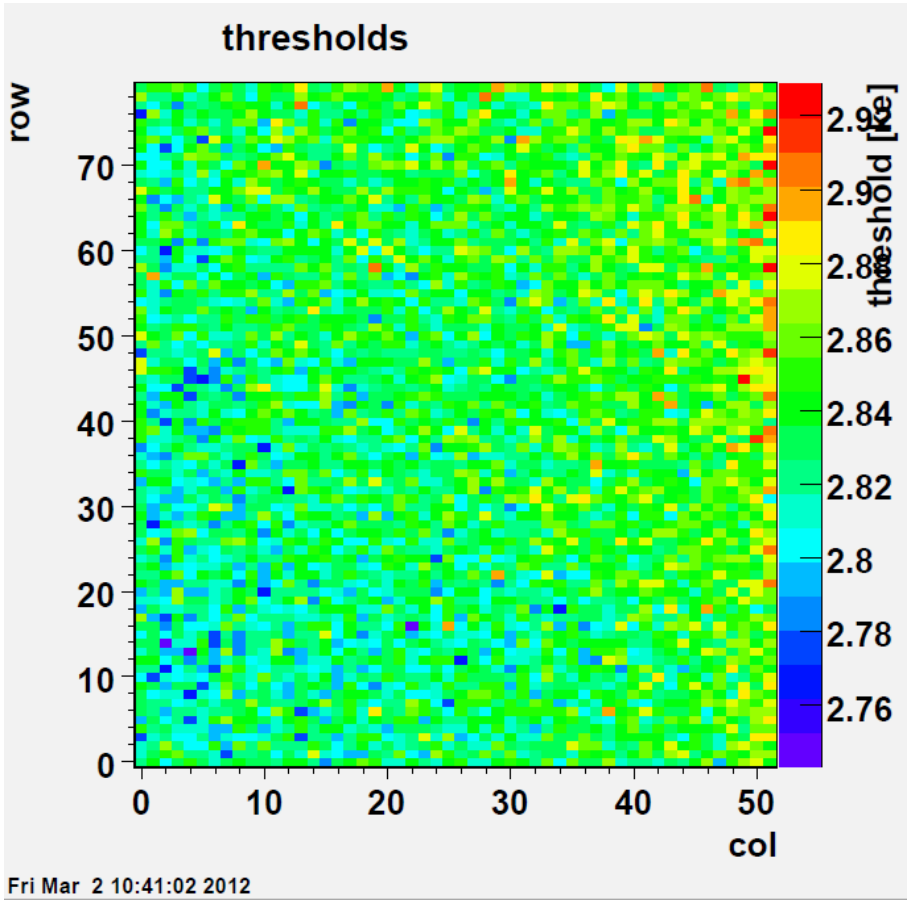


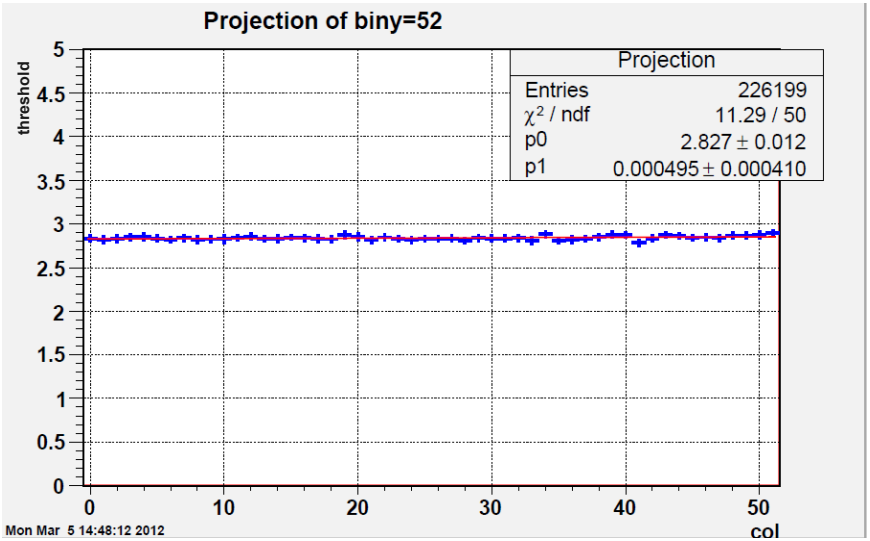


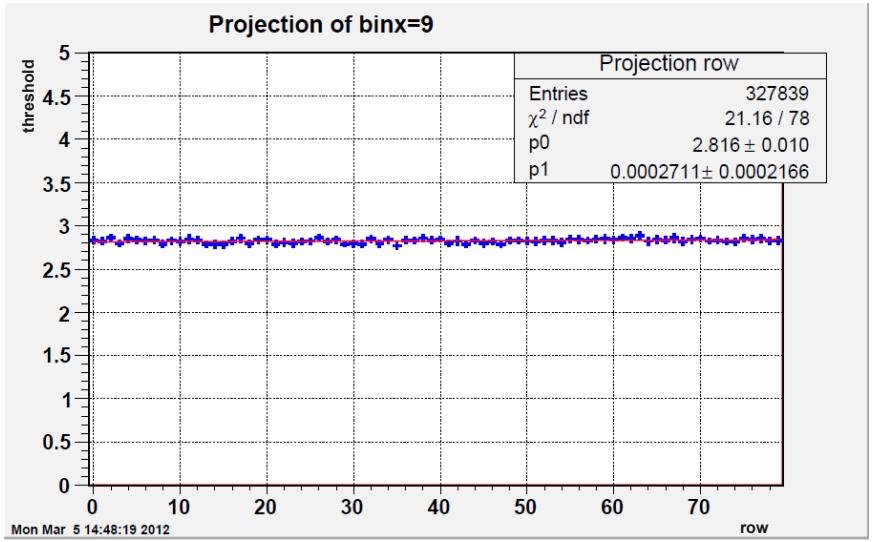


- M1207, all 66560 pixels trimmed
- Peaks are at nominal positions
- 6% spread (14% if not trimmed)
- 2.8 ke is an optimal threshold for M1207 (?)

Trimming results, new

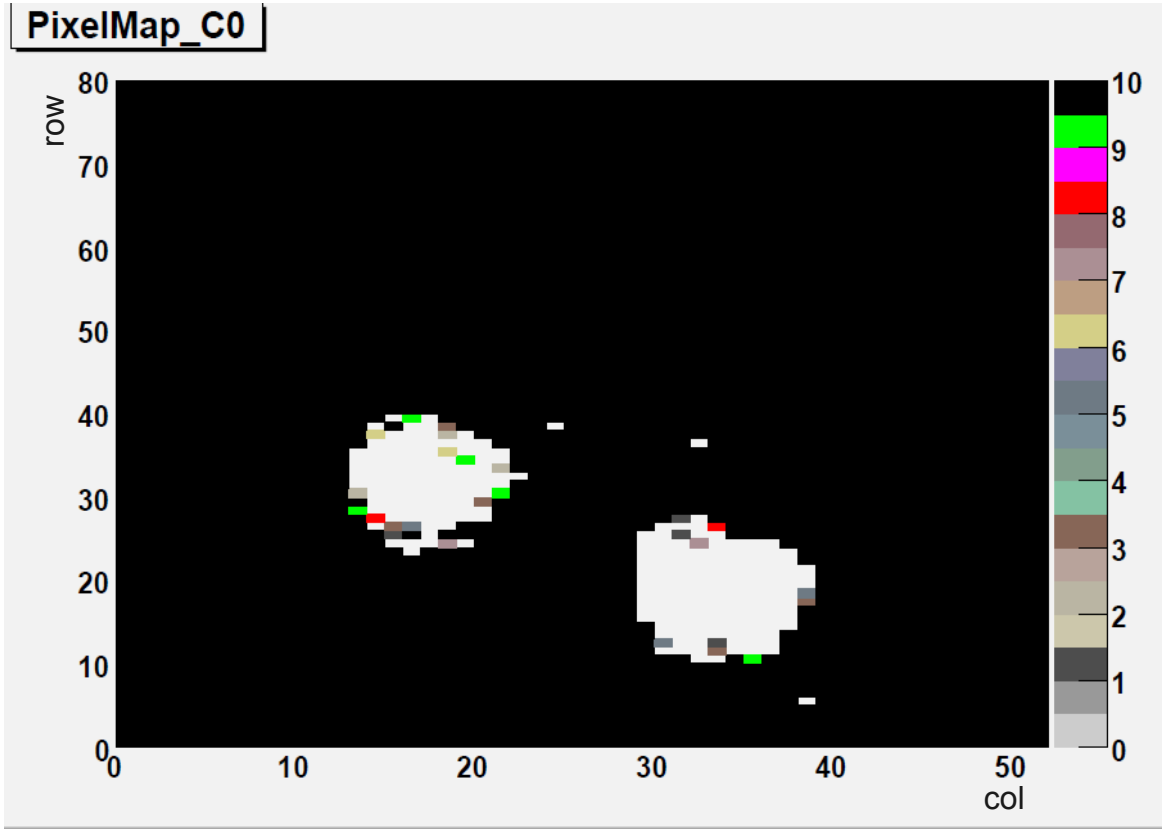






- M1207, all pixels trimmed
- TrimVcal = 40
- 2d is more uniform now

ROC 13 (Not from M1207)



- Sad news: chip 13 is not really functional even after wire bonds repairing

Summary

- New progress in Trimming procedure is done → step forward towards module threshold optimization
- M1207 after Trimming: spread of pixel thresholds reduced from 14% to 6%. Operational threshold = 2.8 ke
- PSI: effectively usable threshold is 3.2 ke [Nuclear Instruments and Methods in Physics Research A 565 (2006) 188–194]

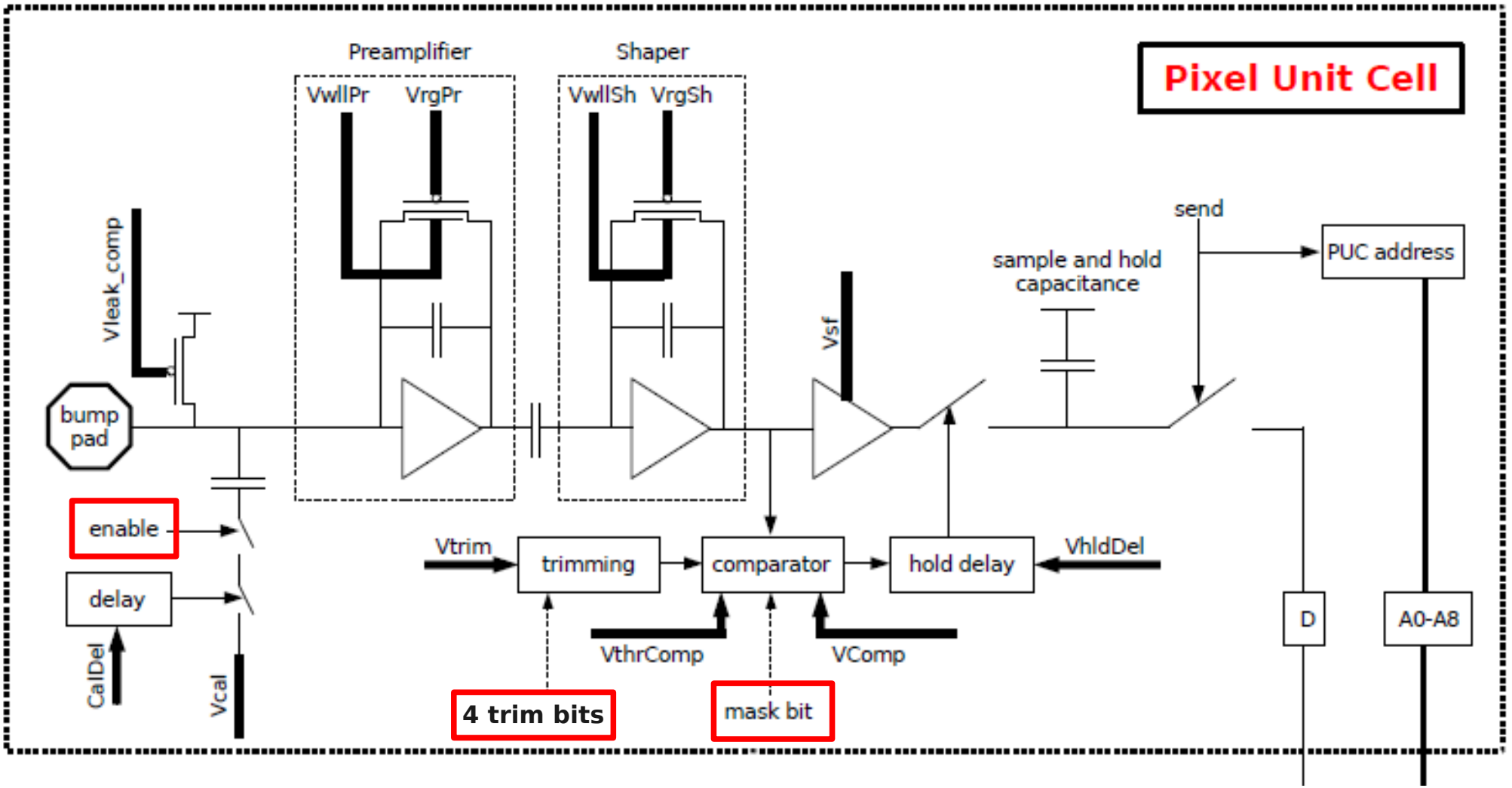
Back up

psi46 DACs, Pretest

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

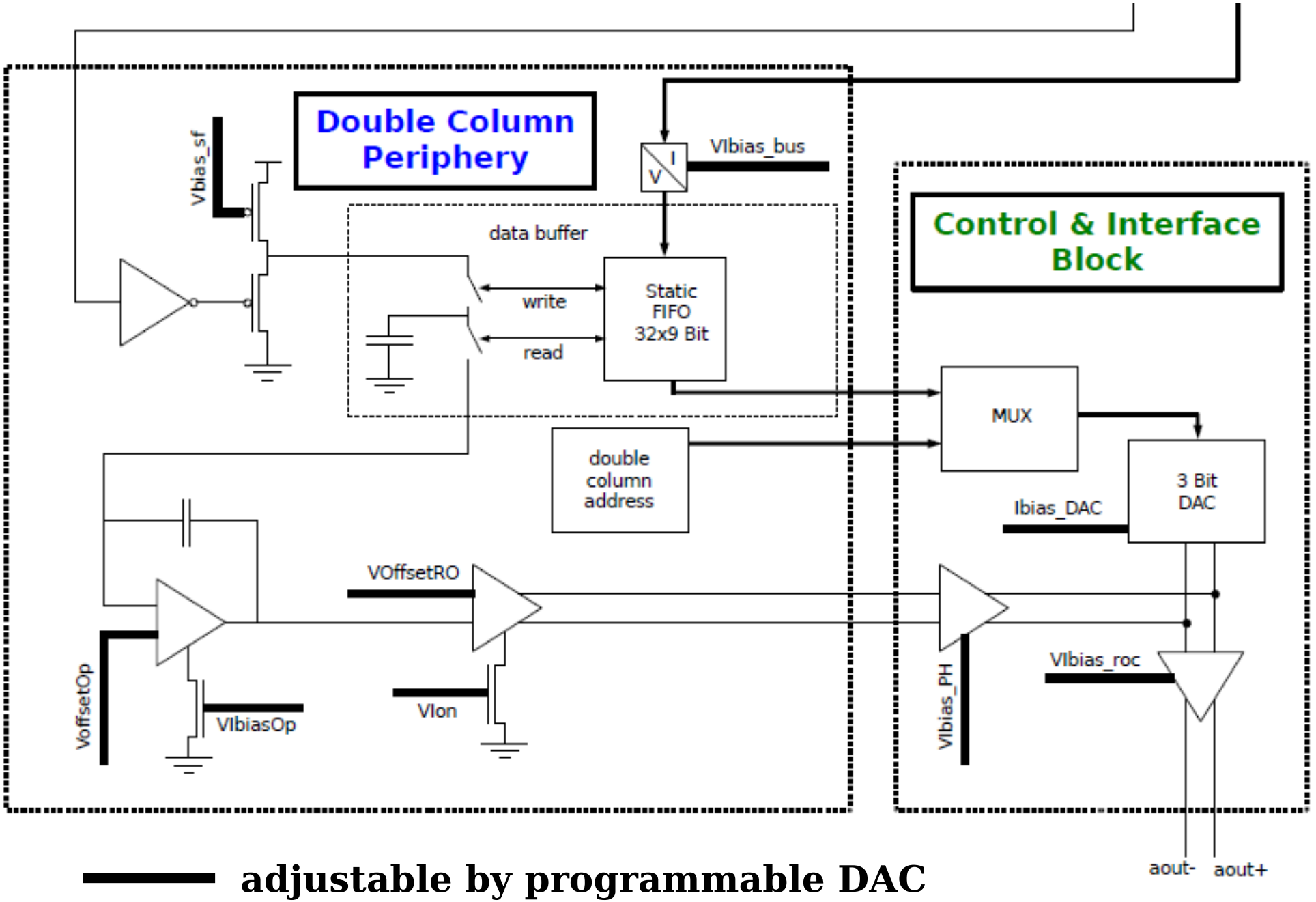
psi46 pixel readout chip



adjustable by programmable DAC, per ROC

programmable register, per pixel

psi46 pixel readout chip



adjustable by programmable DAC