Synchronizing the clock to the beam

Luigi Calligaris

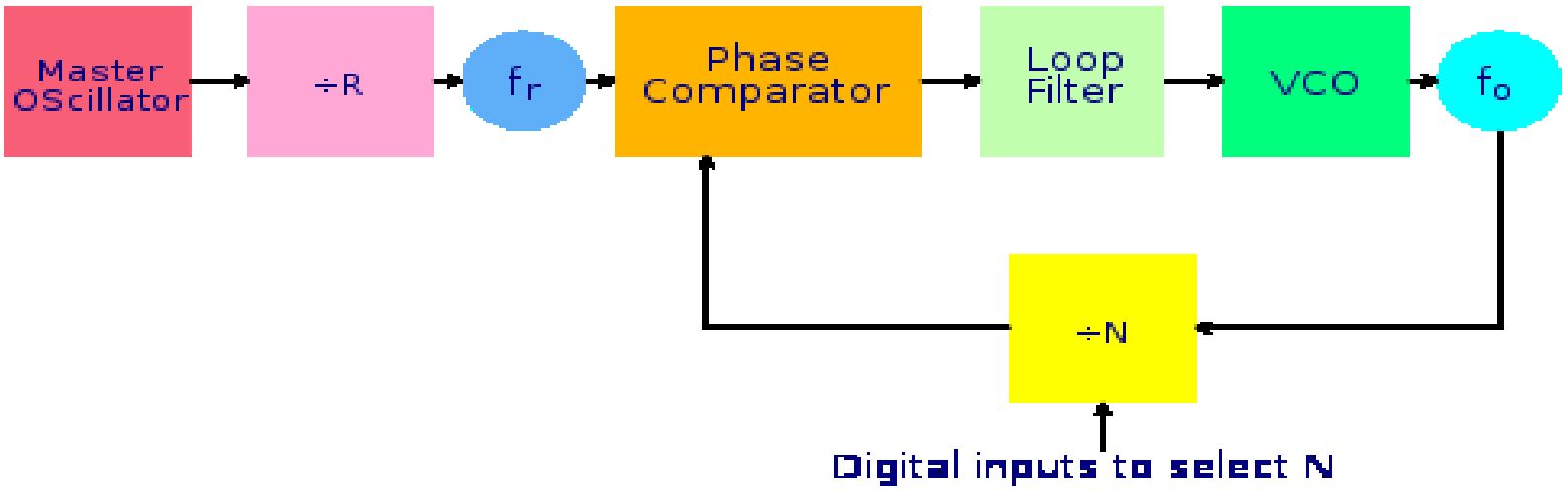
DESY CMS Phase I Pixel meeting, 09/03/2012

Synchronizing the clock

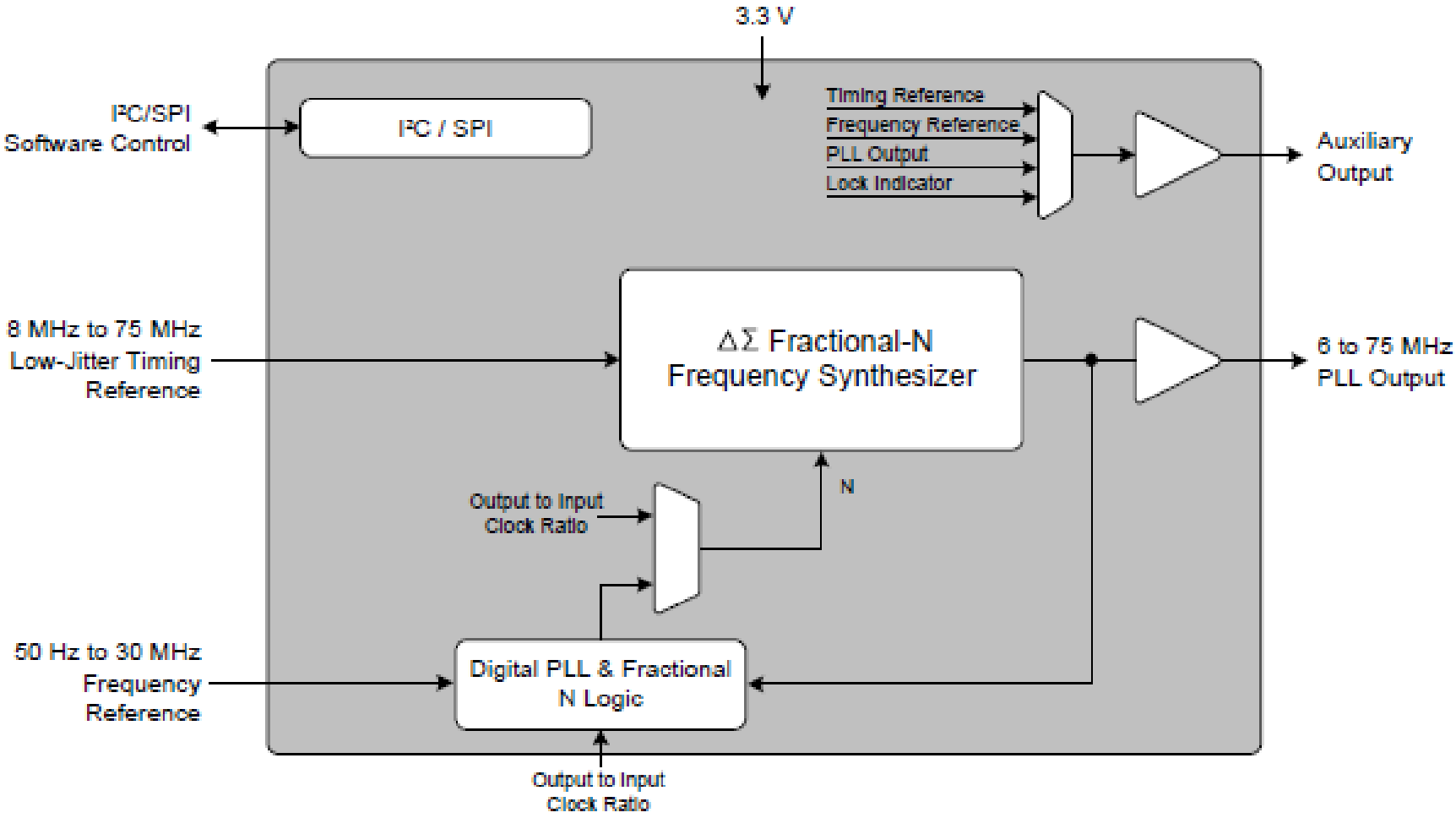
- At the moment Pixel ROC is clocked internally
  - Particles could be assigned to different “BX” tags
- We want to synchronize the CMS pixel to the DESY II beam
  - CMS Pixel → approx. 40 MHz clock
  - DESY II beam → RF is approx 1,024 MHz
- Testbeam area has a wire carrying RF signal
  - Try to use it to synchronize our chip
  - We have to synthetize 40 MHz from 1,024 MHz

PLL: a negative feedback loop

- Take input signal with frequency f_r
- Generate with a Voltage Controlled Oscillator an output signal with frequency f_o
- Divide f_o by the multiplication factor N
- Phase compare f_r and f_o/N and output as a voltage
- Feed this voltage to the VCO

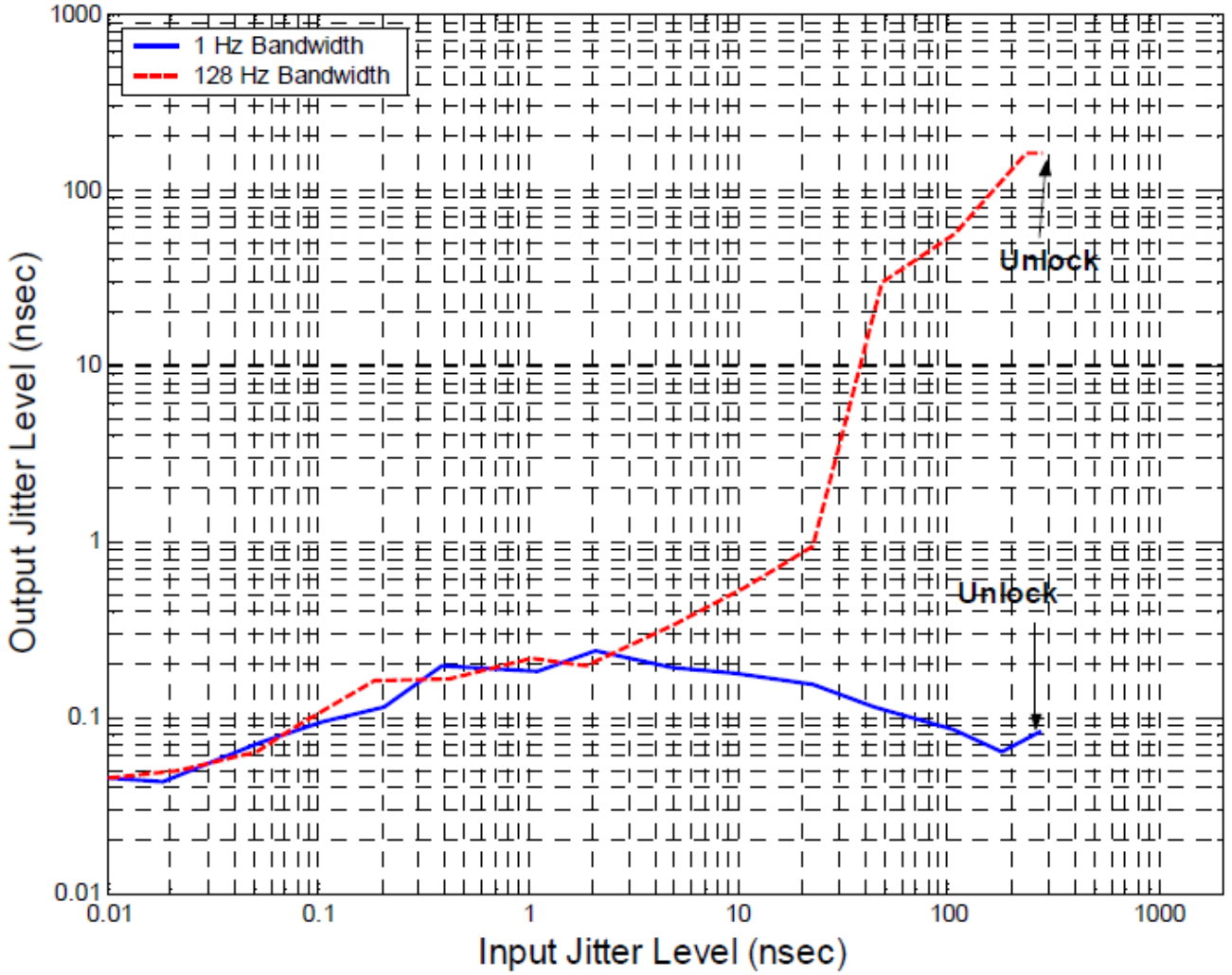


Our setup – Cirrus Logic CS2000CP



Status

- Thu 8/3/2012
  - First tries at the test beam
  - PLL doesn't lock to DESY II signal
    - Probably due to jitter in the input clock signal
  - PLL does locks on a very stable function generator signal at the same frequency and amplitude
- Hypothetical mechanism for lock failure
  - Amplifier in DESY II crate is not powerful enough to drive the long cable with a fast rise time
  - Time walk in this signal leads to jitter
  - The PLL cannot lock due to jitter


1 Hz Bandwidth
128 Hz Bandwidth
Unlock
Unlock
Output Jitter Level (nsec)
Input Jitter Level (nsec)
1000
100
10
1
0.1
0.01
0.01
0.1
1
10
100
1000