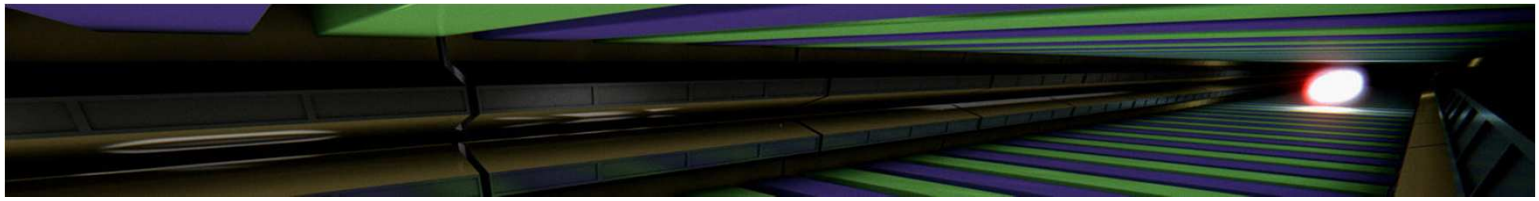

WP76 status summary

XDAC review meeting

14-16.5.2012

C.Youngman for WP76

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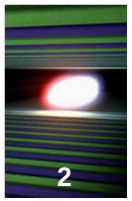
Content



- Electronics – DAQ and slow control
- Software
- Slice test
- Integration
- Conclusions

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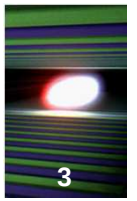
Devices to control, monitor, readout, analyze…



- Optics (WP73)
  - KB mirrors for focusing
  - Refractive lens focusing
  - Monochromatic
  - Collimator
  - Slits
  - Attenuators
- Sample environment (WP79)
  - Particle injector
  - Cryostat
  - Precision stages
- Beam diagnostics (WP74)
  - Intensity monitors
  - Beam positioning monitor
  - Photon-electron spectrometers
  - K-monochromator
  - Screens and cameras
- Vacuum systems (WP73, 8x)
  - Turbo pumps
  - Ion pumps
- Laser systems (WP78)
  - Pump laser and diagnostics
- Vacuum systems (WP73, 8x)
  - Turbo pumps
  - Ion pumps
- Complex detectors (WP75)
  - 2D pixel cameras
  - pnCCD
- Simple detectors (WP8x)
  - e- and ion TOF
  - Diodes, BS-foils, diamonds
- Other control systems
  - e-machine
  - Undulator
- DAQ sub systems
  - VETO sub-system
- Software systems
  - DM and SC devices

Long list = need common solutions for entire control-DAQ-DM-SC chain

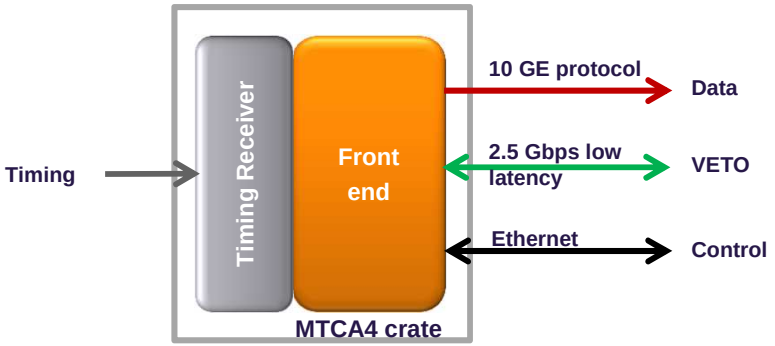
Electronics for control and DAQ

Task

- Attribute configuration, monitoring and run state driving
- Data readout and processing

Solution

- Ethernet for control and monitoring
- 10GE Ethernet for data streaming (readout)
- Low latency protocols for feedback systems
- FPGA data processing (formatting, rejection)
- e-machine timing board for synchronization



Implementation status on next slides

- Fast ADC = diodes, diamonds…
- High-Speed digitizers = TOFs, VMI, XBPM, XGDM, PES…
- Common backend DAQ = 2D, TOFs…

Prototype single width MTCA e-machine Timing receiver Board (Stockholm University / DESY)

Outlook

- See comments on slides

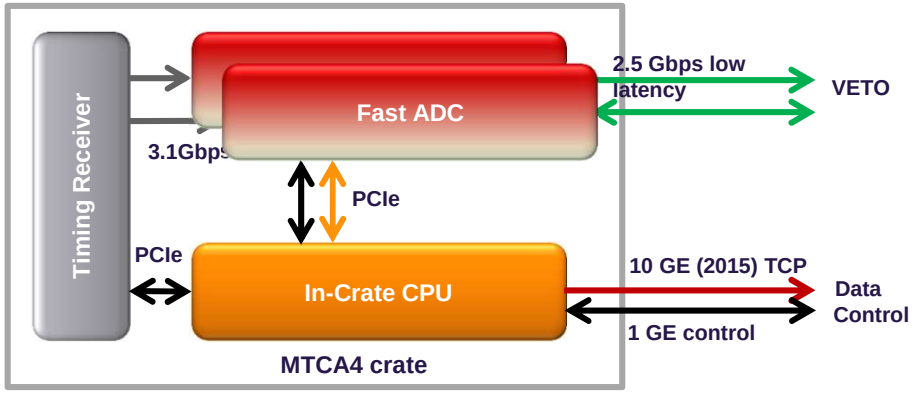
Fast ADC

Task

- Acquire 4.5MHz pulse data from 0D detectors

Solution

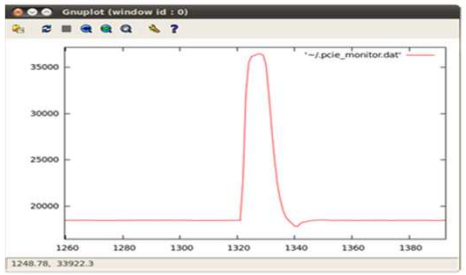
- Use Struck SIS8300 MTCA.4 Fast ADC board
  - 125 MHz, 16 bit resolution, 10 channel
  - Vertex 5 (data and VETO processing)
- Signal shaping
  - Build custom Rear Transition Module



Status of tests with APD

- Custom RTM developed with Peter Goettlicher (DESY)
  - Signal shaping increasing the pulse length and maintain the amplitude information
- Processing in FPGA or CPU and streaming of data
- System was tested with beam and APD module at Petra3

RTM



APD

SIS 8300

Outlook as test bed

- VETO source and related signal generation
- Using Simulink for algorithm implementation
- Baseline device server s/w control implementation for MTCA.4

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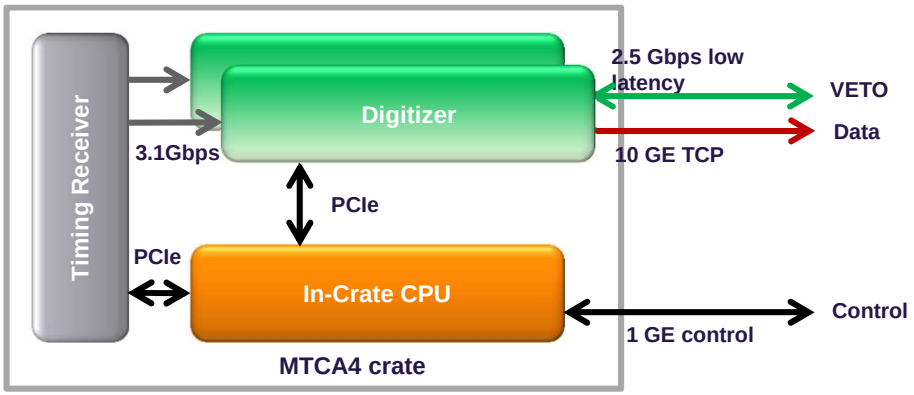
High-Speed digitizers

Task

- 1 – 7GS/s : 14 – 8 bit resolution digitizers for TOF, VMI, etc.



Solution

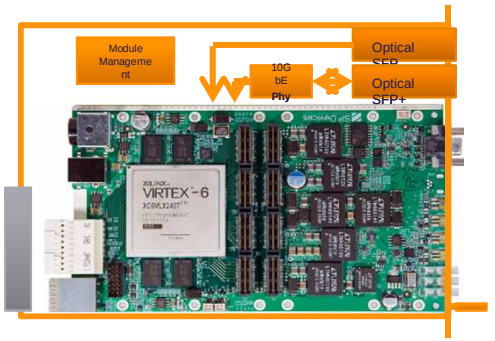
- Use SP Devices vendor digitizer family

Product	Resolution	Maximum Sample Rate	Analog Bandwidth	Channels	On-Board Memory Size	Interface
SDR14	14bit in 14bit out	800 MSPS in 1600 MHz out	500 MHz	2 in 2 out	2 x 500 Mbyte	USB, cPCIe/PXIe, PCIe
ADQ108	8 bit	7 GSPS	2 GHz	1	1024 MS	USB, cPCIe/PXIe, PCIe
ADQ412	12 bit	1.8/3.6 GSPS	2/1.3 GHz	4/2	700 MS	USB, cPCIe/PXIe, PCIe
ADQ1600	14 bit	1.6 GSPS	800 MHz	1	500 MS	USB, cPCIe/PXIe, PCIe
ADQ DSP	-	-	-	-	1 GByte	USB, cPCIe/PXIe, PCIe

- Contract signed to add 10GE and SFP low latency functionality to existing PXIe layout on MTCA board
  - Mother board common to product family – digitizer specific functionality on mezzanine

Status and outlook

- Currently testing ADQ1600 PCIe
- Expect prototype board Q3/2012, product Q4/2012



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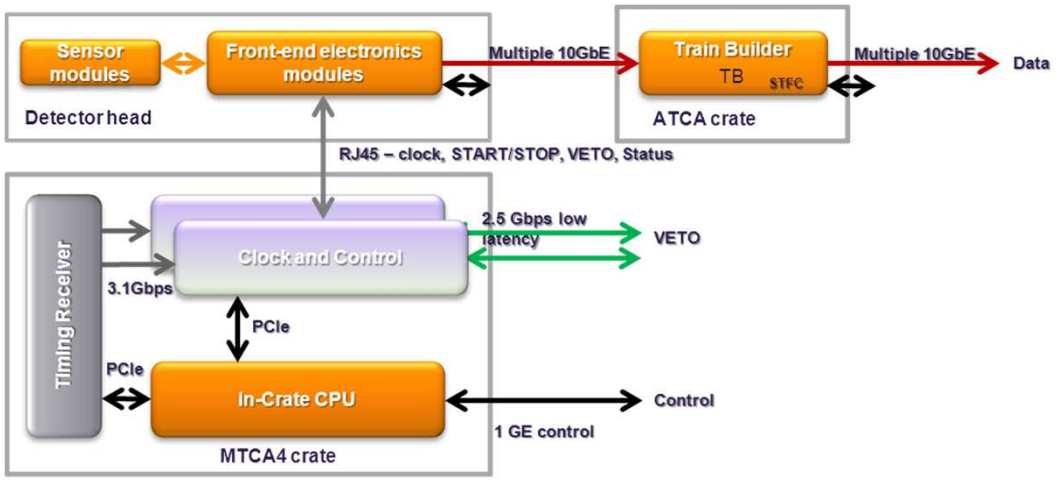
Common backend DAQ



Task

- Combine 2D camera module data
- Reformat and process data
- Push frame ordered data trains to PCL

Solution

- Control camera front end modules using custom RTM clock and control module interfaced by DAMC2 board
- Data pushed to ATCA train builder board
- Train builder pushes data to PCL using Round-Robin distribution

Status

- Prototype clock and control board onsite, s/w device in preparation
- Prototype train builder board delivery planned 9.7.2012

Outlook

- Expect working LPD (2 tile or 1/4Mpxl) by end of 2012

Prototype Train Builder ATCA Board (STFC)

Prototype Clock and Control RTM (UCL)

DAMC2 (DESY/FEA)

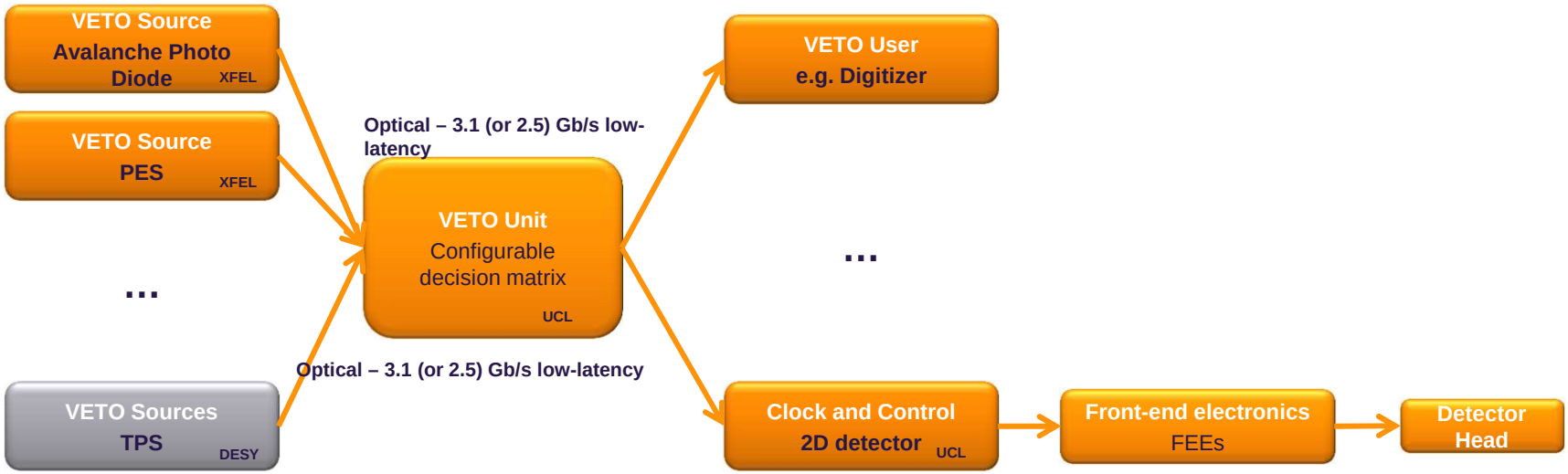
VETO System for data reduction and memory optimization

Task

- Optimize picture quality of 2D detectors, alleviate limited frame capacity in ASICs (~300-700 frames)
- Replace bad frames with new ones in ASIC before read out and transmission
- Data reduction discard useless data before transmission

Solution

- FPGAs of diagnostics and detectors provide bunch information with low-latency
- Configurable central VETO unit per experiment decides on bunch quality
- FPGAs of (all) detectors receive the decision and react on it
- Using a common protocol with beam based feedback system



Status and outlook

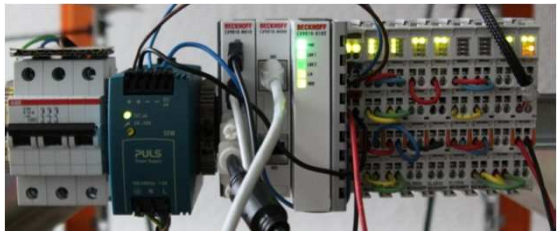
- Currently testing protocol f/w modules on DAMC2

PBS slow control for expts, optics, diags

Purpose – Control PBS "slow" experiment and tunnel systems (pumps, motors, gauges,valves…)

Solution – Beckhoff distributed EtherCAT PLC h/w

- Industry standard COTS with real time Ethernet protocol
- Technology provides required physical layer topologies (loops, trees…)
- Already used in XFEL undulator system, PETRA3



PLC h/w terminals

Firmware – PLC programming environment

- Platform Windows XP (also Windows CE and Windows 7)
- Provides FSM, main business logic; h/w synchronization (axes coupling);
- Controllable by s/w device running in linux-box (via TCP);
- Logging and high level administrative tools provided

Implementation – status

- PLC f/w code generation driven from DB of h/w connections (need cable DB KDS manpower)
- Validation of PLC version running
- Devices integrated: Varian pumps, Maxi and MKS gauges, Gauge, step and pezos…

Outlook

- Migrate to TwinCAT 3 environment (allows embedded C/C++ in f/w – "simulink" type development)
- Complete integration with control s/w and with users
- Replace current csv code driver by DB

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PBS homogeneous s/w framework

Purpose – provide a single s/w environment for control, DAQ, DM and SC(analysis)

Solution – standards

- Proper standardization results in modular, scalable and homogeneous software
- use C++ / Boost / Python / PyQt as core technologies
- Do not re-invent the wheel, use high quality libraries: Boost (shared_ptr, any, msm, function, asio), PyQt, OpenMQ, Log4cpp, CImg, etc.

Issues of specific interest for control and DAQ

- **s/w or h/w instances** to control are called **Devices** = **plugins created by factories** in Device servers
- **communication:** use MOM broker (**OpenMQ** now) and **p-2-p** for large volume data transfer
- **configuration** and reconfiguration: **XML and XSD** (i.e. self-describing) driven (cmd line, file, DB)
- **flow control:** all devices are **FSM** enabled (message event driven)

Implementation – status

- **first s/w release mid-March contains complete toolkit set**
- Devices for h/w (MPOD, Beckhoff…) and s/w (PC layer, Data feeders…) online
- Generic GUI integration in progress

Outlook

- Final DB design and update of s/w API starts 1.6.2012
- Upgrades driven by requirements (OpenMQ to ZeroMQ?)

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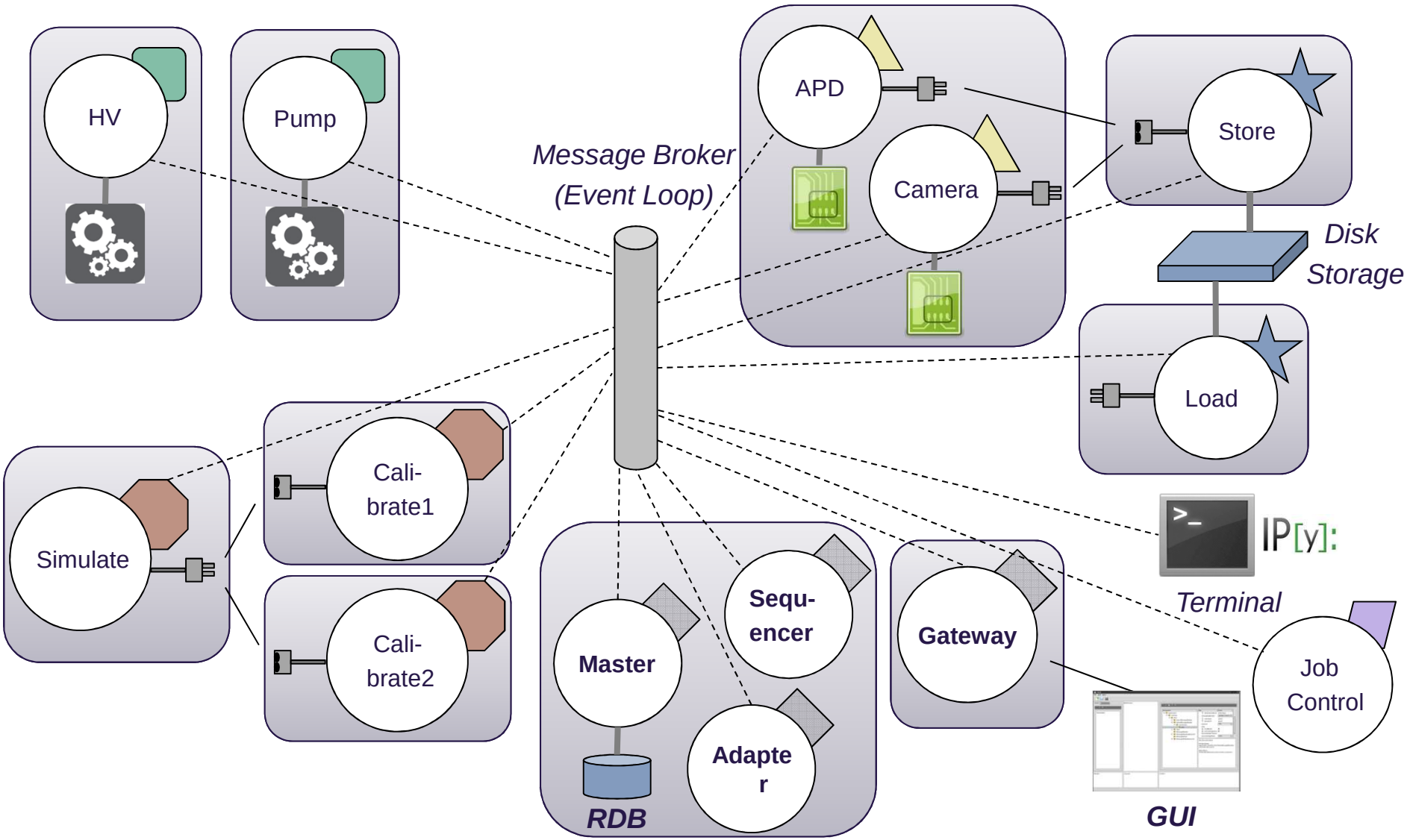
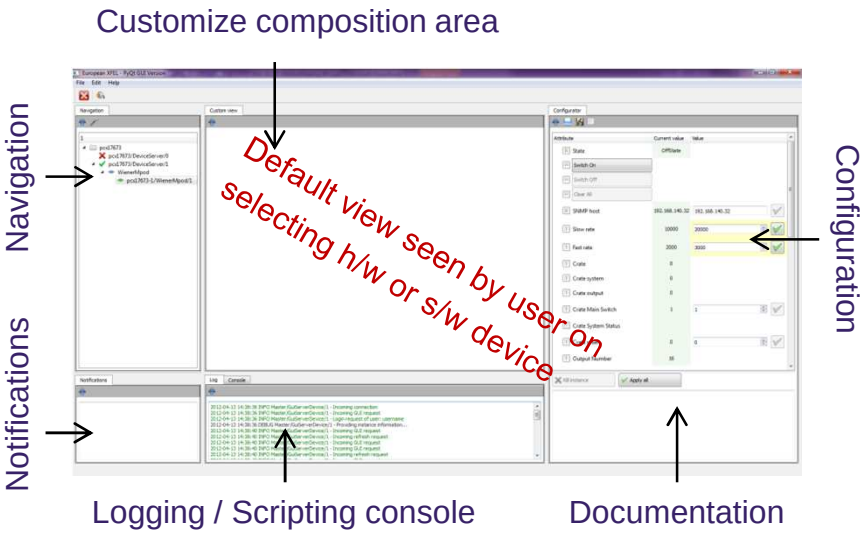
PBS s/w device big picture



PBS GUI development

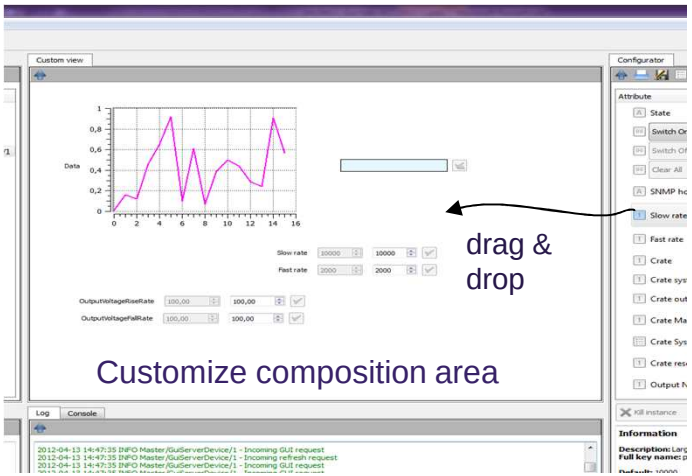
Hot off the press

- generic, multi-purpose, cross-platform GUI
- self explaining, default layout for any device
- customizable user panels
- fully integrated with s/w framework
  - many features
- Widgets are plugins – 3rd party ones can be used with a simple wrapper (e.g. have tested with Taurus widget)



Generic GUI

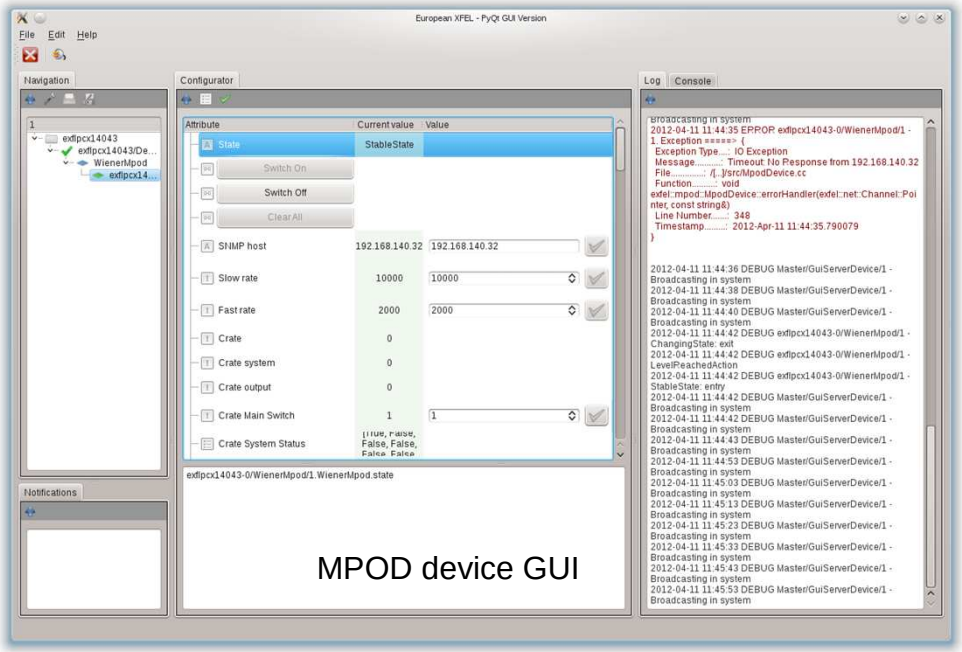
- Framework XML and XSD usage = self description
- Configuration attributes immediately seen
- FSM states immediately drivable
- Device driven – not code generation



Outlook

- Include user-role driven (database)
- …

Device integration



Devices s/w in implementation

- MPOD Wiener+Iseg power supplies
- Fast ADC system
- Beckhoff
- Clock and control (TB and LPD needed soon)

Feedback coming in from users in the field

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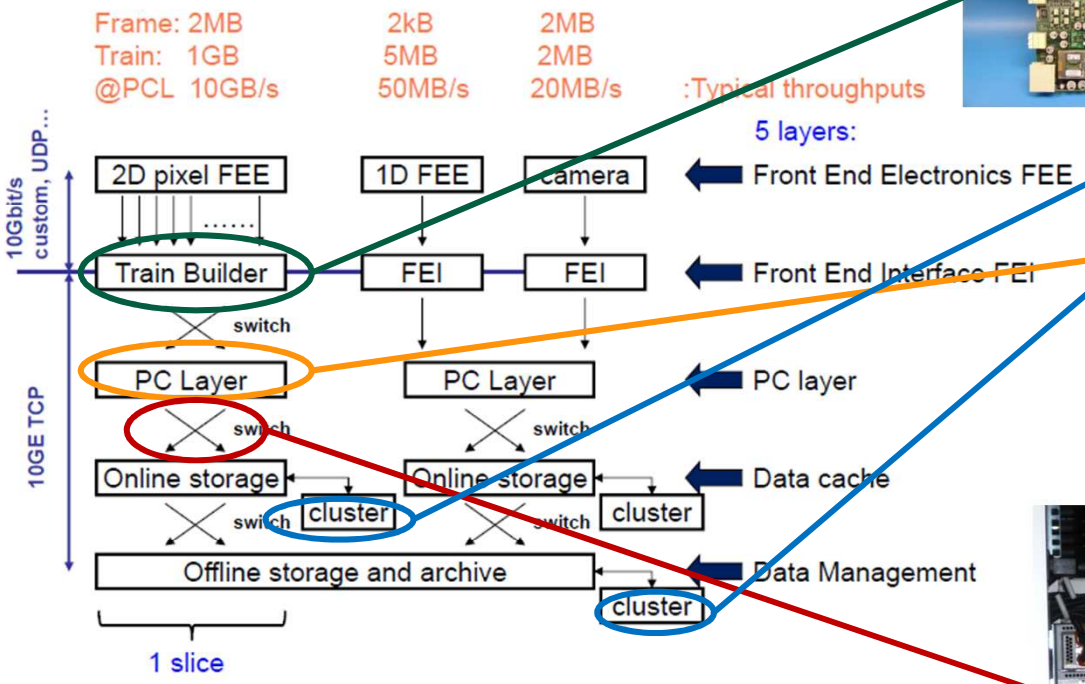
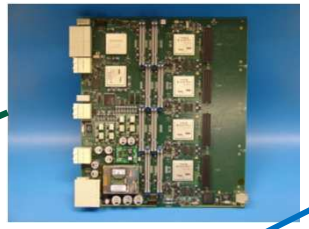
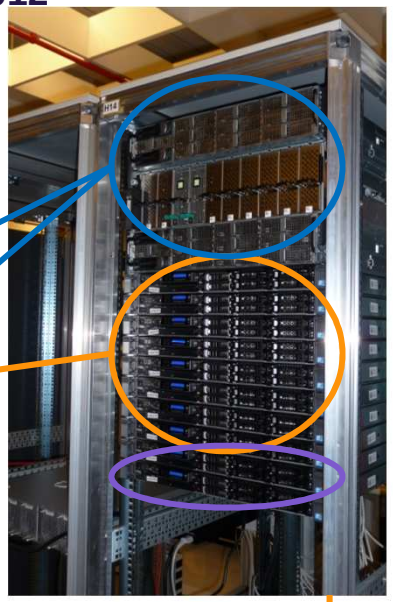
Slice Test: DAQ through DM to SC

DAQ and DM architecture – ½ to 1Mpxl slice test in progress
Final DM system in DESY-CC = 10PB scalable to 100PB
Plus compute services



TB prototype Q3/2012

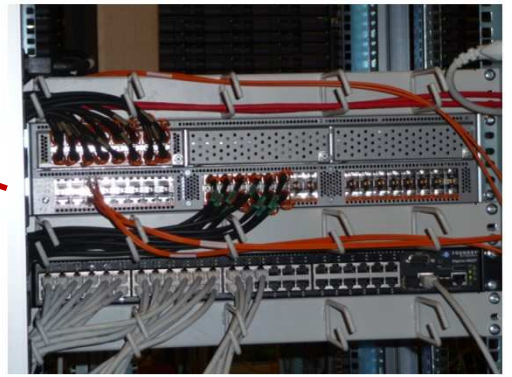


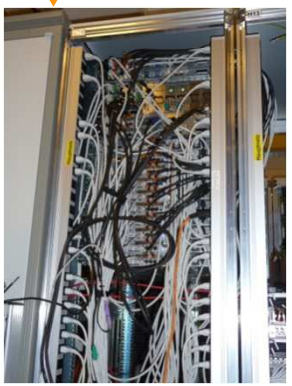


Compute + GPUs nodes

PC nodes

DB+MDS nodes





10 Gbps switch

Prove architecture

- Network, processing and storage performance
- Local and clustered file system usage
- s/w framework APIs (HDF5, net…) and applications (PCL, SC pipelines)
- Test bed for run control and sequencing, calibration…
- Test bed for integrating new h/w (e.g. DDN storage tests)

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Hardware status

- Purpose of h/w is to test all features of DAQ/DM architecture
  - Network, computing, storage, file systems, s/w, deployment, dCache…
- Final width of slice is 16 input TB input links = 1Mpxl
- **Status of first ½ of slice 10.5.2012:**

h/w	function	#	Spec	Status
PowerEdge R610	PC layer	8	3GHz, 2Socket, 6Core, Intel X5675, 96GB, Intel X520 DA2 dual 10GbE NIC	running
PowerEdge R610	Metadata server	2	3GHz, 2Socket, 6Core, Intel X5675, 96GB, Intel X520 DA2 dual 10GbE NIC	running
PowerEdge C6145	Computing cluster	2	2.6GHz, 4Socket, 16Core, AMD 6282SE, 192GB, Intel X520 DA2 dual 10GbE NIC	running
Cisco 5596UP	10GbE switch	1	48 ports (extendible to 96), wire speed, SFP+	running
PowerEdge C410x	PCIe chassis	1	8 HIC Inputs,16 x16 PCIe Sleds	running
NVIDIA M2075	Computing	4	PCIe x16 GPGPU	running
IBM x3650M4	xTB servers (~80TB fast SAS HDD)	6-8	2.9GHz, 2Sock, 8Core, Intel E5-2600, 96GB, Mellanox ConnectX-3 EN Dual NIC	ordering
IBM EXP25XX	xTB ext. chassis (slower)	~2		ordering
Demonstrator	TB	2	Board and ATCA crate	arriving 12.7

- Second ½ of slice will be ordered Q/3 or 4 (or later)
  - when result feedback is available, etc.

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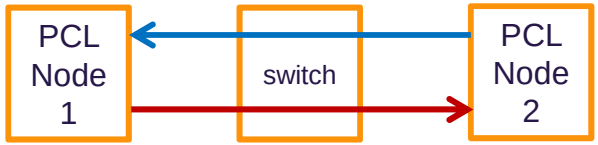
UDP bidirectional test (netperf and mpstat)

Two hosts (1+2), each dual 10Gbps NIC, connected via switch, settings:

- Socket buffer size (128kB-4MB)
- Adjusted kernel parameters
- MTU 9000 (Jumbo frames)
- CPU affinity enabled

```
net.core.rmem_max = 16777216          # 131071
net.core.wmem_max = 16777216          # 131071
net.core.rmem_default = 10000000      # 129024
net.core.wmem_default = 10000000      # 129024
net.core.netdev_max_backlog = 300000  # 1000
```



Bidirectional stream

UDP MTU 9000	send1	recv2	send2	recv1	send1	recv2	send2	recv1
buffer size B	512k	512k	512k	512k	1M	1M	1M	1M
bw Mb/s	9926	9927	9927	9927	9927	9927	9927	9927
packet loss %	0		0		0		0	
cpu sys %	27	26	28	25	26	26	28	25
cpu soft %	5	0.1	5	0.1	6	0.1	5	0.1
intr/s	8k	8k	8k	8k	8k	8k	8k	8k

Dual NIC allows concurrent read/write at wire speed, no packet loss for UDP

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Slice Test: PCL layer node work

Task

- Receive detector format data from FEI layer (TB)
- Process data (monitor, reject, format, aggregate)
- Write to data cache storage layer in final HDF5 format

Implementation

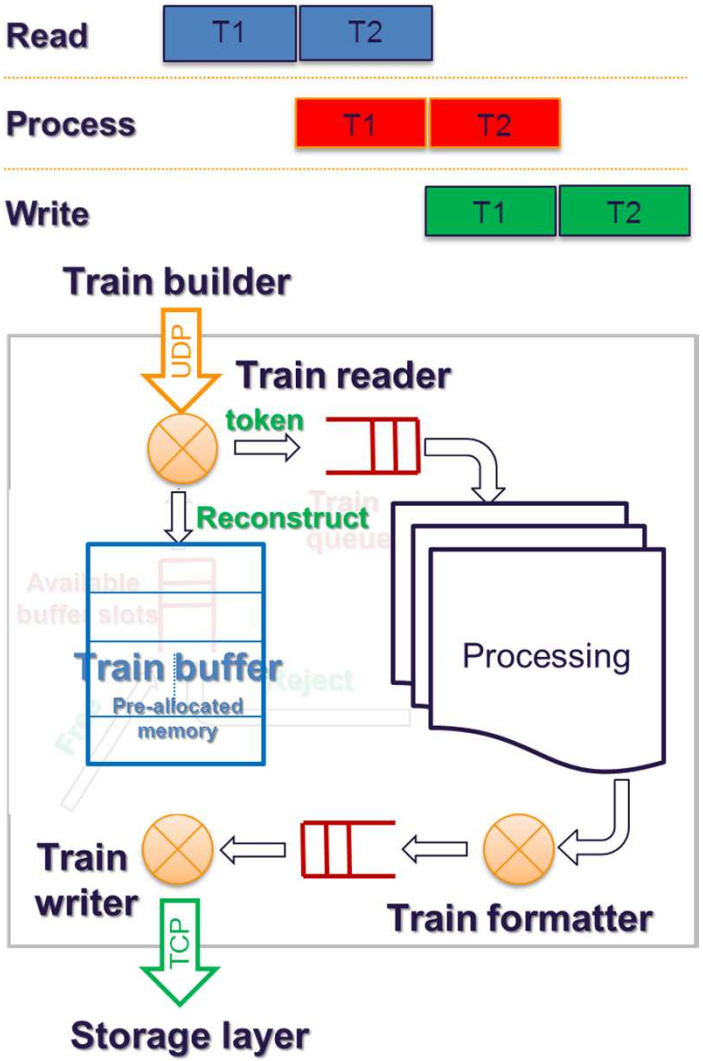
- PCL node s/w
  - is a framework device
  - has r,w worker threads and multi threaded processing pipeline
- Feeder device written for testing (drives PCL node)
  - uses LPD and TB detector formats
- Writes data using framework HDF5 API
  - uses vectors of attributes (images, image-descriptors, etc.)
- Processing pipeline implements
  - CRC calculation, later detector specific

Status

- PCL device software now being tested
  - network performance results concurrent r,w results verified
  - Measuring concurrent r,w,processing performance

Outlook

- Continuing tests processing, iWARP, etc.



Slice Test: Data Management services

Task

- Data formatting
- Generic scheme for data files and data objects
- Data Storage and access
- European wide authentication system (AAI)
- Data archiving and export services

Implementation

- Serialization of data structures (Hash) to HDF5
  - Optimized for high speed transfer – avoid memory copying, buffered writes and reads
  - Dynamic configuration and discovery of data format
- Naming convention
  - Directory structure and file names
  - Metadata definition -> DB schema
- Storage
  - Specialized and optimized setup for online data cache
  - Cluster file systems, NFS4.1 for offline storage
- AAI
  - Central/federated authentication system
  - Local facility based authorization
- Data archiving using dCache system, WAN transfer using gridFTP and bbcp tools

Status

- Released framework HDF5 related APIs
  - performance up to 2.4GB/s into RAM disk, storage limited performance
- Definition of file naming convention – in progress
- Storage tests
  - Waiting for hardware to be delivered
  - Further tests foreseen within CRISP project
- AAI
  - CRISP/WP16 - friendly user test phase of the prototype system involving >20 users from European institutes
- Data transfers:
  - Observed dCahce performance up to 600MB/s and up to 200MB/s to archive, no show stoppers seen
  - Test of bbcp and gridFTP tools performed, 80MB/s between SLAC and DESY

Outlook

- Database – start definition of database schema (new manpower from 1.06.2012)
- Configuration and tests of storage systems and cluster file system

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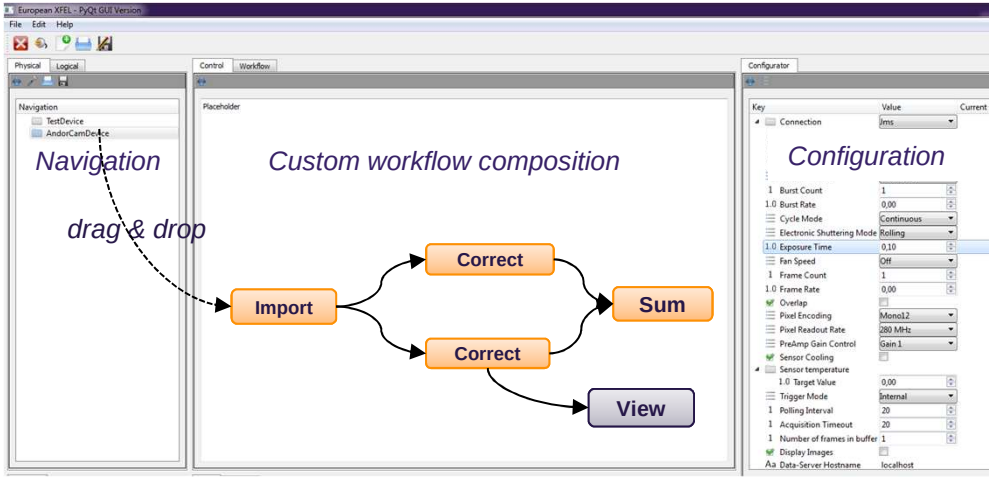
Slice Test: Scientific Computing

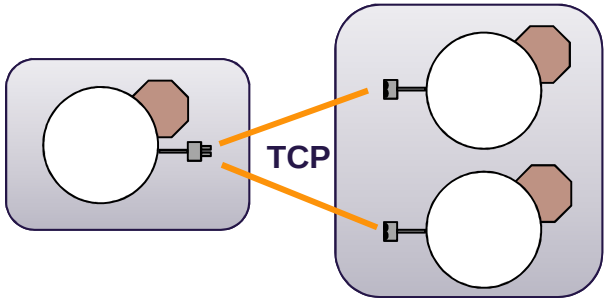
Task

- Adapt/Write analysis code to be a device (C++ or Python)
- Set up a device based scientific workflow system
- Enable GUI to configure workflows, do project management, visualize flowing data
- Provide a basic but generic image processing API for CPUs & GPUs



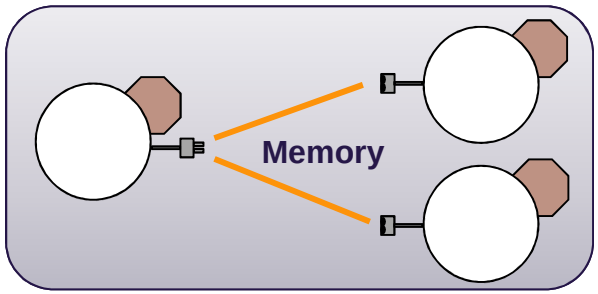
Implementation

- Configurable generic input/output channels on devices
- TCP based asynchronous p-2-p connection for *remote* IO channels
- Asynchronous (shared-)memory connection for *local* IO channels
- Automatic (API transparent) connection type selection (remote/local)
- Broker-based communication for (inter-device) workflow coordination
- Non-intrusive, plug-able serialization interface for data classes
- Drag & Drop of devices from GUI navigation pane into workflow
- Write abstract image interface class on top of Cimg and Cuda libs.



Status

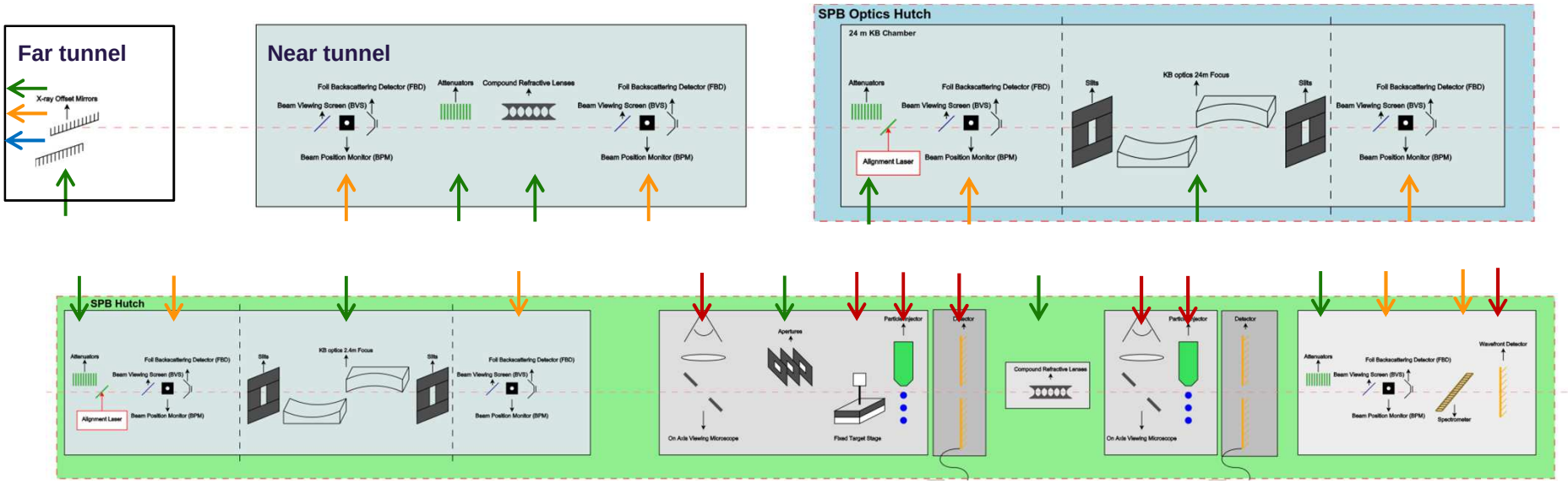
- First algorithms are being adapted (EMC, CrystFEL)
- Work started on image and serialization interface
- Code on workflow system has just been started, needs more time



Outlook

- Use slice test hardware to test distributed computation of CrystFEL algorithms (peak-detection, HKL-indexing, etc.)

PBS experiment, optics, diagnostics, e-machine integration – SPB experiment example



Component functionality to control / interface

- Diagnostics
  - stations, cameras, screens, eTOF**…**
- Optics
  - Focusing CRL, KB… components
  - Attenuators, apertures, slits…
- Experiments
  - Sample injection and laser systems
  - eTOF, diodes, 2D cameras, spectrometer…
- e-machine and undulators

Component (expt. only) control channel count

- Digital In/Out (412/52)
- Analog In/Out (168/9)
- Serial IO (39)
- Relays (48)
- Axis (241)
- Digitizers (1)
- Fast ADCs (28)
- Single shot cameras (9)
- Pixel cameras (2)
- …

Starting with SPB have produced a detailed description of DAQ and control requirements: crates, racks, power, networks, Beckhoff

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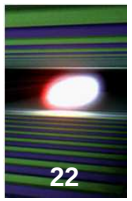
Conclusions

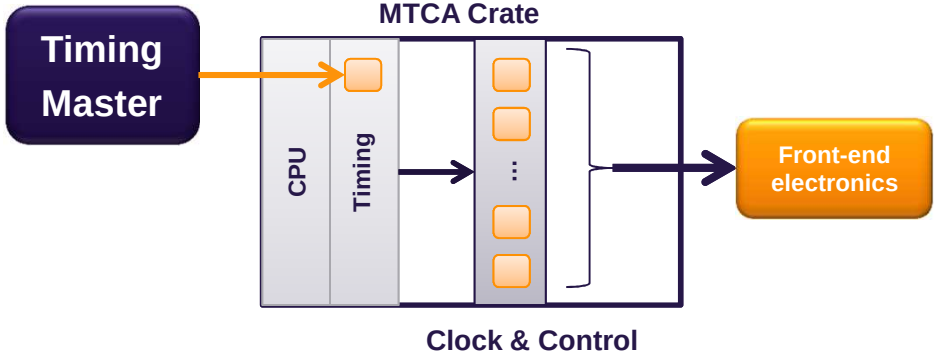
- Hardware…
  - Setting up joint electronics and FPGA group has helped enormously
  - All (most) use case detector types foreseen
- Software
  - First release exposed to non core device developers
  - DB design and API implementation coming soon
  - GUI development looks good
- Slice and other tests
  - As proof of architecture: positive initial results
  - As test platform for DAQ, DM and SC what we need
  - Field tests of devices in progress
- Integration
  - With experiments, diagnostics, optics and e-machine progressing
  - SC analysis algorithm integration progressing
- Future – still much to be done – most important end of year targets:
  - Fully operational control-DAQ-DM-SC slice test with associated s/w
  - Prototype level LPD, FastADC and Digitizer h+f+s/w systems
  - DB integrated, e-machine interface
  - Beckhoff cable DB and h/w installation prototypes
  - Feedback from data rejection, reduction, processing user workshop

Spare slides

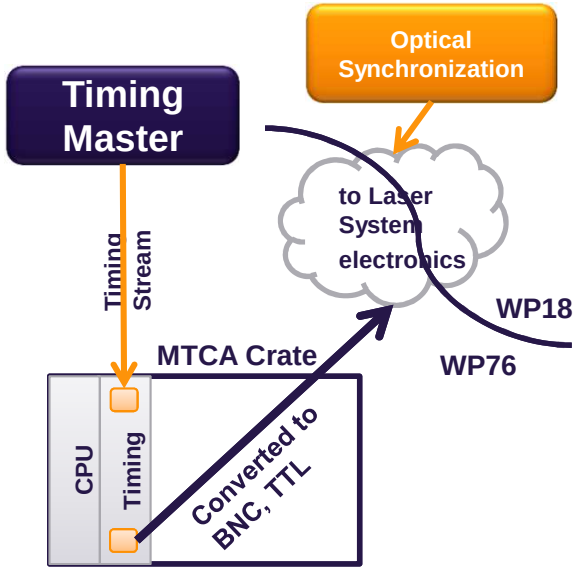


Timing and Synchronization Systems for XFEL

	Timing System (WP28)	Optical Synchronization (WP18)
Provides	Clocks, Triggers and Data	Clocks
Stability	Less than 10ps	Less than 50fs
Applications	DAQ and Detector sequencing	Synchronize lasers to beam



- Timing master distributes reference clock with encoded data
- Drift is actively compensated
- Transmits events used fur triggers (START) and bunch clocks
- Transmits bunch pattern and related information



- Optical synchronization is required to be in phase with beam
- Timing is required to select the correct pulses

European XFEL

WP76 members

Onsite

- C.Batindek – electronics intern
- D.Boukhelef – PCL and DM
- N.Coppola – Beckhoff
- S.Esenov – core s/w and devices
- B.Fernandes – electronics FPGA
- P.Gessler – electronics
- B.Heisen – core s/w and SC
- H.Hoehne – Bechof intern
- I.Koslova – core s/w and Python
- L.Maia – DB and API (>1.6.2012)
- A.Parenti – commercial cameras
- N.Shastri – electronics intern
- J.Szuba – slice test
- J.Tolkiehn – Beckhoff
- K.Weger – core s/w and GUI
- K.Wrona – cores s/w and DM
- C.Youngman - devices

Advertised

- Installation cable DB

To fill 2012

- DM scientist
- s/w manager
- DB manager
- DAQ scientist
- s/w developer
- Experiment support (devices)
- Electronics technician
- Analogue electronics (WP75)
- Electronics technician (WP75)

European XFEL

PBS WP76 mandates: DAQ, control, DM and SC

The PBS controls group (WP76) tasks in a Nutshell:

- DAQ and control = h/w and f/w control and readout systems and s/w interfacing
- Data Management (DM) = meta- and data handling h/w and s/w development, latter homogeneous framework for all PBS tasks
- Scientific Computing (SC) = data processing and analysis environment

Task areas and what this means

- **Experiments**
  - DAQ and control = experiment integration and running of experiments
  - DM = data and meta-data storage, processing, AAA, etc. for experimenters
  - SC = pipelines and processing environments for online and offline analysis for expeimenters
- **Beam line Optics**
  - DAQ and control = expt. control of optics systems (offset mirrors, attenuators…) and by WP73
  - DM = provide required data and meta-data services
- **Diagnostics**
  - DAQ and control = expt. control and configuration and by WP74
  - DM = provide required data and meta-data services
- **Machine**
  - Provide PBS side machine interfaces (e.g. s/w = to DOOCS and f+h/w = to MPS, interlocks…)
- **Undulators**
  - Provide PBS side undulator interface to WP71

European XFEL

TB demonstrator board testing

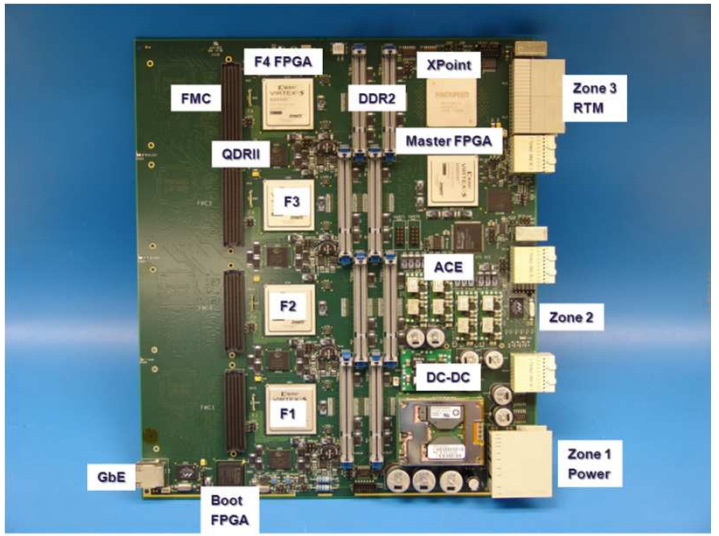
Test Status

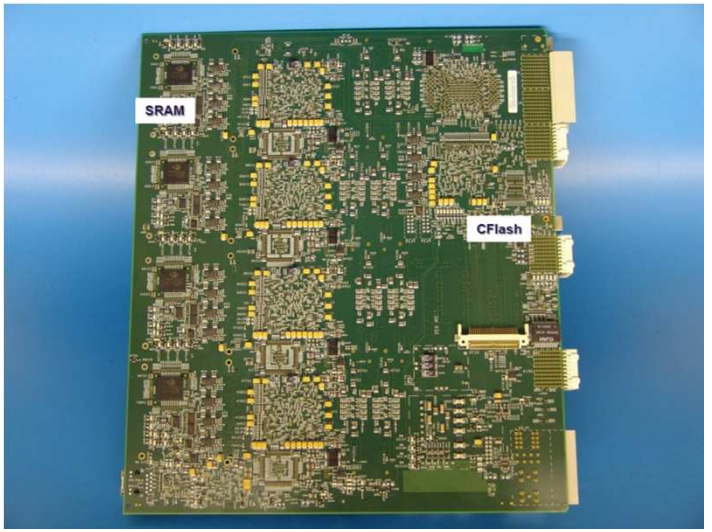
- FMCs 10G loopback (working)
- DDR2s Read & Write (preparing)
- SRAMs Read & Write (preparing)
- QDRIIs Read & Write (started)
- Clock distribution (partially tested)
- Cross-point switching static (working) dynamic (to do) operation
- Serial bus control from PC (Working)
- Ethernet GbE front panel control from PC (to do)
- Program FPGAs from System ACE card (Working)
- I2C chain (Temp monitoring devices, hot switch off) (working)
- Verify operation in ATCA Crate (front panels next week)
- Measure Power consumption

Schedule

- 16.5.2012 Order 2 more TBs
- 01.6.2012 Ship 1 TB to Hamburg
- 20.6.2012 Test in Hamburg
- 10.7.2012 thru12.7.2012
- 12.7.2012 TB&CC meeting at XFEL

Courtesy: John Coughlan (STFC) 10.5.2012





European XFEL

MTCA.4: 2U small crate with 6 slots

- Development with PowerBridge and Schroff
  - 2U high MTCA.4 crate with
    - 4 slots with double size AMC with RTM
    - 2 slots with double size AMC
    - 1 MCH
    - 1 Power Module
  - Prototype expected in May
  - When successfull, plan of
    - 4U high 12 slot version and
    - 6U high 12 slot version with full redundency